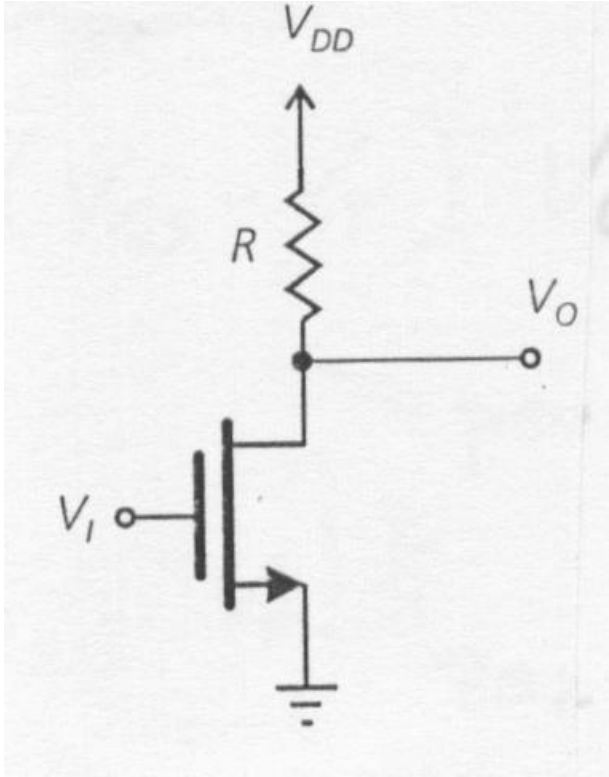
UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

I circuiti logici NMOS

A.Carini – Elettronica digitale

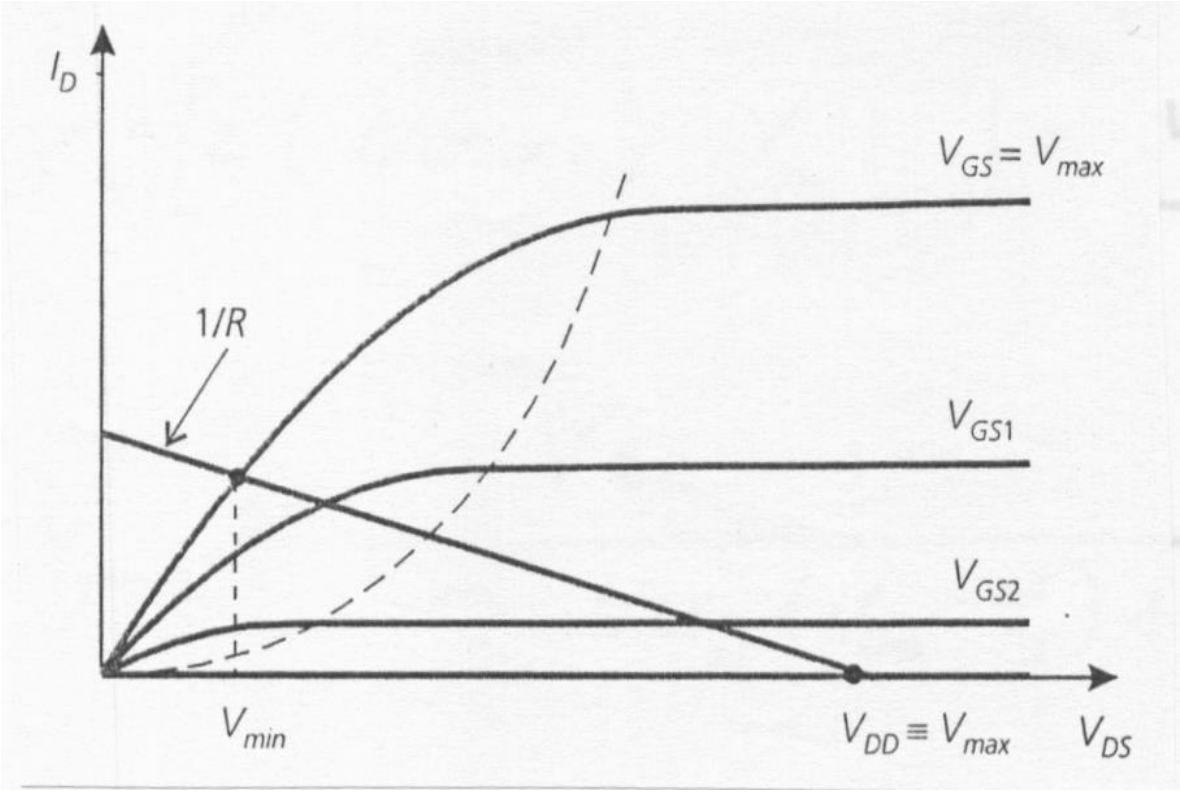
Invertitore NMOS



Analisi per via analitica

$$\begin{cases} I_D = f(V_{GS}, V_{DS}) \\ R\,I_D = V_{DD} - V_{DS} \end{cases}$$

Analisi per via grafica



Calcolo di Vmin

$$I_D = K_N\left[2(V_{GS} - V_T)\,V_{DS} - V_{DS}^2\right] \qquad \text{per} \quad V_{DS} < V_{GS} - V_T$$

$$I_D = K_N(V_{GS} - V_T)^2 \qquad \text{per} \quad V_{DS} \geq V_{GS} - V_T$$

Poniamo $V_I = V_{GS} = V_{DD}$

e calcoliamo $V_{\min} = V_O = V_{DS}$

Ipotesi: $V_{\min} = V_{DS} << 2(V_{GS} - V_T)$

Da cui $I_D = K_N\,2(V_{GS} - V_T)\,V_{DS}$

Calcolo di V_{min}

Poichè $$R\,I_D = V_{DD} - V_{DS}$$

$$K_N\,2(V_{GS} - V_T)\,V_{DS} = \frac{V_{DD} - V_{DS}}{R}$$

$$V_{\min} = V_{DS} = \frac{V_{DD}}{2\,K_N\,(V_{GS} - V_T)R + 1}$$

Progetto della resistenza R

Consideriamo:

$$\left.\begin{array}{l} k_n = 50\,\mu A/V^2 \\ W/L = 2 \end{array}\right\} K_N = 100\,\mu A/V^2$$

$$V_T = 1V \qquad V_{DD} = 5\,V$$

Imponiamo: $V_{\min} = 0.2\,V$

Si ottiene: $R = 30\ k\Omega$

Progetto della resistenza R

Per realizzare: $R = 30\ k\Omega$

Utilizziamo area drogata con resistenza $50\Omega/\square$

L= 600 W

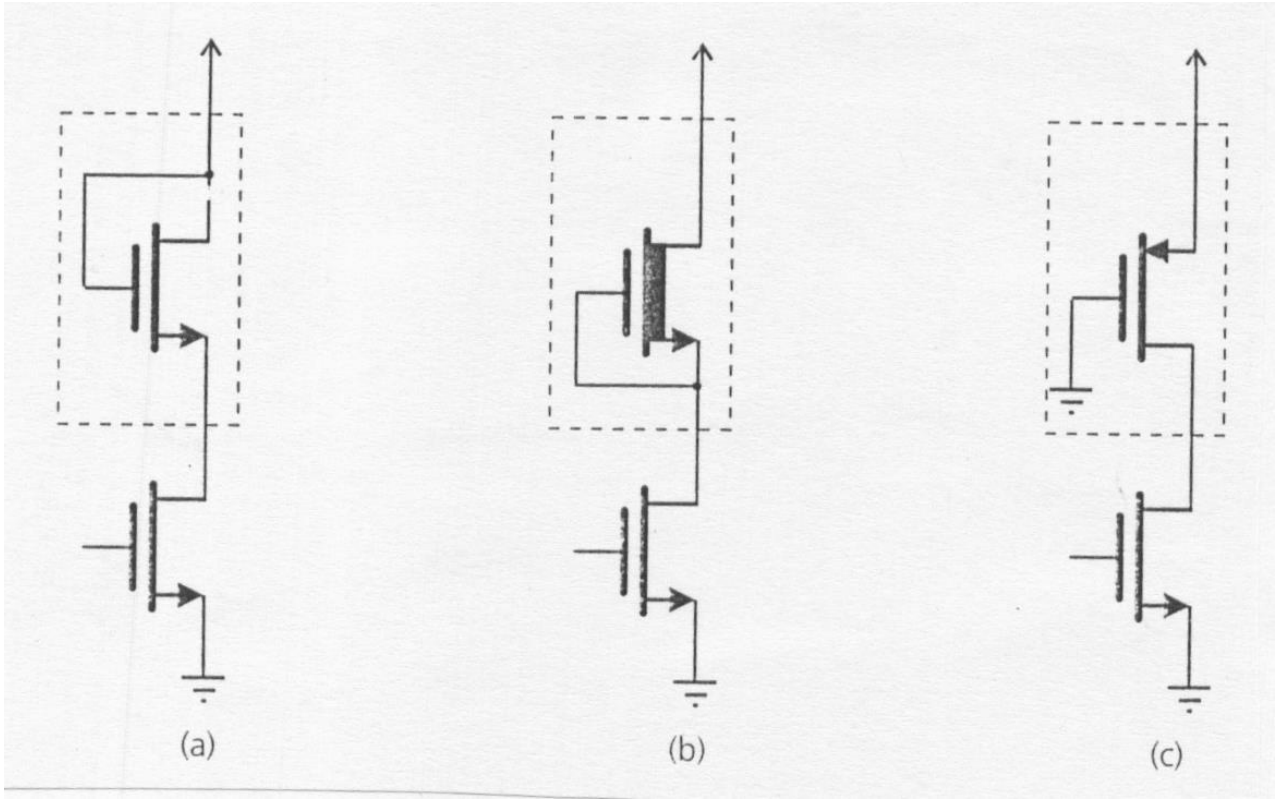
Detta λ minimum-feature-size

Minima dimensione di una resistenza: 3λ

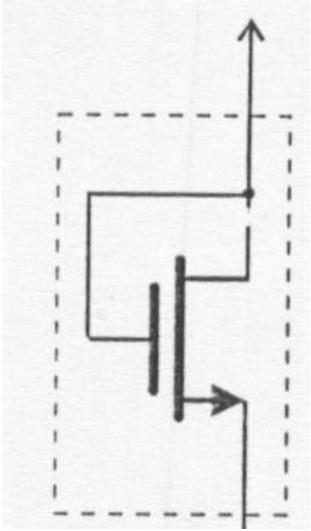
Minima area di gate: $2\lambda \times 3\lambda$

Minima area resistenza da 30 kOhm: $1800\lambda \times 3\lambda$!!!

Invertitore NMOS con carico attivo



NMOS ad arricchimento

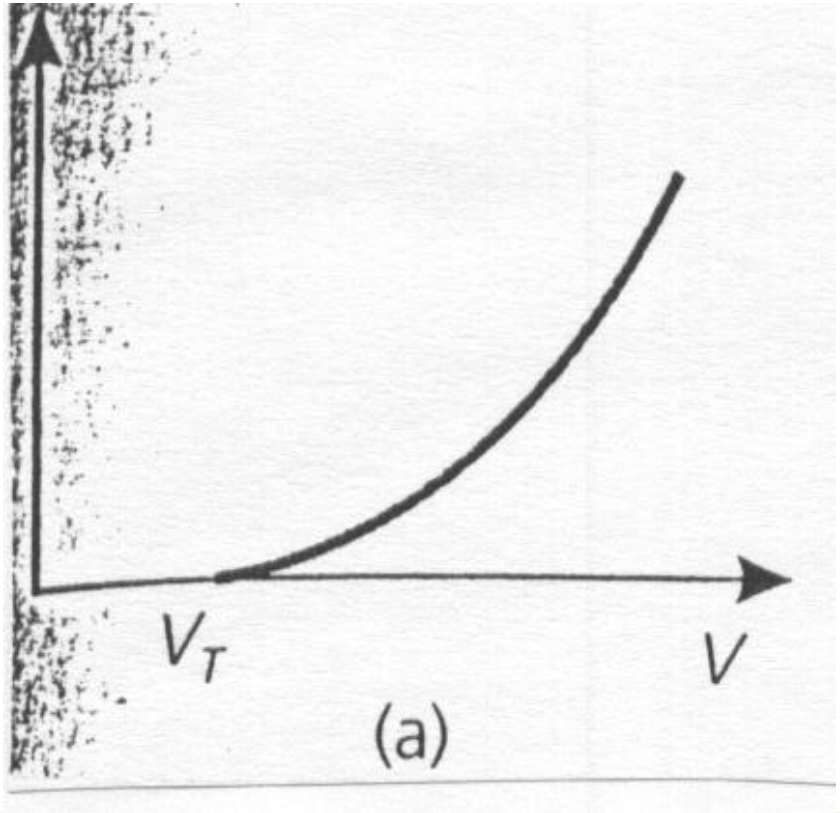


$$V_{DG} = 0$$

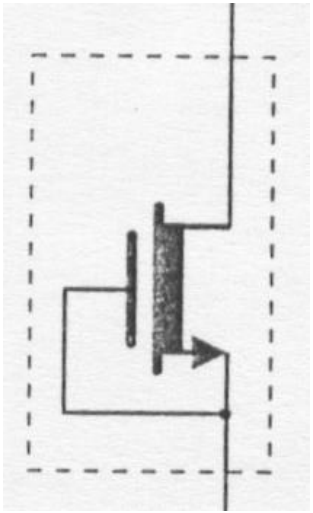
$$V = V_{DS} = V_{GS}$$

$$I = I_D = K_N \left(V - V_T\right)^2$$

NMOS ad arricchimento



NMOS a svuotamento



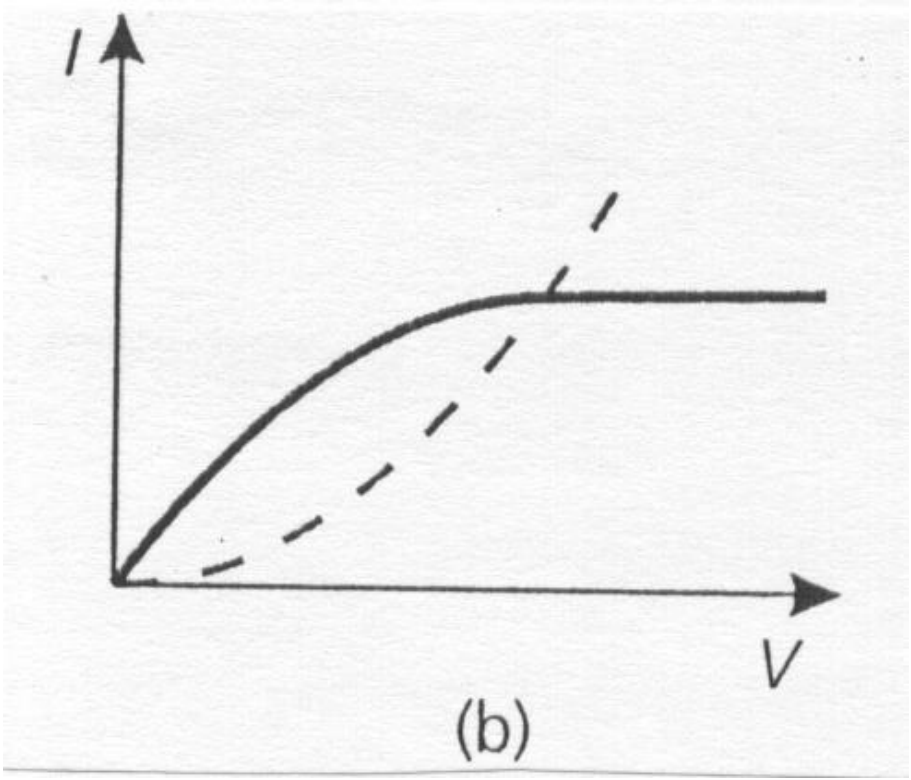
$$V_{GS} = 0$$

$$V_{GS} - V_{TD} = |V_{TD}|$$

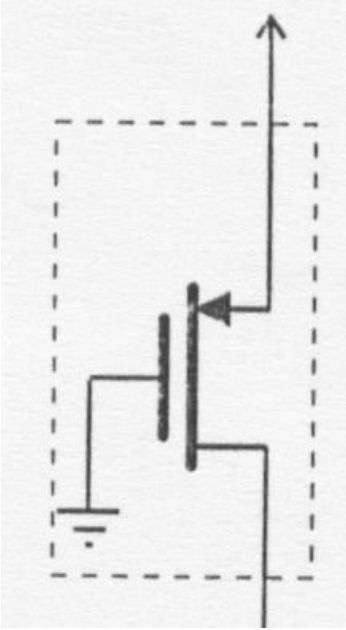
$$I_D = K_N \left[2|V_{TD}| V_{DS} - V_{DS}^2 \right] \qquad \text{per } V_{DS} < |V_{TD}|$$

$$I_D = K_N |V_{TD}|^2 \qquad \text{per } V_{DS} \geq |V_{TD}|$$

NMOS a svuotamento



PMOS ad arricchimento



$$|V_{GS}| = V_{DD}$$

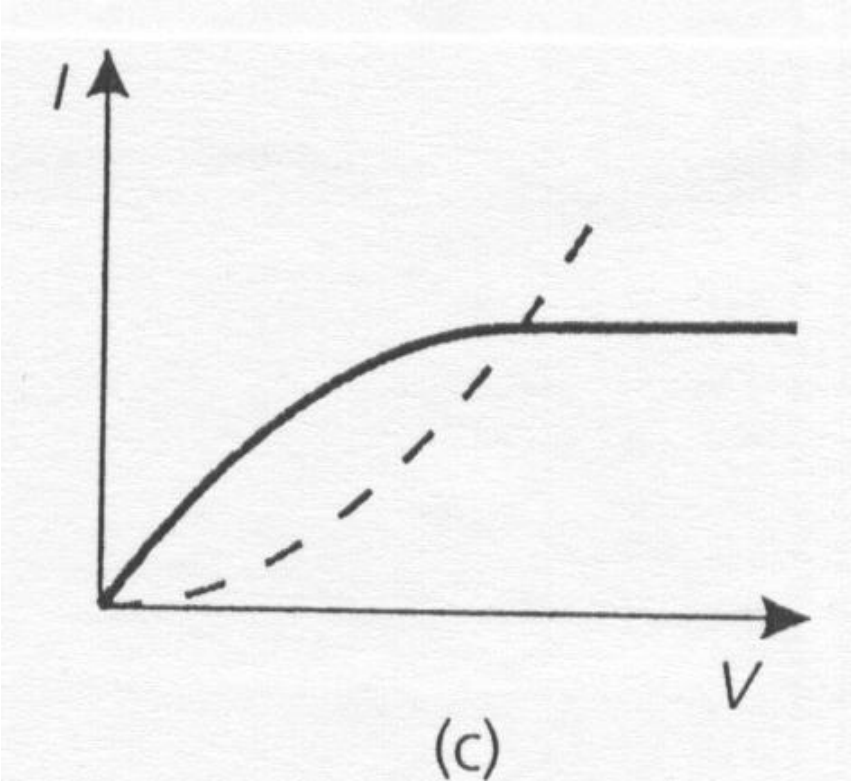
$$I_D = K_P\left[2(V_{DD} - |V_{TP}|)\,|V_{DS}| - |V_{DS}|^2\right]$$

per $\quad |V_{DS}| < V_{DD} - |V_{TP}|$

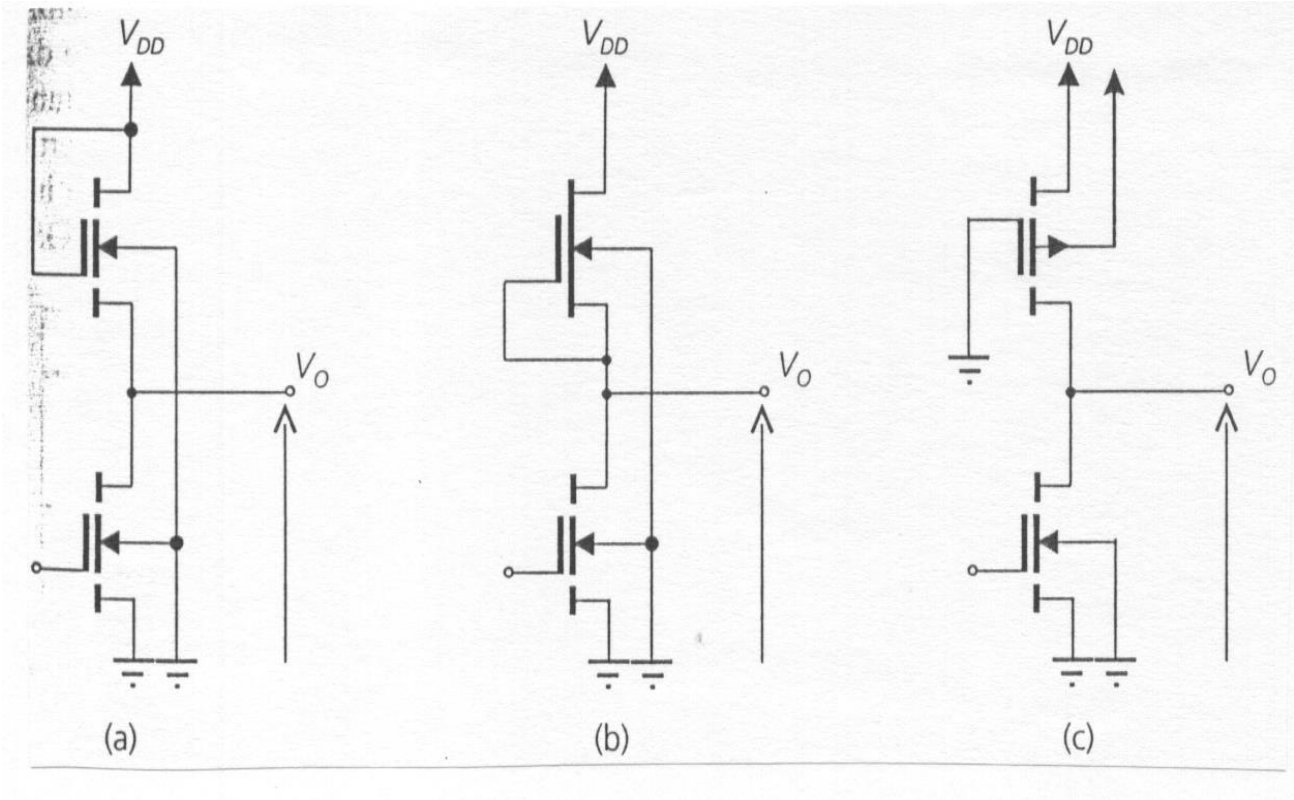
$$I_D = K_P(V_{DD} - |V_{TP}|)^2$$

per $\quad |V_{DS}| \geq V_{DD} - |V_{TP}|$

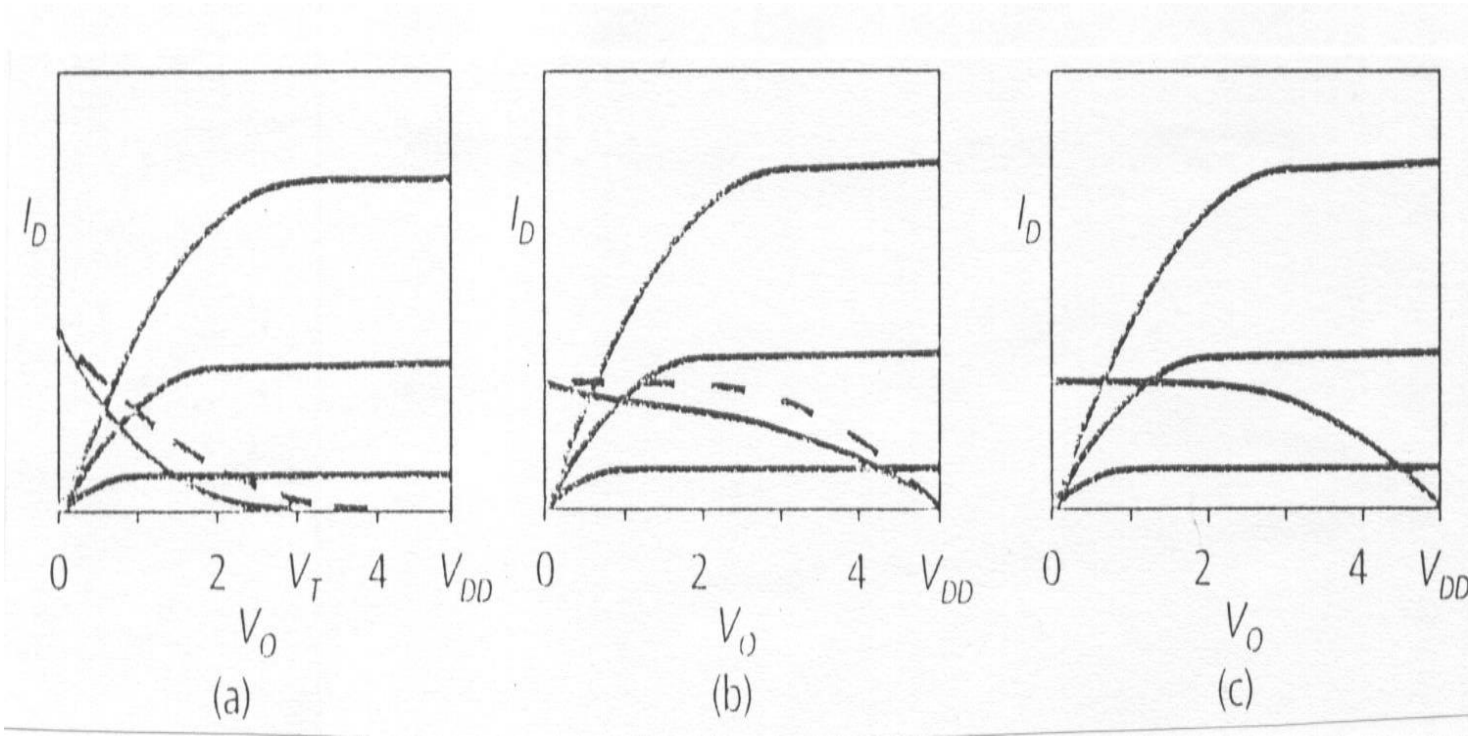
PMOS ad arricchimento



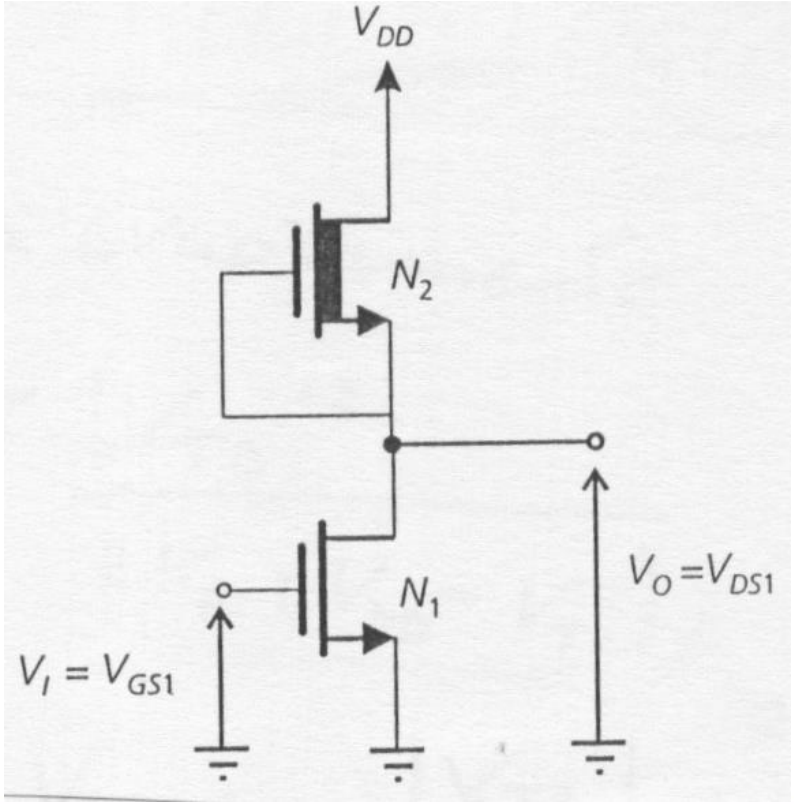
Invertitore con carico attivo



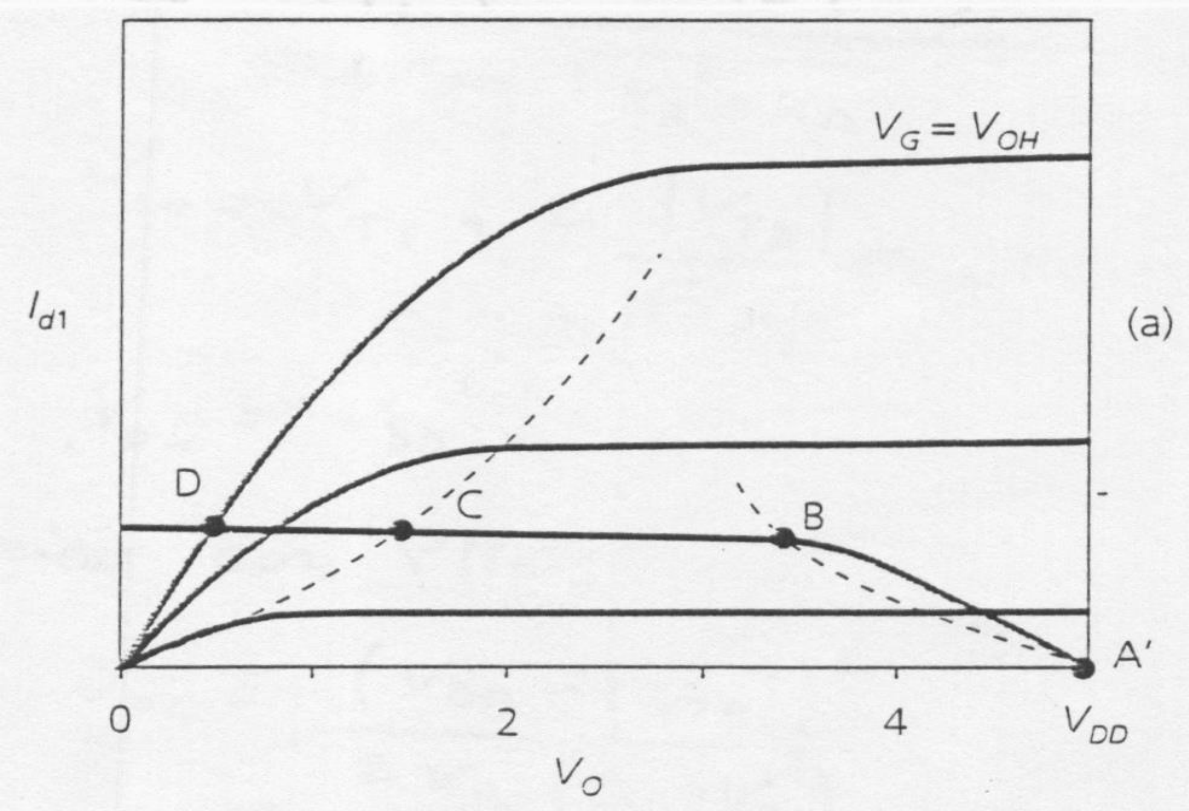
Invertitore con carico attivo



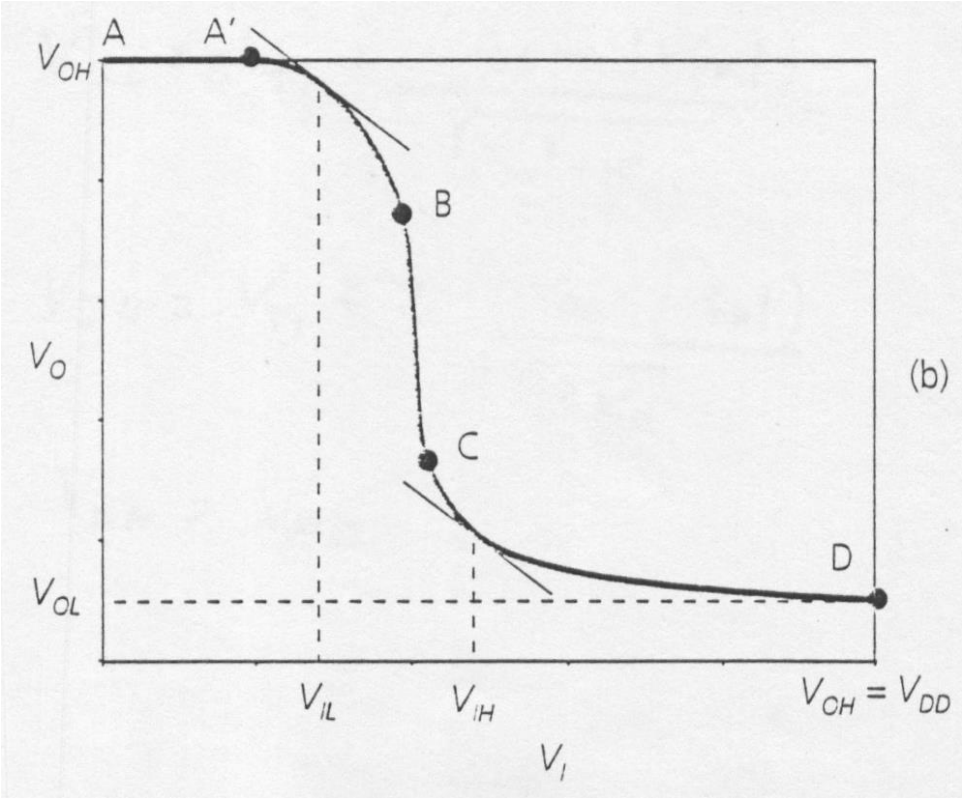
Caratteristica di trasferimento



Caratteristica di trasferimento



Caratteristica di trasferimento



Caratteristica di trasferimento

A – A’ : N1 interdetto, N2 in r. di triodo

$$V_I < V_T, \quad V_O = V_{DD}$$

A’ – B : N1 in r. di pinch-off, N2 in r. di triodo

B – C : N1 ed N2 in r. di pinch-off

C – D : N1 in r. di triodo, N2 in r. di pinch-off

Livelli logici con NMOS a svuotamento

$$V_{OL} \cong \frac{|V_{TD}|^2}{2K_R(V_{DD} - V_{T1})}$$

$$V_{IL} = V_{T1} + \frac{|V_{TD}|}{\sqrt{K_R{}^2 + K_R}}$$

$$V_{IH} = V_{T1} + 2\frac{|V_{TD}|}{\sqrt{3K_R}}$$

$$V_{OH} = V_{DD}$$

$$K_R = \frac{K_1}{K_2}$$

Livelli logici con PMOS ad arricchimento

$$V_{OL} \cong \frac{\left(V_{DD} - |V_{TP}|\right)^2}{2K_R\left(V_{DD} - V_{T1}\right)}$$

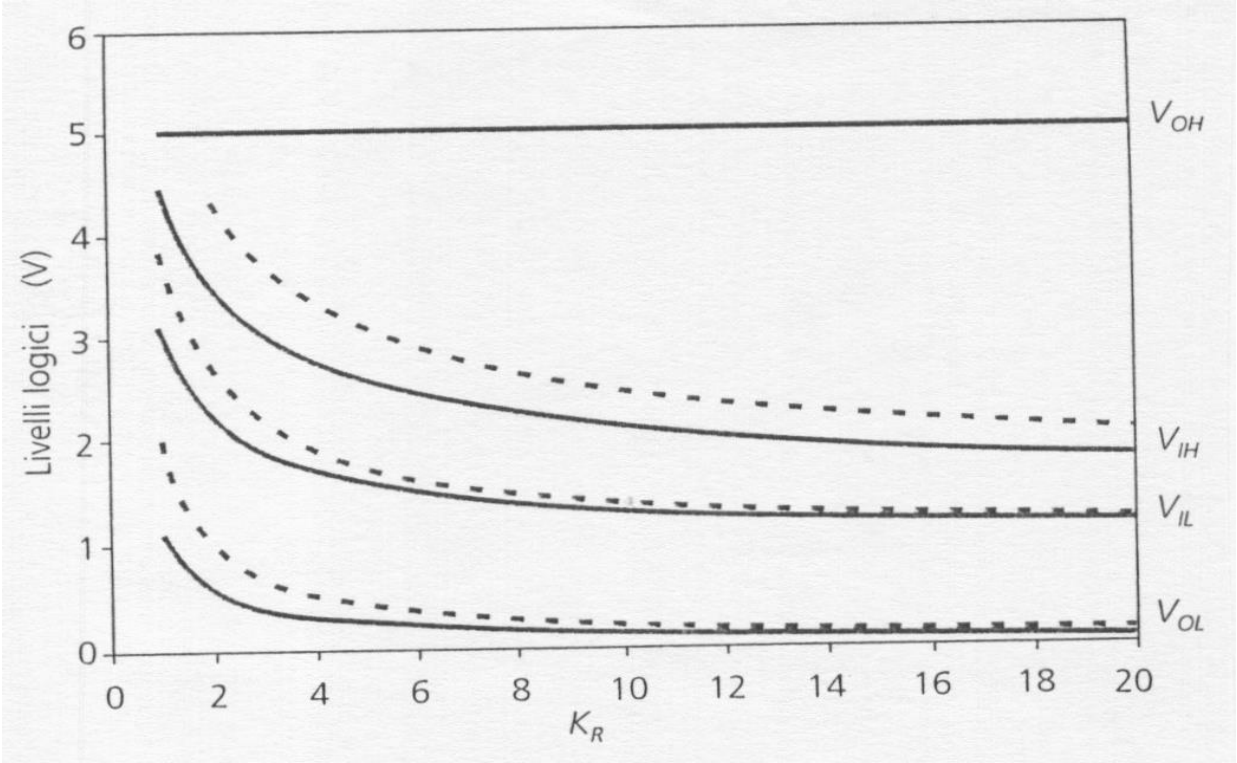
$$V_{IL} = V_{T1} + \frac{\left(V_{DD} - |V_{TP}|\right)}{\sqrt{K_R{}^2 + K_R}}$$

$$V_{IH} = V_{T1} + 2\frac{\left(V_{DD} - |V_{TP}|\right)}{\sqrt{3K_R}}$$

$$V_{OH} = V_{DD}$$

$$K_R = \frac{K_1}{K_2}$$

Livelli logici



K_R

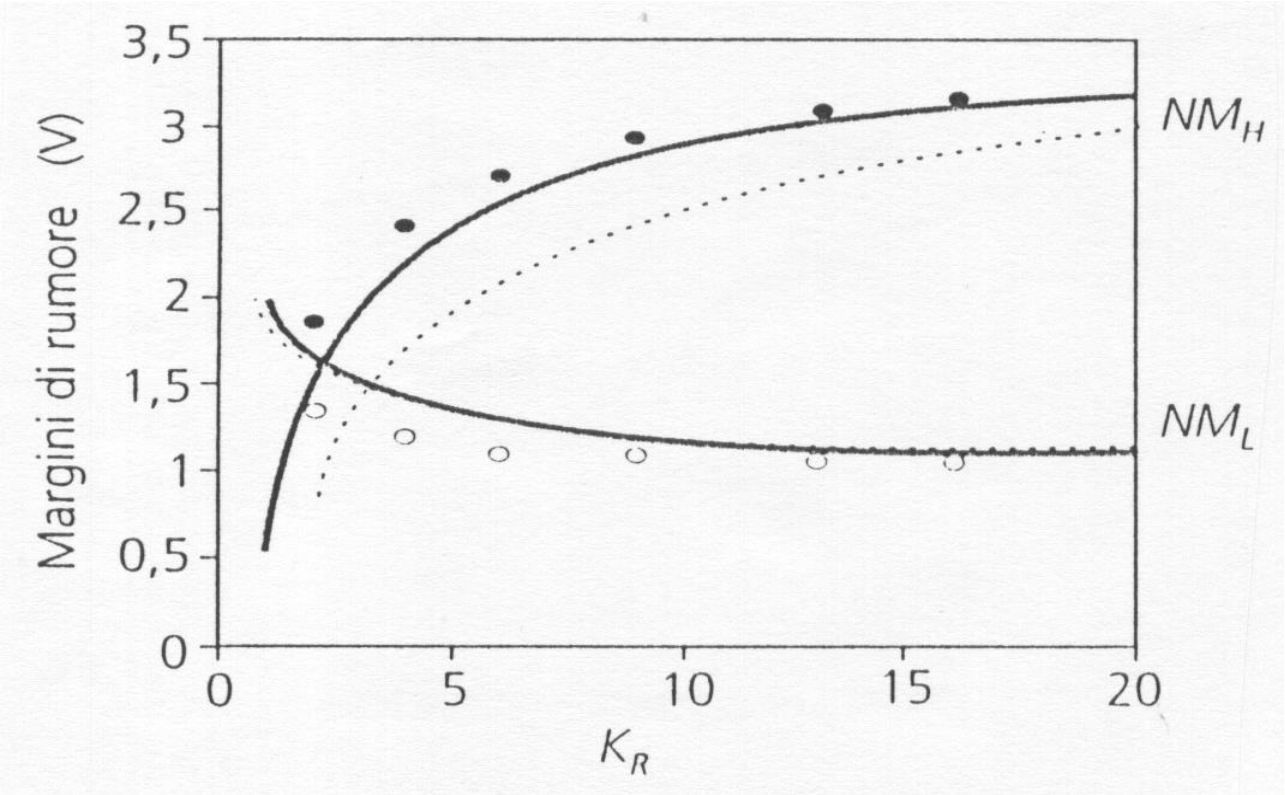
- Invertitore con carico NMOS a svuotamento

$$K_{R,N} = \frac{K_1}{K_2} = \frac{W_1}{W_2}\frac{L_2}{L_1}$$

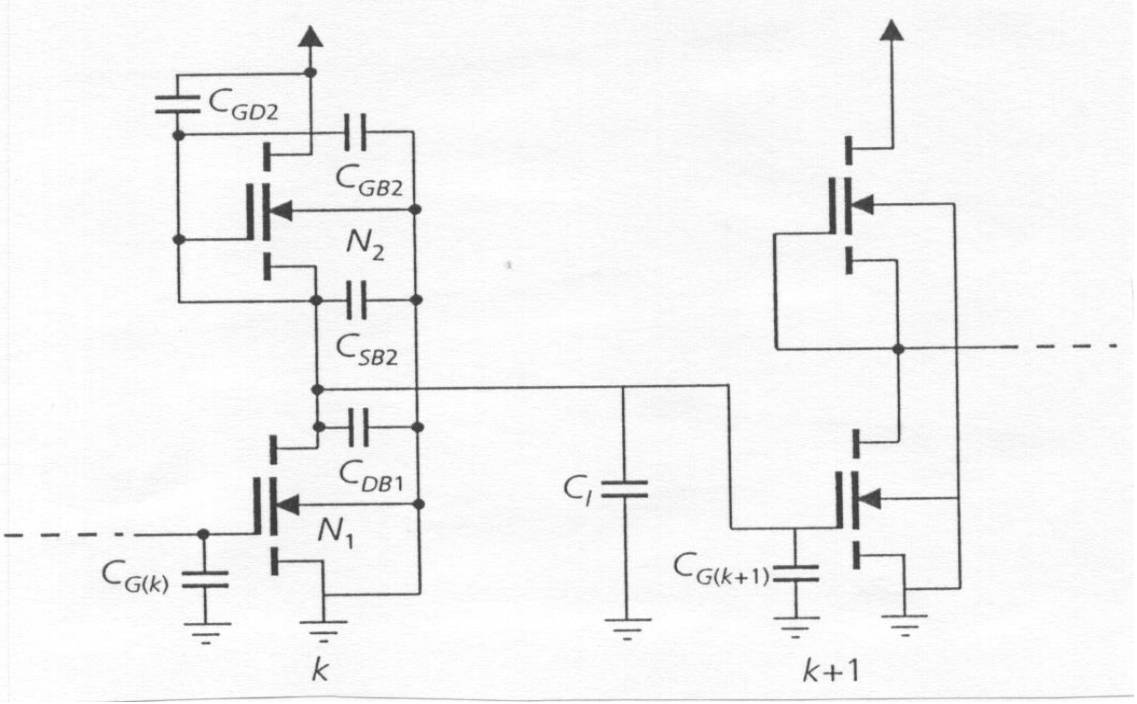
- Invertitore con carico PMOS ad arricchimento

$$K_{R,P} = \frac{K_1}{K_2} = \frac{\mu_N}{\mu_P}\frac{W_1}{W_2}\frac{L_2}{L_1} \cong 2{,}5\,\frac{W_1}{W_2}\frac{L_2}{L_1}$$

Margini di rumore

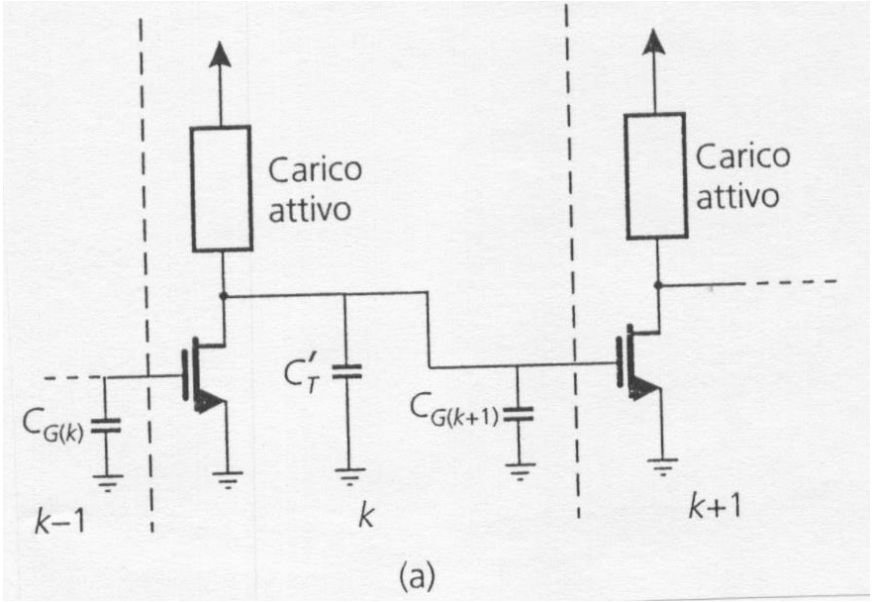


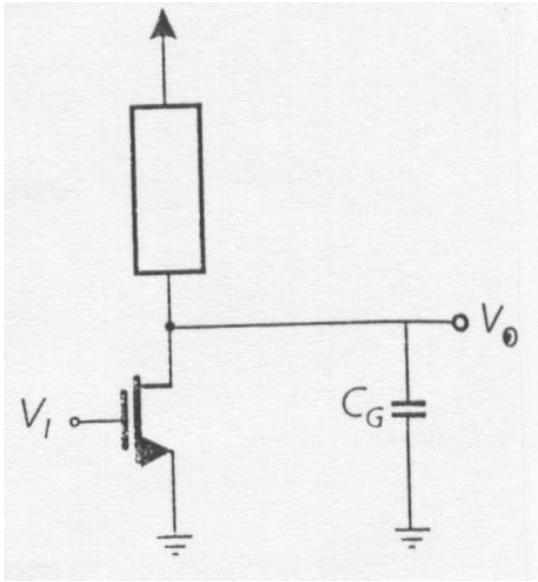
Capacità del circuito



$$C_G = C_{GS} + C_{GB} + C_{GD}$$

Capacità del circuito

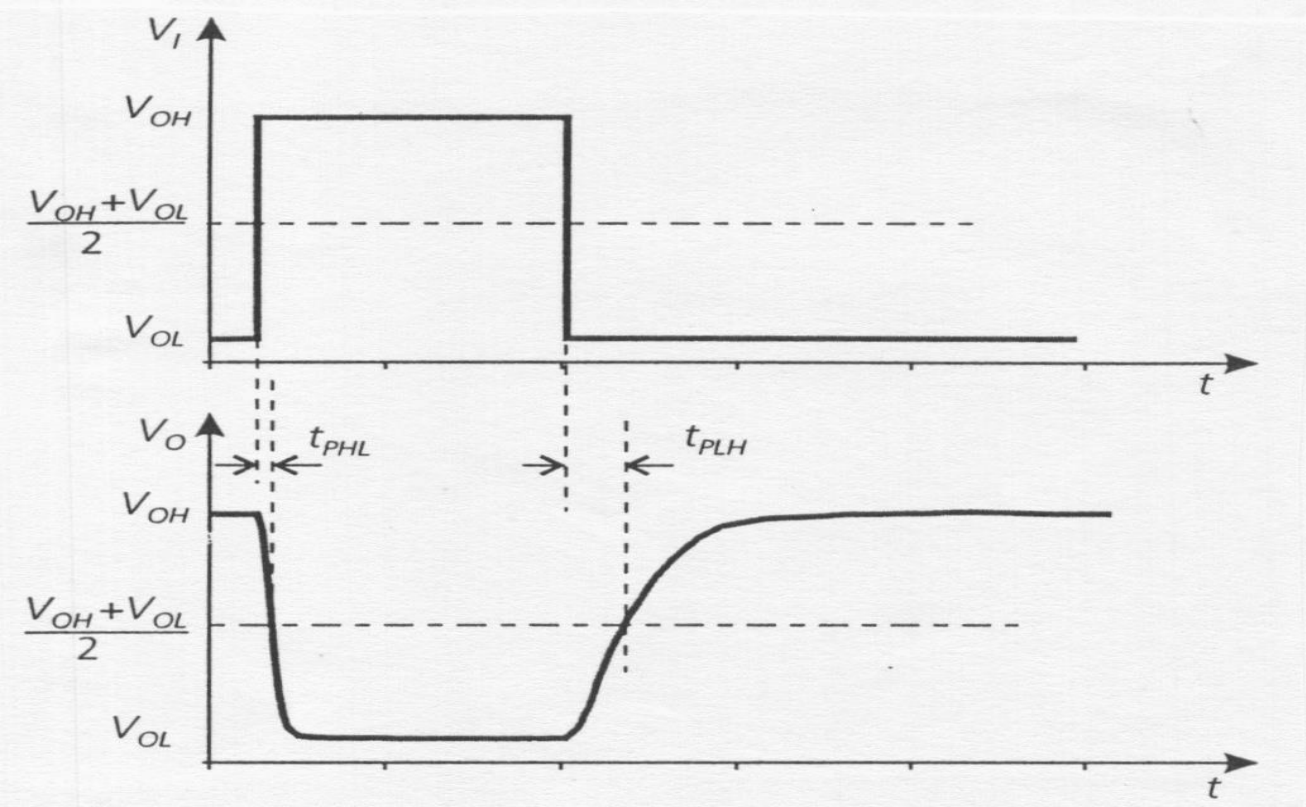




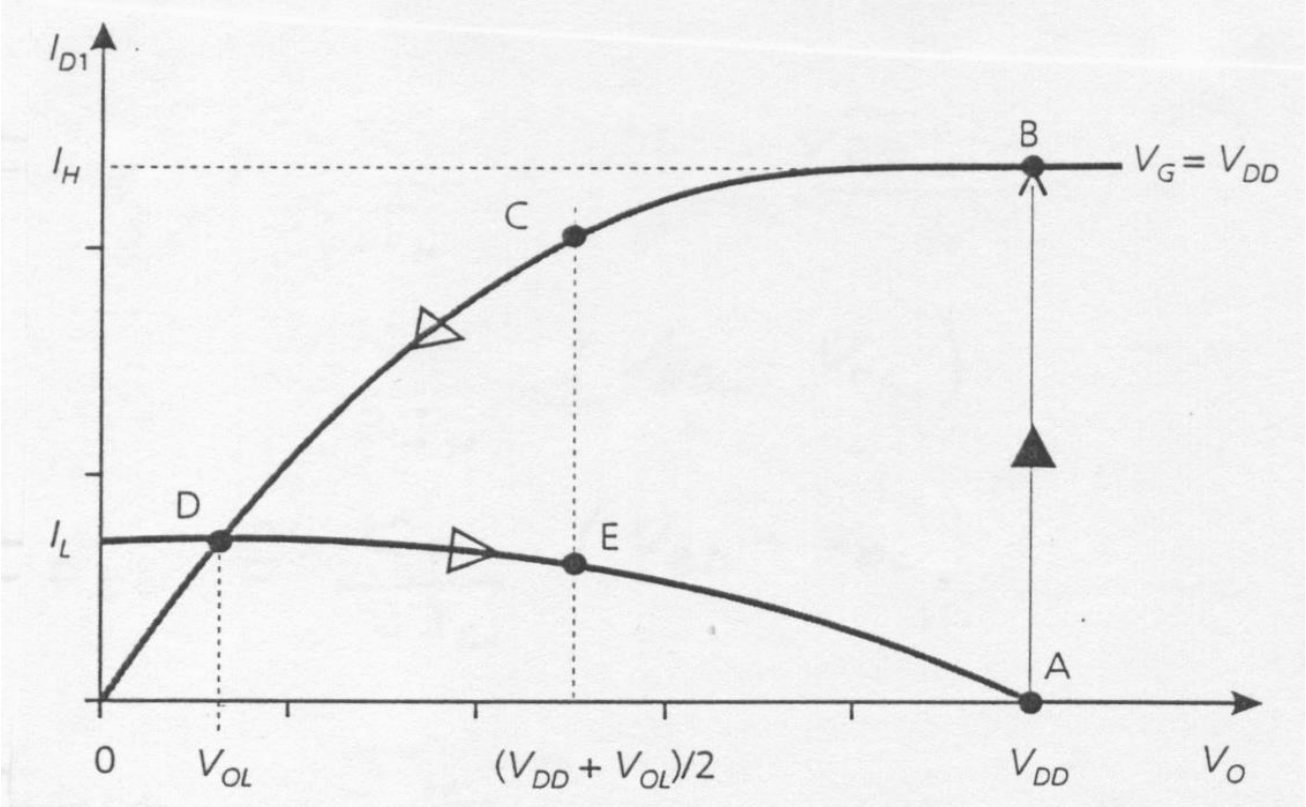
$$C_{T,NMOS} = C_{DB1} + C_{SB2} + C_{GD2} + C_{GB2} + C_l + C_{G(K+1)}$$

$$C_{T,pNMOS} = C_{DB1} + C_{DB2} + C_{GD2} + C_l + C_{G(K+1)}$$

Tempi di propagazione



Analisi grafica



Tempi di propagazione - calcolo

$$i(t) = C_T \frac{dV}{dt} \quad \Rightarrow \quad dt = C_T \frac{dV}{i(t)}$$

$$t_{PHL} = C_T \int_{V_{DD}}^{V^*} \frac{1}{i_C} dV_o = C_T \int_{V_{DD}}^{V^*} \frac{1}{-i_{N1} + i_{N2}} dV_o$$

$$t_{PLH} = C_T \int_{V_{OL}}^{V^*} \frac{1}{i_C} dV_o = C_T \int_{V_{OL}}^{V^*} \frac{1}{i_{N2}} dV_o$$

Dove: $V^* = \frac{V_{OL} + V_{OH}}{2}$

Tempi di propagazione - calcolo

$$t_P = \frac{1}{2}\left(t_{PHL} + t_{PLH}\right) \cong \frac{t_{PLH}}{2} = \frac{C_T}{4I_L}\left(V_{DD} - V_{OL}\right)$$

Invertitore NMOS:

$$t_P \cong \frac{t_{PLH}}{2} = \frac{C_T}{4K_2}\frac{\left(V_{DD} - V_{OL}\right)}{\left|V_{TD}\right|^2}$$

Invertitore pseudo-NMOS:

$$t_P \cong \frac{t_{PLH}}{2} = \frac{C_T}{4K_2}\frac{\left(V_{DD} - V_{OL}\right)}{\left(V_{DD} - \left|V_{TP}\right|\right)^2}$$

Potenza dissipata

$$V_I = V_{OL} \longrightarrow P_D = 0$$

$$V_I = V_{OH} \longrightarrow P_D = I_{D2}(V_{OL})\,V_{DD}$$

$$P_{D,media} = \frac{I_{D2}(V_{OL})\,V_{DD}}{2}$$

Invertitore NMOS:

$$P_D = \frac{K_2}{2}\left|V_{TD}\right|^2 V_{DD}$$

Invertitore pseudo-NMOS:

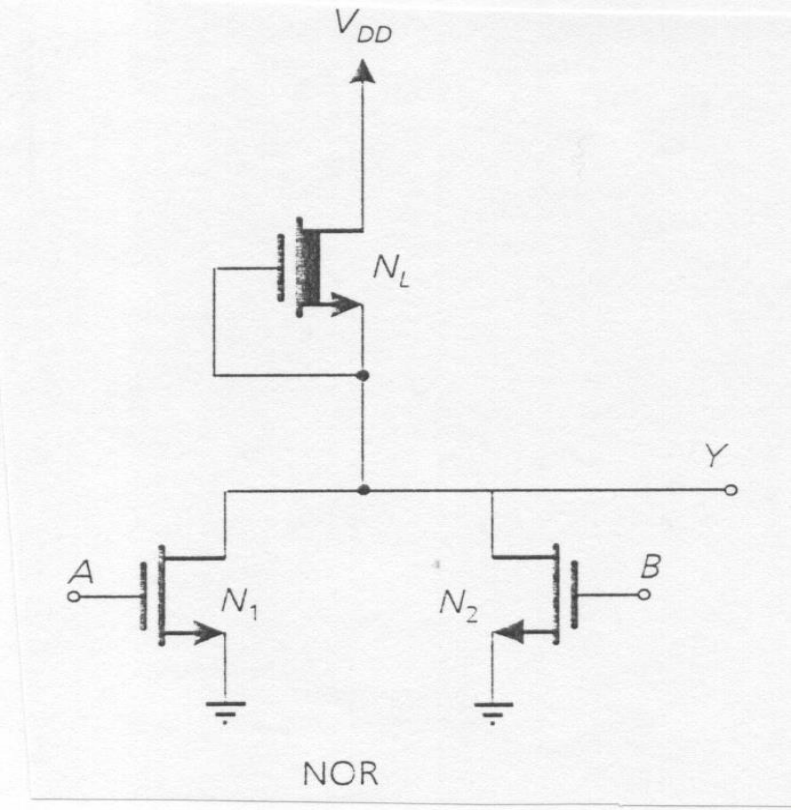
$$P_D = \frac{K_2}{2}\left(V_{DD} - \left|V_{TP}\right|\right)^2 V_{DD}$$

Prodotto Ritardo Potenza

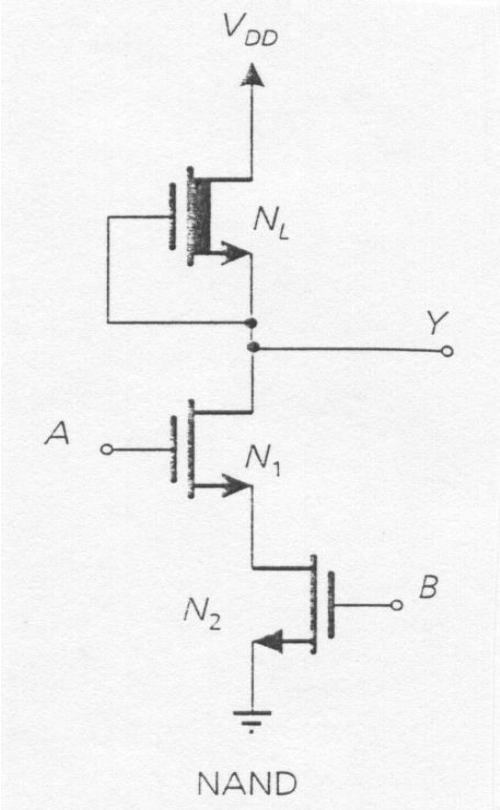
$$P_D \cdot t_P = P \cdot D = \frac{C_T}{8}\left(V_{DD} - V_{OL}\right)V_{DD}$$

$$\cong \frac{C_T}{8} V_{DD}^{\ 2}$$

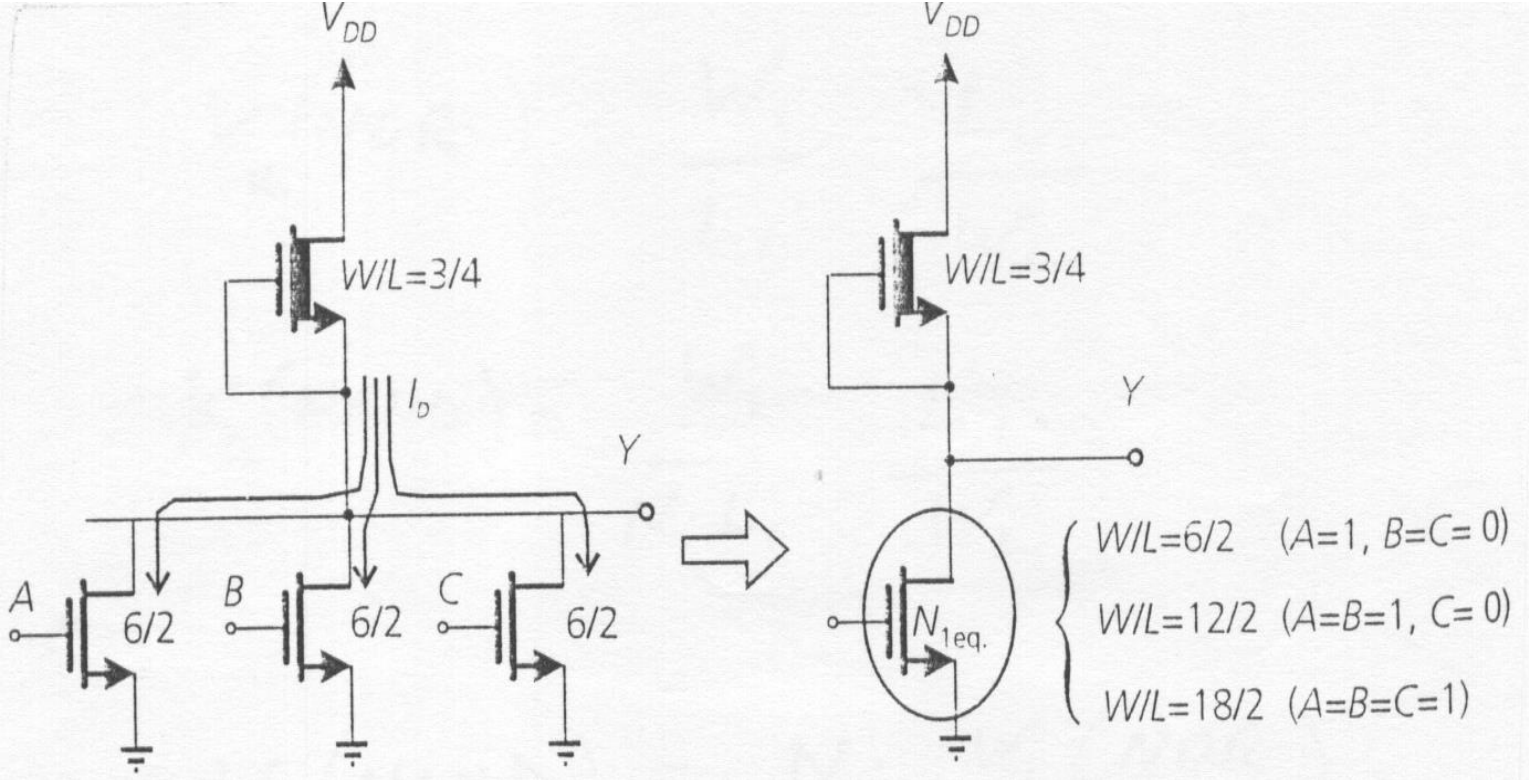
Porta NOR NMOS



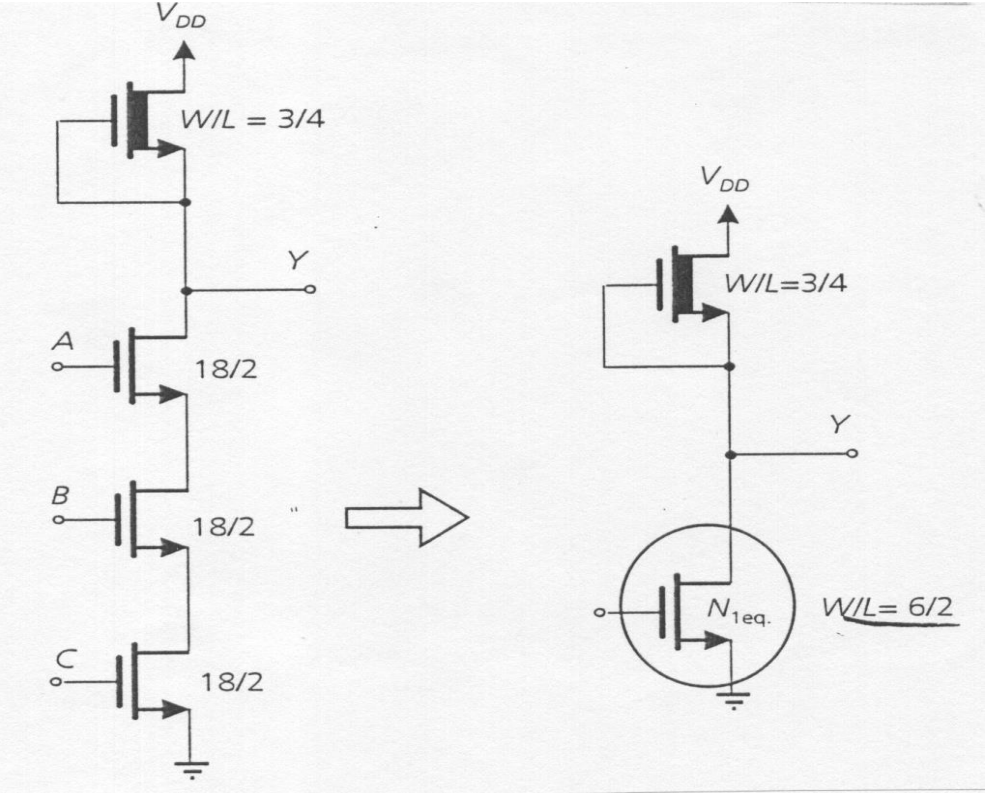
Porta NAND NMOS



Dimensionamento dei MOS



Dimensionamento dei MOS



Confronto NOR - NAND

$$V_{OL(W.C.)}\Big|_{NOR} \Rightarrow \frac{W_1}{L_1}\frac{L_2}{W_2} = K_R(NOR)$$

$$V_{OL}\Big|_{NAND} \Rightarrow \frac{W_1}{N\ L_1}\frac{L_2}{W_2} = K_R(NAND)$$

A parità di prestazioni statiche, ovvero di V_{OL}

$$W_{1,NAND} = N\ W_{1,NOR}$$

FAN-OUT e FAN-IN

- FAN-OUT
  - Limitazioni dovute alle prestazioni dinamiche ed all'aumento del carico capacitivo in uscita
  - 5 – 6 porte
- FAN-IN
  - Infinito per le porte NOR
  - 5 – 6 ingressi per le NAND a causa dell'aumento della capacità di gate con il numero degli ingressi

Vedere:

- Paolo Spirito, “Elettronica Digitale”, Ed. McGraw-Hill
  - Cap. 4.1-4.6
  - Cap. 4.8-4.14