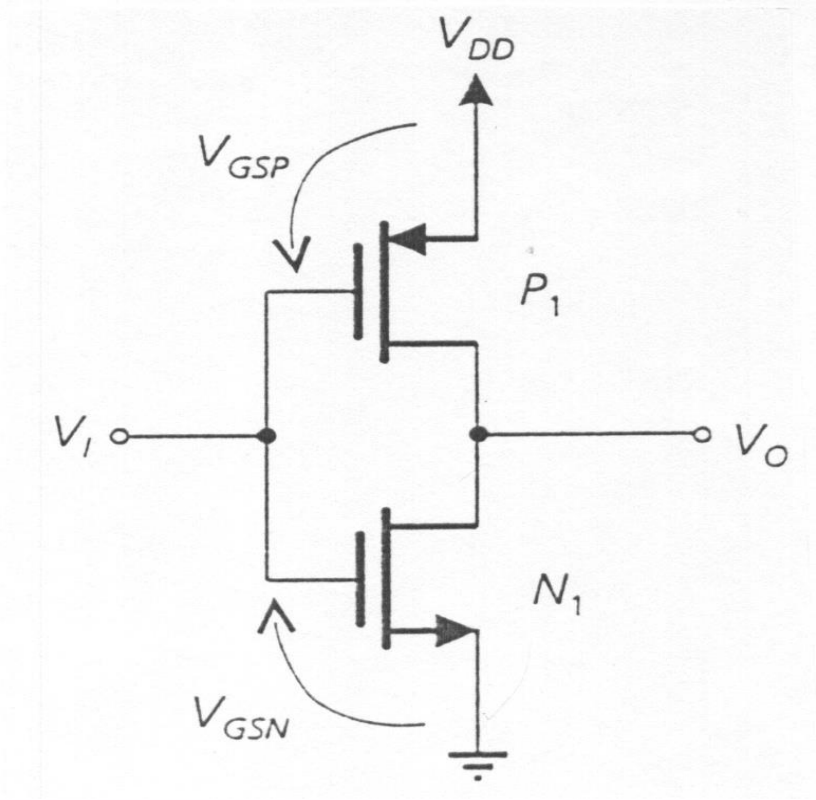
UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

I circuiti logici CMOS

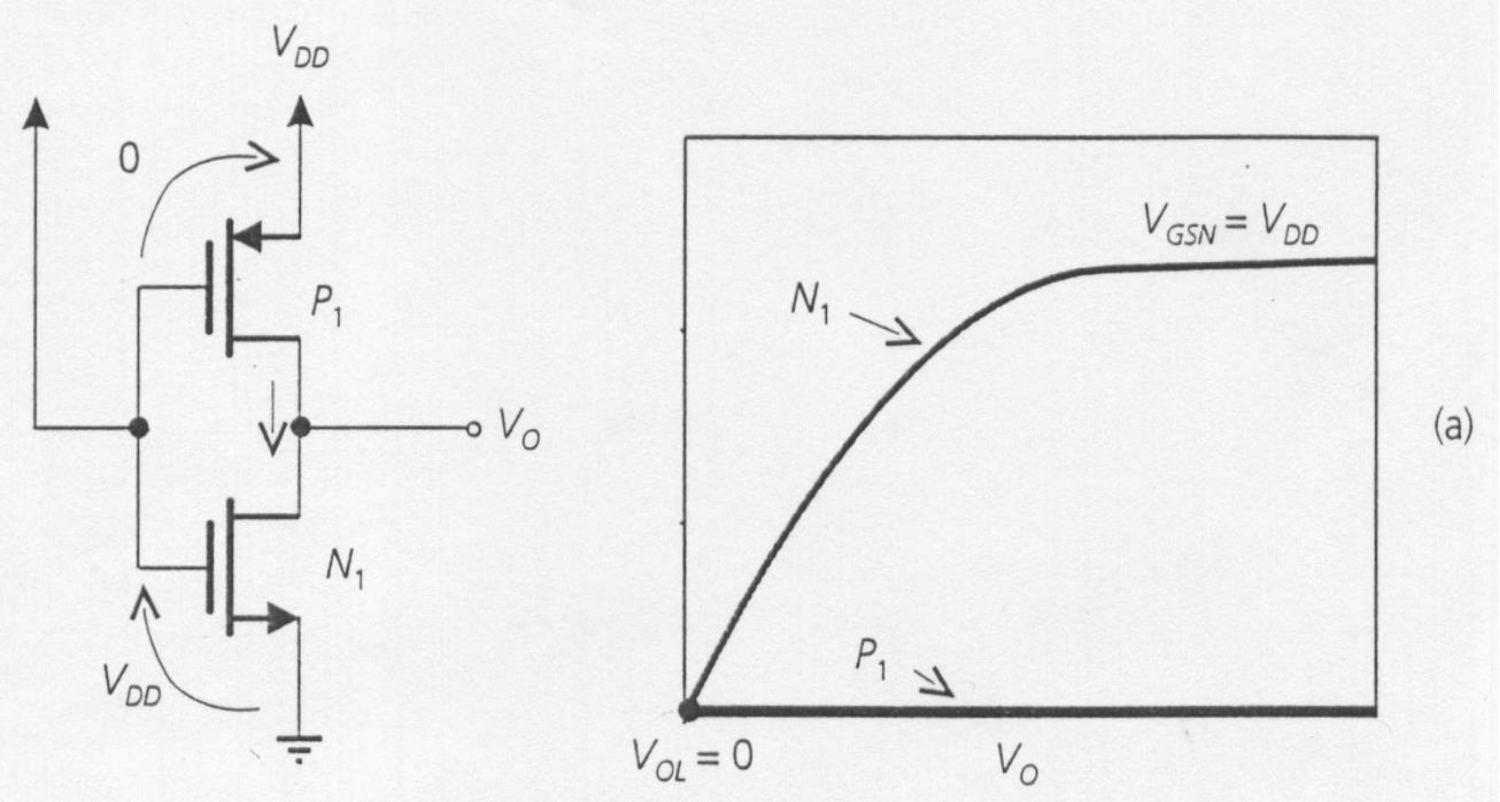
A.Carini – Elettronica digitale

L’invertitore CMOS

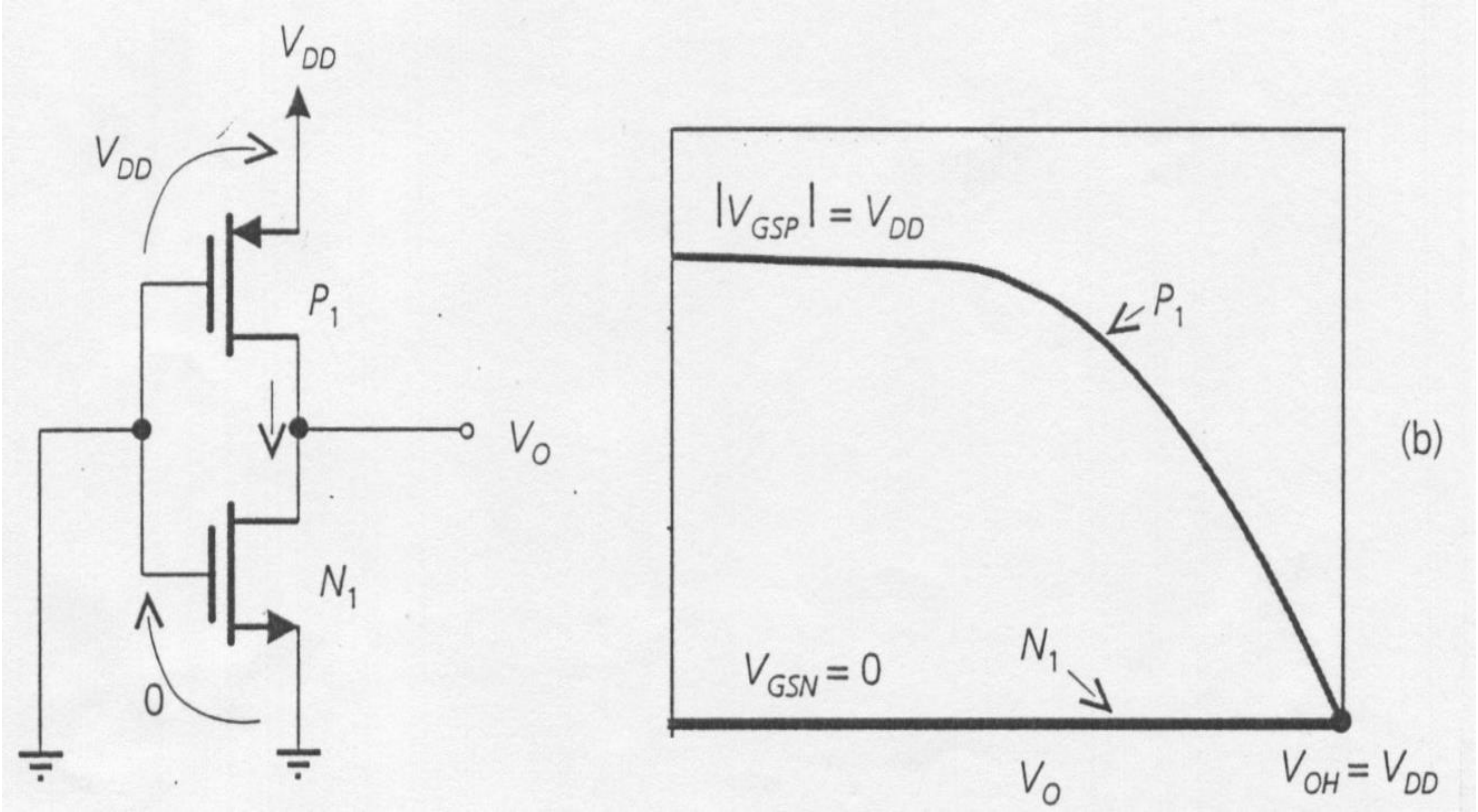


$$V_{GSN} = V_I$$
$$|V_{GSP}| = V_{DD} - V_I$$

$V_I = V_{DD}$



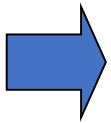
$V_I = 0$



Caratteristica di Trasferimento

Ipotesi:

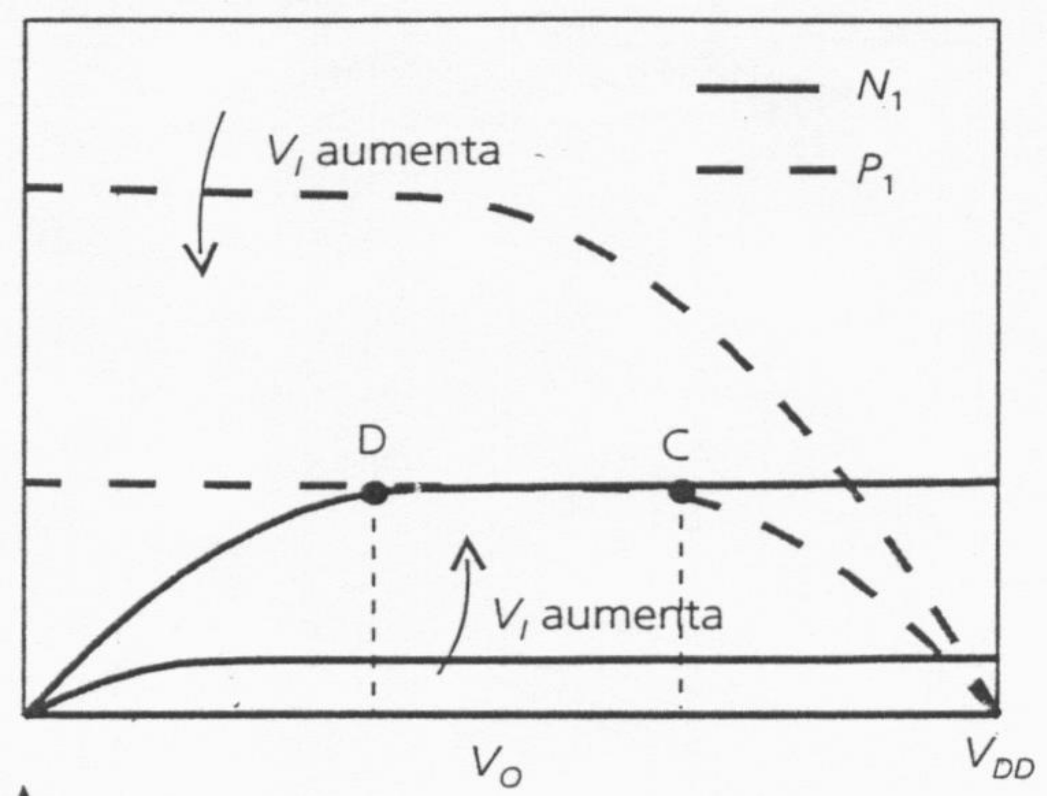
$$K_N = K_P = K$$



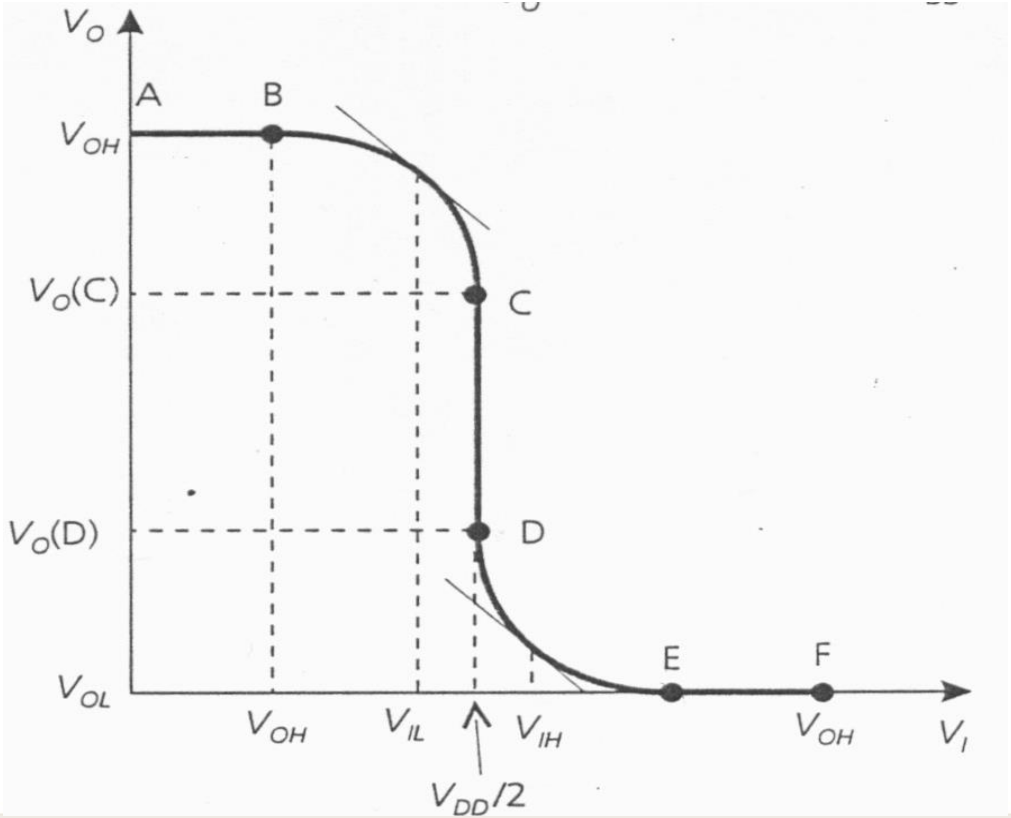
$$\left.\frac{W}{L}\right|_P = 2.5 \left.\frac{W}{L}\right|_N$$

$$V_{TN} = |V_{TP}| = V_T$$

Caratteristica di Trasferimento



Caratteristica di Trasferimento



Caratteristica di Trasferimento

- A-B : NMOS interdetto, PMOS in r. triodo
- B-C : NMOS r. pinch-off, PMOS in r. triodo
  - Qui cade V_{IL}
- C-D : NMOS e PMOS in r. pinch-off
  - Qui abbiamo V_{SL}
- D-E : NMOS in r. triodo, PMOS in pinch-off
  - Qui cade V_{IH}
- E-F : NMOS in r. triodo, PMOS interdetto

Caratteristica di Trasferimento

$$V_{SL} = \frac{V_{DD}}{2}$$

- Calcolo di $V_O(C)$ $\qquad V_I = \frac{V_{DD}}{2}$

$$|V_{DSP}| = |V_{GSP}| - |V_{TP}|$$

$$V_{DD} - V_O(C) = V_{DD} - V_I - V_T$$

$$\Rightarrow \qquad V_O(C) = \frac{V_{DD}}{2} + V_T$$

Caratteristica di Trasferimento

- Calcolo di $V_O(D)$

$$V_I = \frac{V_{DD}}{2}$$

$$V_{DSN} = V_{GSN} - V_T$$

$$\Rightarrow \quad V_O(D) = \frac{V_{DD}}{2} - V_T$$

Calcolo di V_{IH}

- NMOS in r. triodo, PMOS in pinch-off

$$I_{DN} = I_{DP}$$

$$2\,(V_I - V_T)\,V_O - {V_O}^2 = (V_{DD} - V_I - V_T)^2 \quad (*)$$

- Derivando:

$$2\,(V_I - V_T)\,\frac{dV_O}{dV_I} + 2\,V_O - 2\,V_O\frac{dV_O}{dV_I} = -2\,(V_{DD} - V_I - V_T)$$

Calcolo di V_{IH}

- Imponiamo:

$$\frac{dV_O}{dV_I} = -1$$

$$-2\ (V_{IH} - V_T)\ + 4\ V_O = \ -2\ (V_{DD} - V_{IH} - V_T)$$

$$V_{IH} = \ V_O + \frac{V_{DD}}{2}$$

- E sostituendo nella (*):

$$V_O = \ \frac{1}{4}\left(\frac{V_{DD}}{2} - V_T\right) \quad \Rightarrow \quad V_{IH} = \ \frac{1}{4}\left(\frac{5\ V_{DD}}{2} - V_T\right)$$

Calcolo di V_{IL}

- Per la simmetria:

$$V_{IH} - \frac{V_{DD}}{2} = \frac{V_{DD}}{2} - V_{IL}$$

$$V_{IL} = \frac{1}{4}\left(\frac{3\ V_{DD}}{2} + V_T\right)$$

Riassumendo

$$V_{OH} = V_{DD}$$

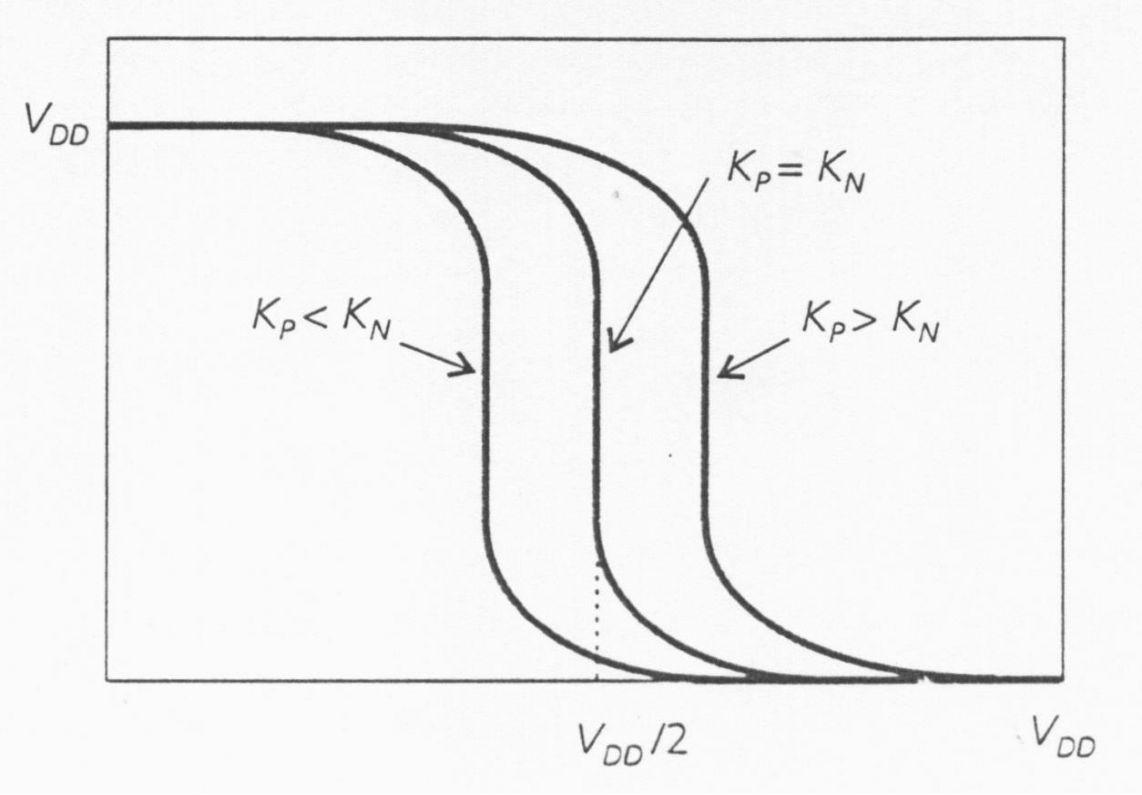
$$V_{OL} = 0$$

$$V_{IH} = \frac{1}{4}\left(\frac{5\ V_{DD}}{2} - V_T\right)$$

$$V_{IL} = \frac{1}{4}\left(\frac{3\ V_{DD}}{2} + V_T\right)$$

$$NM_H = NM_L = \frac{3}{8}\ V_{DD} + \frac{1}{4}V_T$$

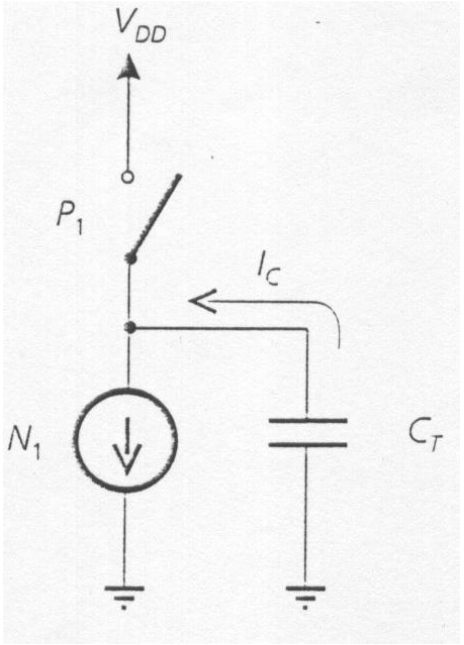
In assenza di simmetria

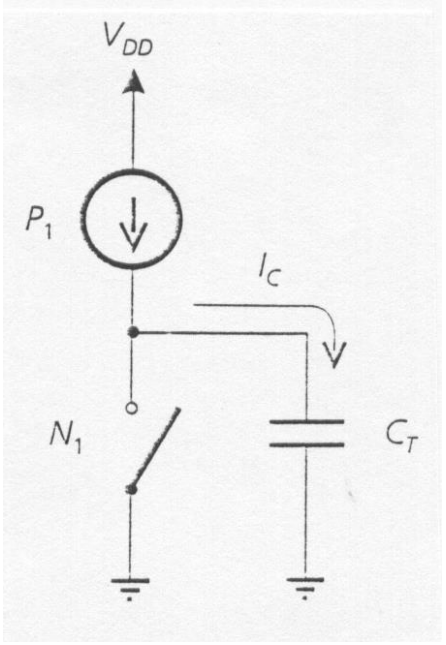


Capacità totale di gate del carico

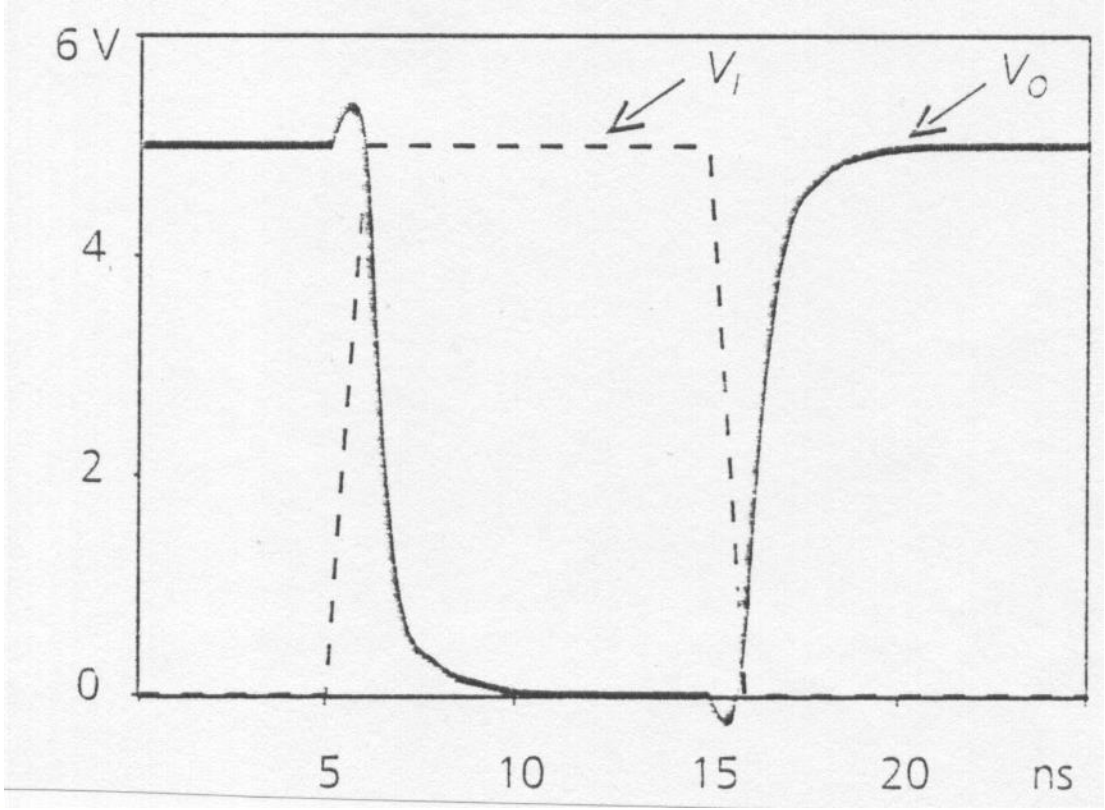
$$
\begin{aligned}
C_{GT} &= C_{GN} + C_{GP} \\
&= C_{OX}(W_N L_N + W_P L_P) \\
&= C_{OX}(W_N L_N + 2.5\ W_N L_N) \\
&= 3.5\ C_{GN}
\end{aligned}
$$

Comportamento dinamico

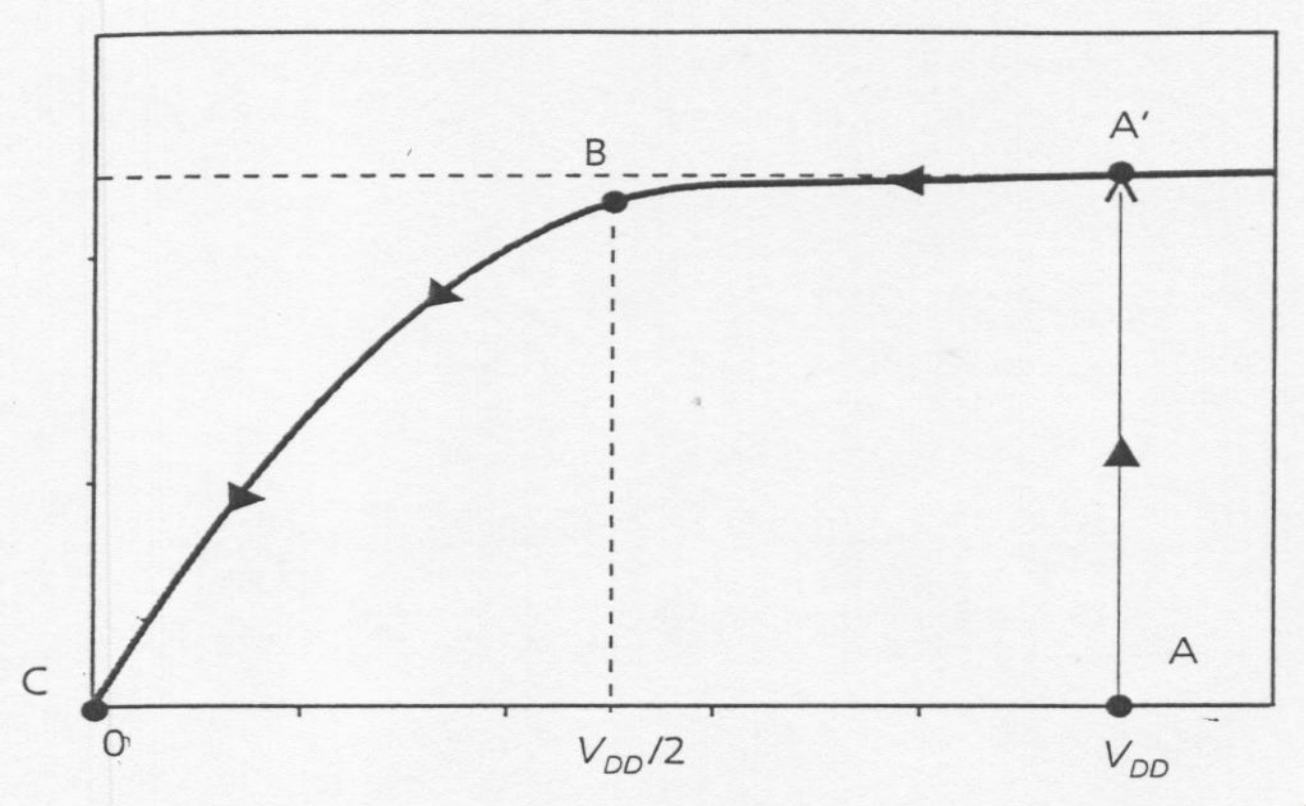




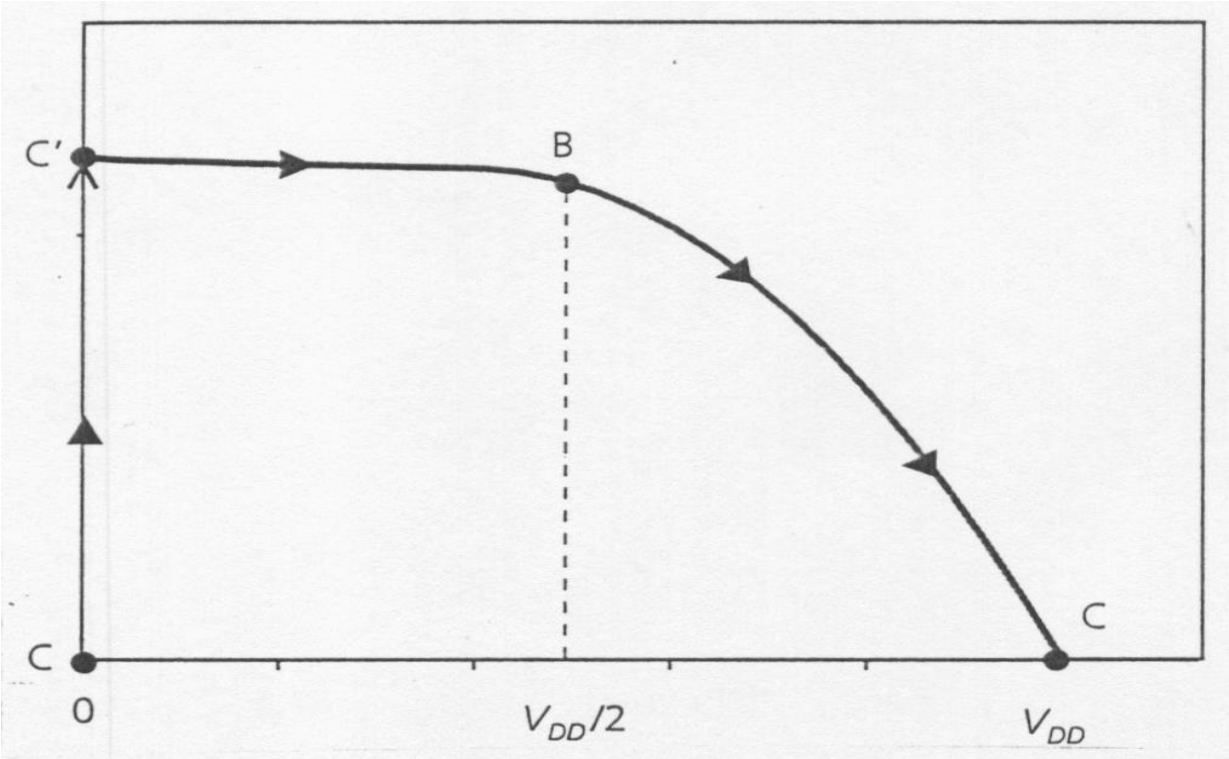
Comportamento dinamico



Passaggio da Alto a Basso

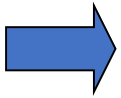


Passaggio da Basso a Alto



Tempi di propagazione

- A’ – B : $I_N = K_N(V_{DD} - V_{TN})^2$
- C’ – B : $I_P = K_P(V_{DD} - |V_{TP}|)^2$
- Ipotesi: $K_N = K_P \ , \quad V_{TN} = |V_{TP}|$



$$t_P = t_{PHL} = t_{PLH} \cong \frac{C_T(V_{OH} - V_{OL})}{2\ I_H} = \frac{C_T V_{DD}}{2\ K_N(V_{DD} - V_T)^2}$$

Tempi di propagazione

$$t_P = \frac{3.5\ C_{GN} V_{DD}}{2\ K_N (V_{DD} - V_T)^2}$$

$$t_P \propto \frac{C_{GN}}{K_N} = \frac{C_{OX} W_N L_N}{k_N {W_N}/{L_N}} \propto L_N^2$$

Tempi di propagazione

- E se …

$$\left.\frac{W}{L}\right|_N = \left.\frac{W}{L}\right|_P$$

- Capacità di carico:

$$C_T = 2\ C_{GN}$$

$$t_{PHL} = \frac{2\ C_{GN} V_{DD}}{2\ K_N (V_{DD} - V_T)^2}$$

$$t_{PLH} = \frac{2\ C_{GN} V_{DD}}{2\ K_P (V_{DD} - V_T)^2}$$

Tempi di propagazione

$$K_P = K_N/2.5$$

$$t_P = \frac{t_{PHL} + t_{PLH}}{2} = \frac{C_{GN} V_{DD}}{K_N (V_{DD} - V_T)^2} \frac{1 + 2.5}{2}$$

$$= \frac{3.5\ C_{GN} V_{DD}}{2\ K_N (V_{DD} - V_T)^2}$$

Potenza dissipata

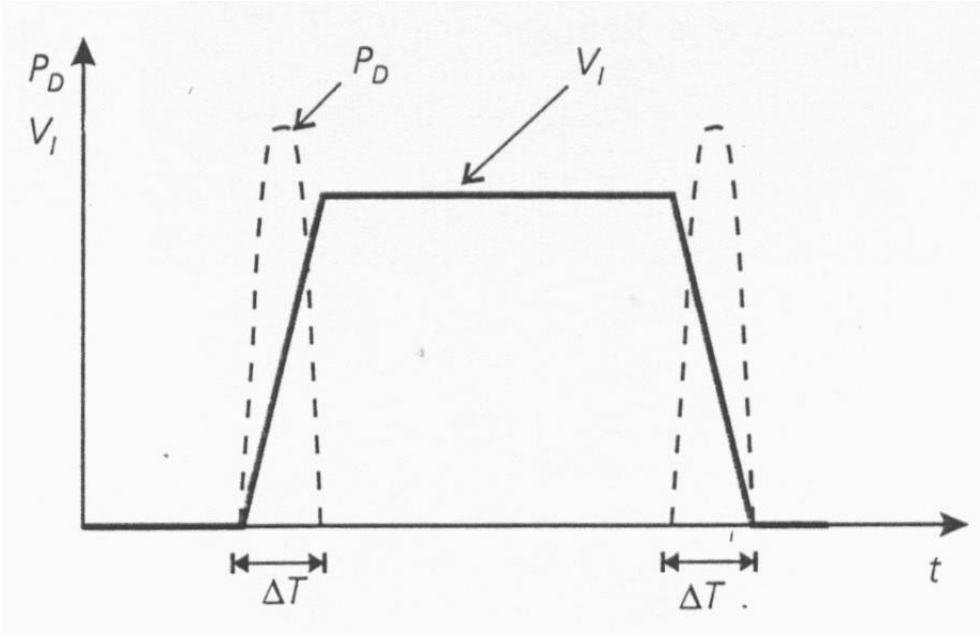
- Sola potenza dissipata dinamica:

$$P_{Dd} = \frac{1}{T}\left[\int_{\Delta T_{HL}} V^+ \; i \; dt + \int_{\Delta T_{LH}} V^+ \; i \; dt\right]$$

- Due contributi:
  - Contributo dovuto alla corrente che circola nei due MOS nelle fasi di transizione, P_D'
  - Contributo dovuto alla corrente di carica della capacità di uscita, P_D''
- Ipotesi:
  - Invertitore simmetrico $\Delta T_{HL} = \Delta T_{LH} = \Delta T$

Potenza dissipata

$$P_{Dd} = \frac{2}{T}\int_{\Delta T} V^{+}\ i(t)\ dt$$



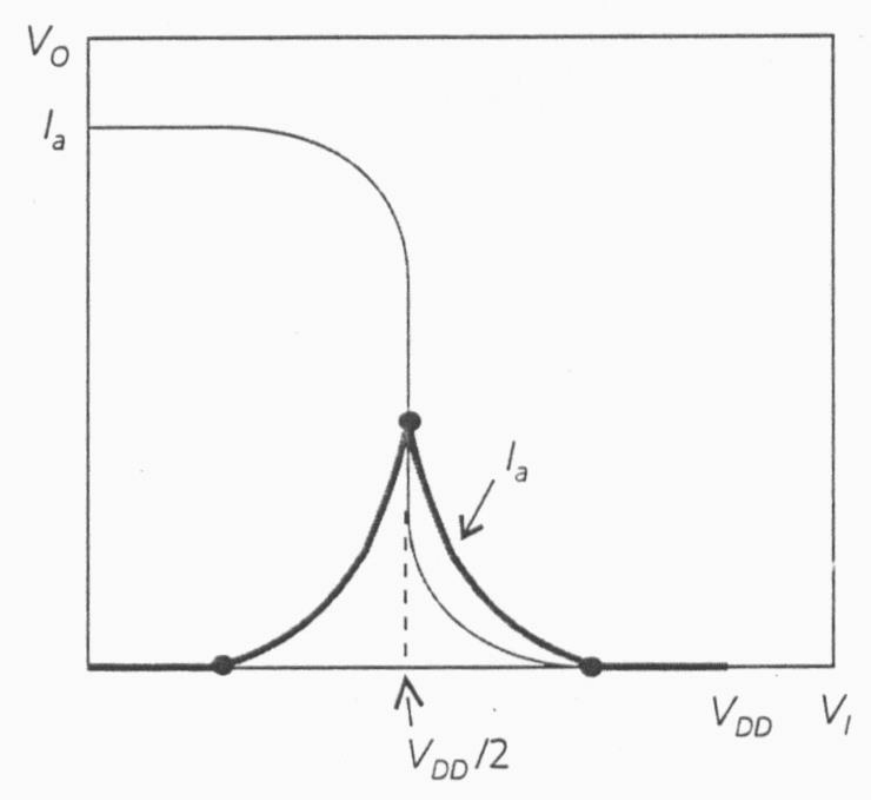
Calcolo di PD’

- Ipotesi: Andamento lineare nel tempo di V_I durante le transizioni:

$$V_I = \alpha\ t \quad \Rightarrow \quad dt = \frac{dV_I}{\alpha}$$

$$V_T < V_I < \frac{V_{DD}}{2}: \qquad I_D = K_N(V_I - V_T)^2$$

Calcolo di PD’



Calcolo di PD’

$$P_D{}' = \frac{2}{T}\int_0^{\Delta T} V_{DD}\, I_D(t)\; dt =$$

$$= \frac{4}{\alpha\; T}\int_{V_T}^{V_{DD}/2} V_{DD}\, I_D(V_I)\; dV_I =$$

$$= \frac{4\; V_{DD}\; K_N}{3\alpha\; T}\left(\frac{V_{DD}}{2} - V_T\right)^3$$

$$\alpha = \frac{V_{DD}}{2\; t_p}$$

Potenza dissipata

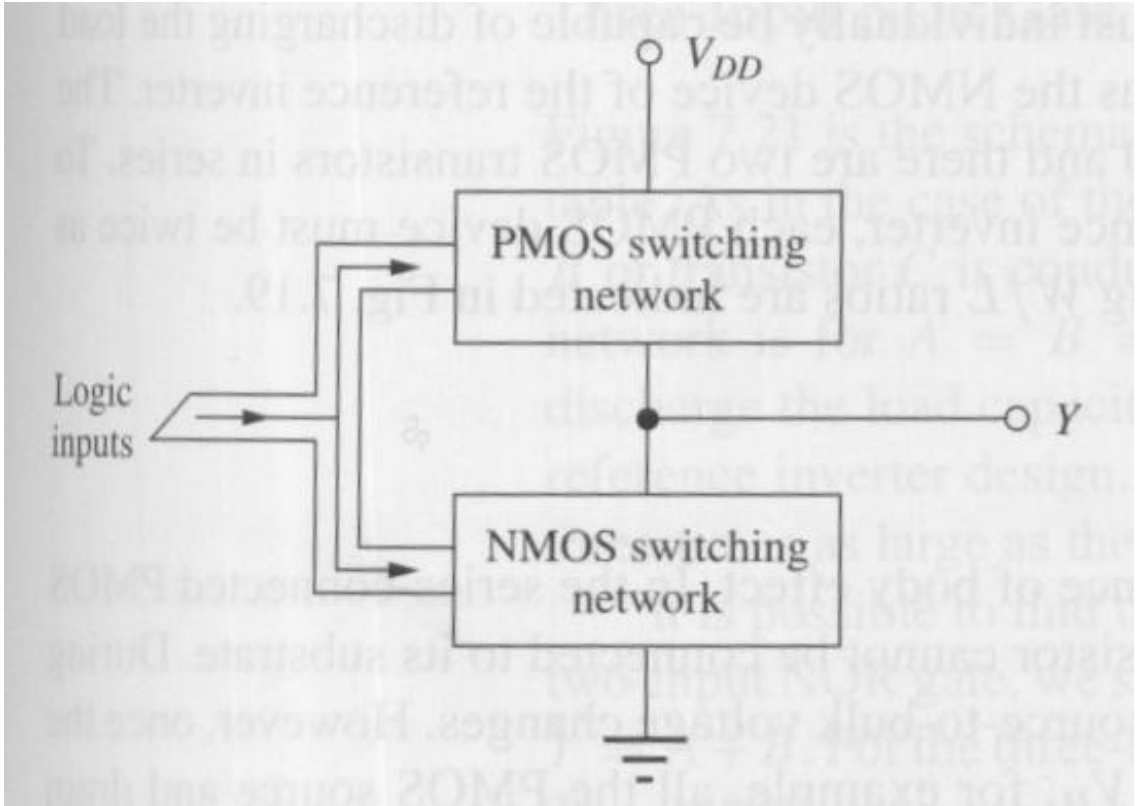
$$P_D'' = \frac{C_T \ {V_{DD}}^2}{T}$$

$$\frac{P_D'}{P_D''} = \frac{8 \ t_p K_N}{3 \ C_T \ {V_{DD}}^2} \left(\frac{V_{DD}}{2} - V_T \right)^3$$

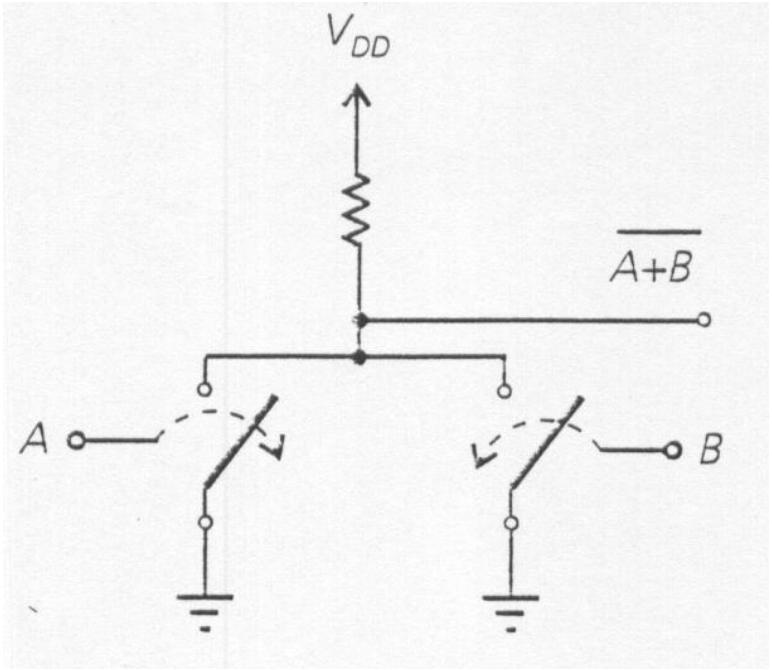
$$\frac{P_D'}{P_D''} \propto \frac{t_p K_N}{C_T} \quad \Longrightarrow \quad \text{Invariante progettuale!}$$

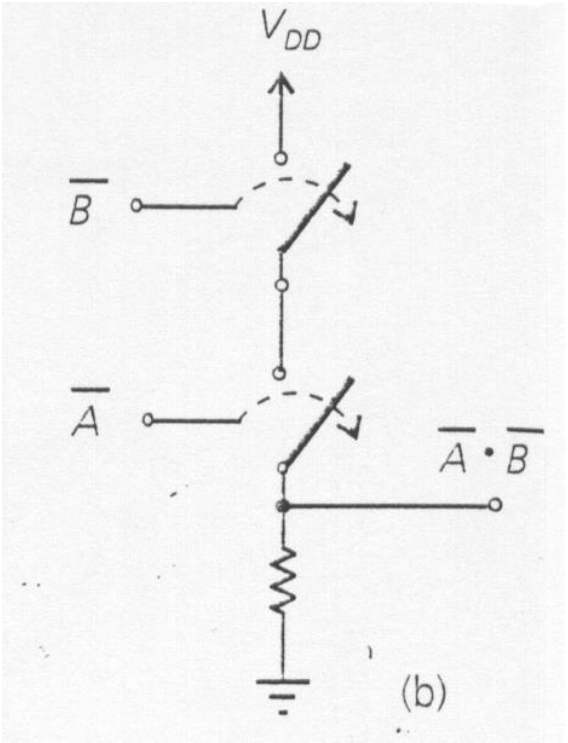
In genere: $\frac{P_D'}{P_D''} < 0.1$

Porte logiche CMOS



Porte logiche CMOS

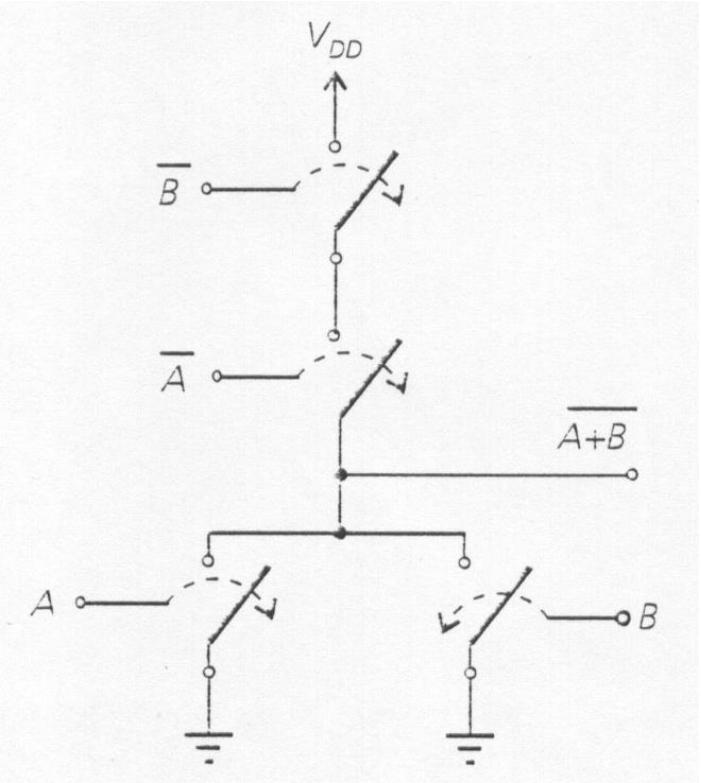




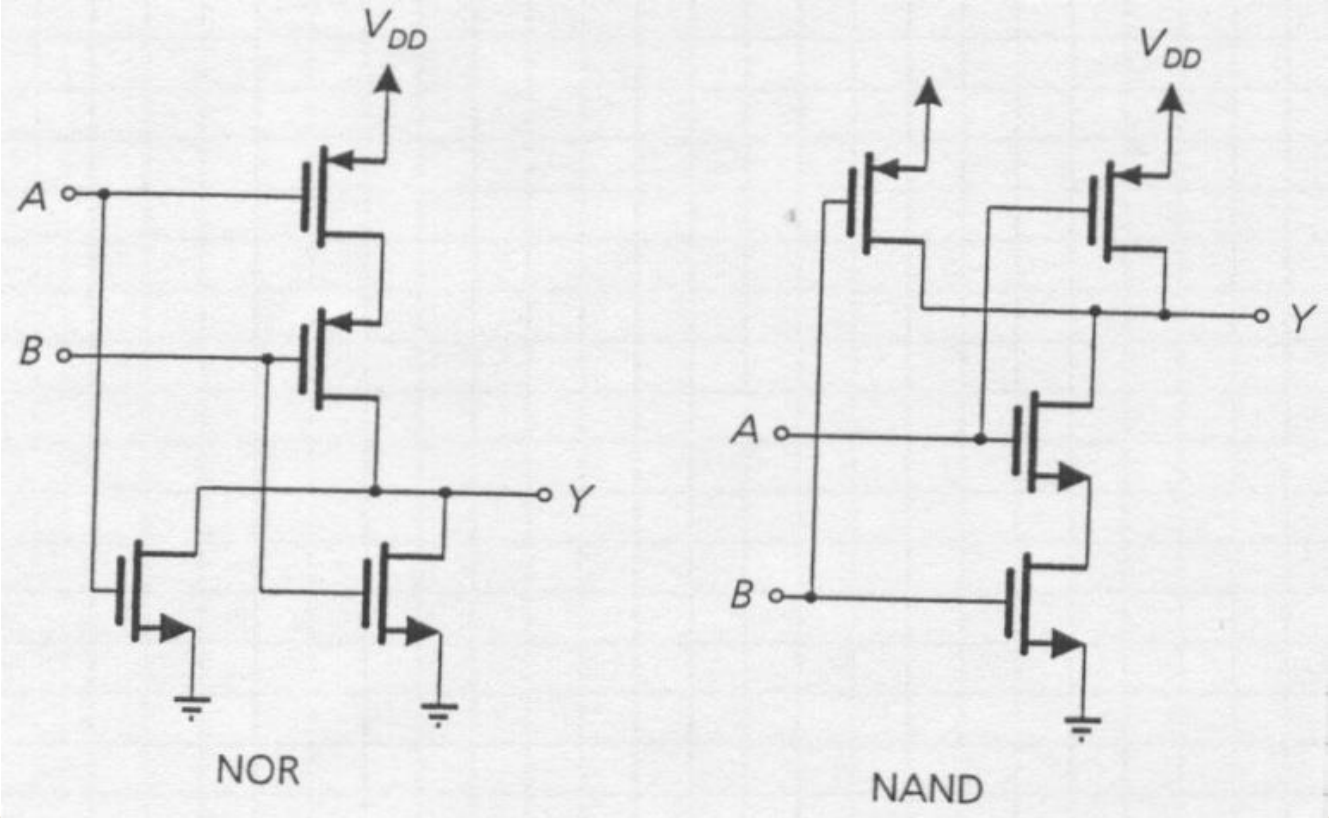
NOR

Porte logiche CMOS

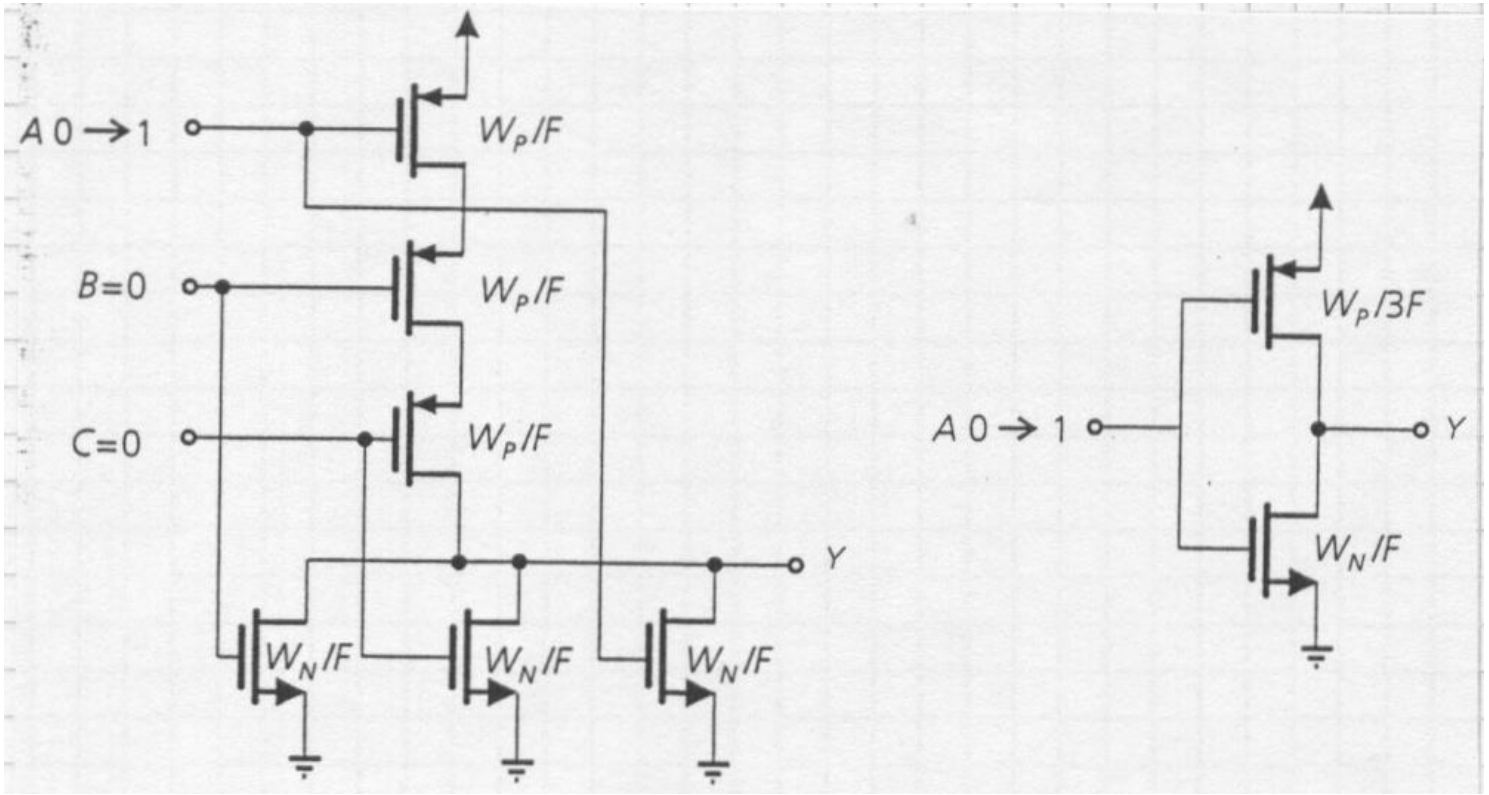
NOR



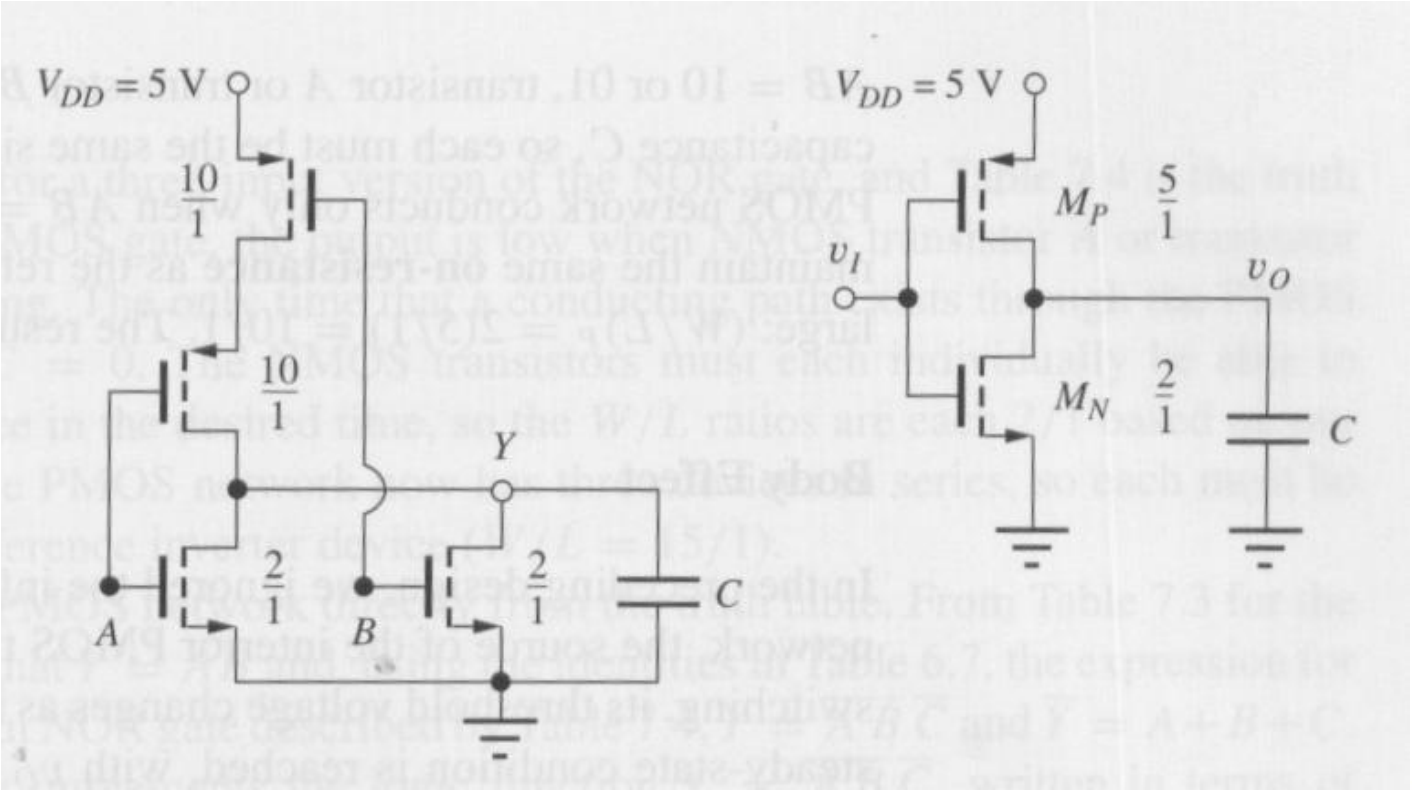
Porte logiche CMOS



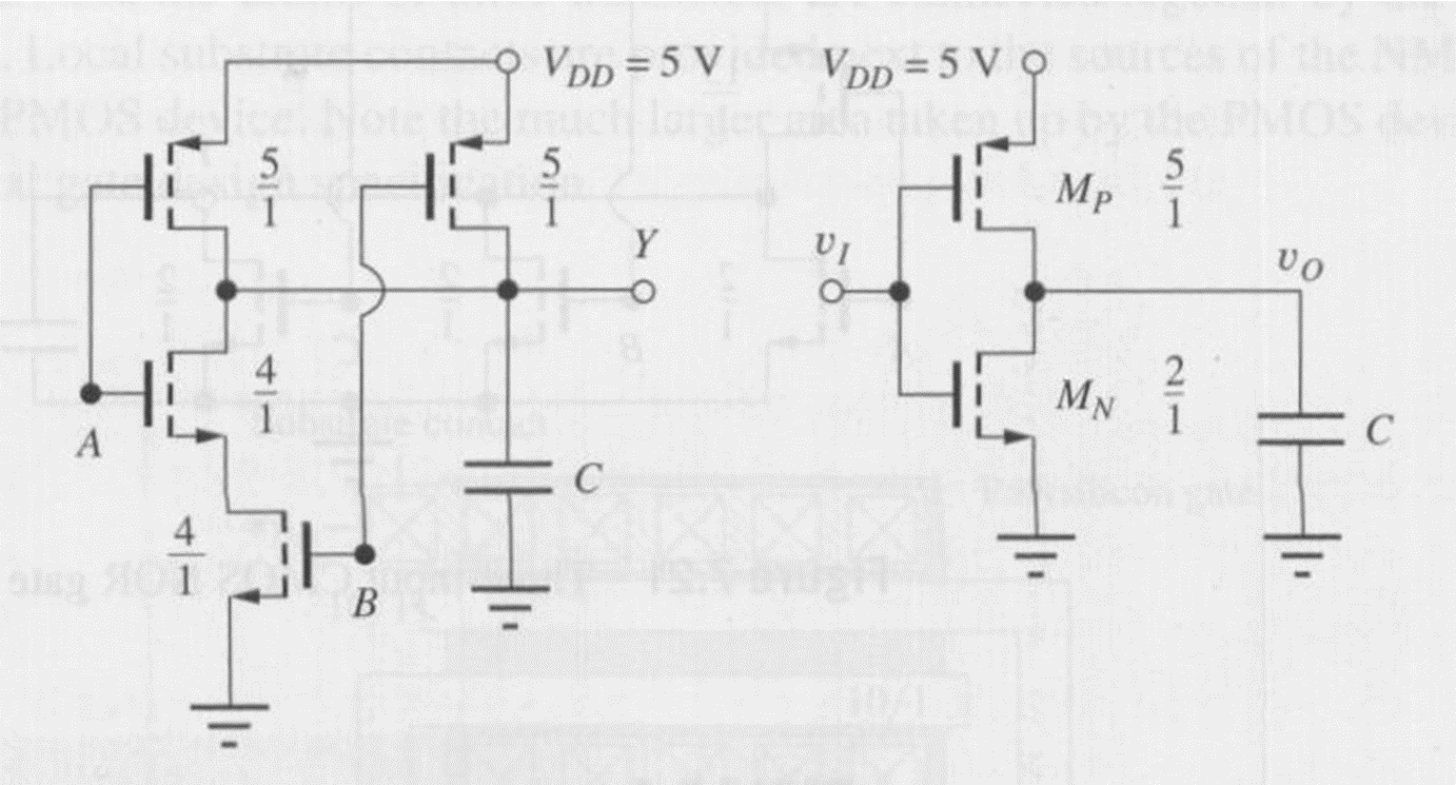
Invertitore equivalente



Progetto porta NOR



Progetto porta NAND



Contronto aree NOR – NAND

- Progetto a parità di prestazioni con un invertitore avente $K_P = K_N$ e fattori di forma $\frac{W_P}{F} = \frac{2.5\,W_N}{F}$.

- **NOR**: $t_{PLH} = t_{PHL}(w.c.)$ ⟹ $K_{Peq} = K_N$

  $W_N(NOR) = W_N$ $\qquad$ $W_P(NOR) = 2.5\ N\ W_N$

- **NAND:** $t_{PLH}(w.c.) = t_{PHL}$ ⟹ $K_P = K_{Neq}$

  $W_N(NAND) = N\,W_N$ $\qquad$ $W_P(NOR) = 2.5\ W_N$

Contronto aree NOR – NAND

$$Area\ (NOR) = N\ W_N F + N\ (2.5\ W_N N)\ F$$
$$= N\ (1 + 2.5\ N)\ W_N F$$

$$Area\ (NAND) = N\ (W_N\ N)\ F + N\ (2.5\ W_N)\ F$$
$$= N\ (N + 2.5)\ W_N F$$

Progetto ad area minima

- Certe volte si considera area per NMOS e PMOS fissata pari all'invertitore di base.
  - NMOS: $W/L = 3\lambda/2\lambda$
  - PMOS: $W/L = 2.5 \cdot 3\lambda/2\lambda$

- Le porte NAND e NOR avranno uguale area ma tempi di propagazione t_{PHL},t_{PLH} diversi.
- Tempi di propagazione peggiore:
  - determinato dalla attivazione del ramo con i dispositivi in serie.

Progetto ad area minima

$$t_{PHL}(NAND) \propto \frac{C_T}{K_{N\ eq}}$$

$$t_{PLH}(NOR) \propto \frac{C_T}{K_{P\ eq}}$$

Con: $\left.\frac{W}{L}\right|_P = 2.5 \left.\frac{W}{L}\right|_N$ ⇒ $K_{P\ eq} = K_{N\ eq}$

$$t_{PHL}(NAND) = t_{PLH}(NOR)$$

FAN-IN: caso progetto ad area minima

Ritardo dell'invertitore:

$$t_{PHL} = t_{PLH} \cong \frac{C_T \ V_{DD}}{2 \ K_N (V_{DD} - V_T)^2} = t_{P_0}$$

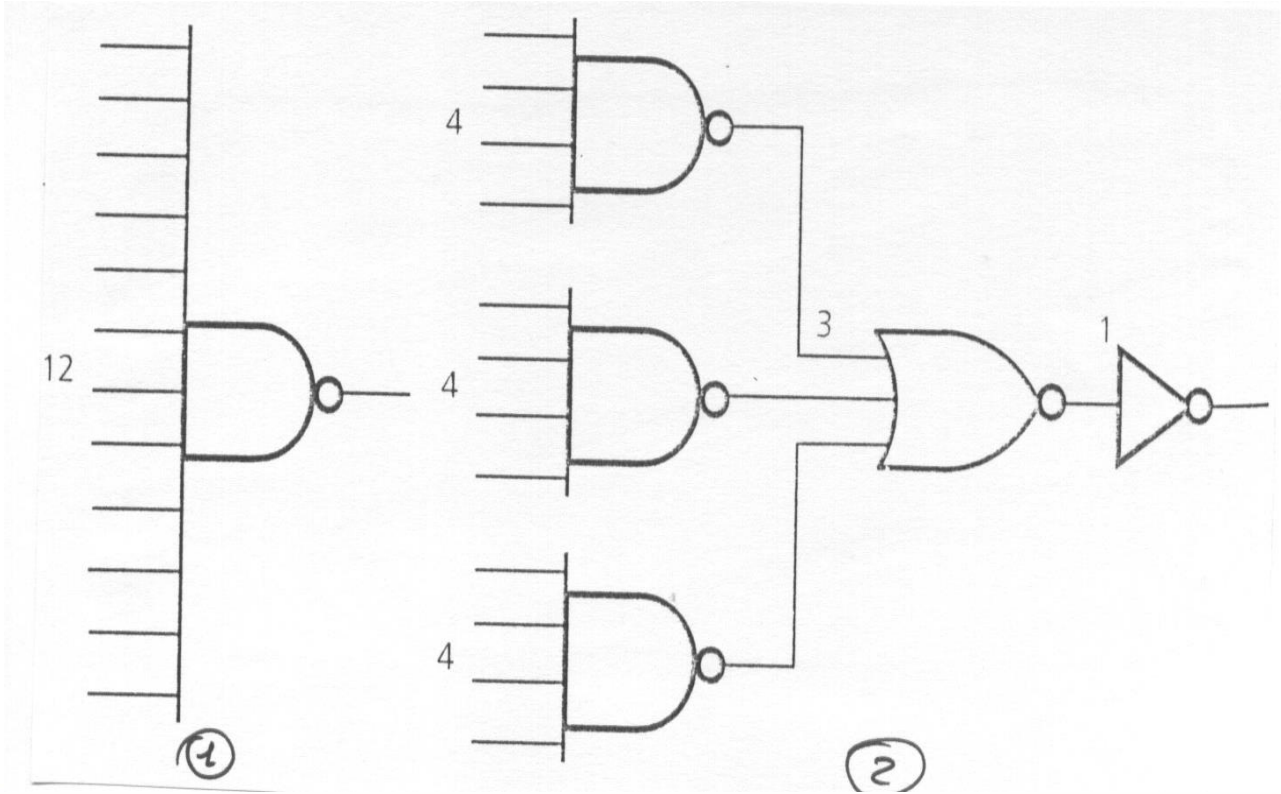
Ritardo peggiore nella porta NOR:

$$t_{PLH} \cong \frac{N \ C_T \ V_{DD}}{2 \ K_N (V_{DD} - V_T)^2} = N \ t_{P_0}$$

Ritardo peggiore nella porta NAND:

$$t_{PHL} \cong \frac{N \ C_T \ V_{DD}}{2 \ K_N (V_{DD} - V_T)^2} = N \ t_{P_0}$$

Per elevati FAN-IN

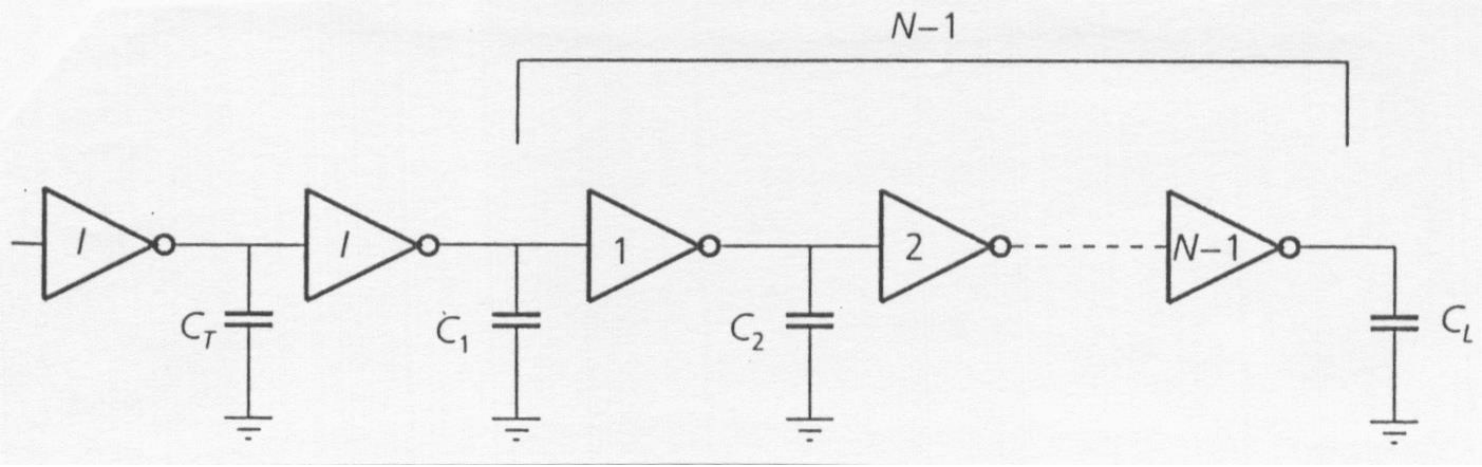


FAN-OUT

$$t_P \cong \frac{N\ 3.5\ C_G\ V_{DD}}{2\ K_N(V_{DD} - V_T)^2} = N\ t_{P_0}$$

- 5-6 se vogliamo limitare il peggioramento del ritardo entro un ordine di grandezza

Progetto porta NOR



$$G = \frac{K_{J+1}}{K_J} \quad \Rightarrow \quad G = \frac{C_{J+1}}{C_J}$$

$$\frac{C_L}{C_T} = \frac{C_L}{C_{N-1}} \cdot \frac{C_{N-1}}{C_{N-2}} \cdot \ldots \cdot \frac{C_1}{C_T} = G^N$$

Stadi separatori di uscita

$$N = \frac{1}{\ln G} \ln\left(\frac{C_L}{C_T}\right)$$

$$t_{P_0} \propto \frac{C_1}{K} = G\,\frac{C_T}{K} \quad \Rightarrow \quad t_{P_0} = G\ t_P$$

$$t_{P_1} \propto \frac{C_2}{K_1} = \frac{G^2\ C_T}{G\ K} \quad \Rightarrow \quad t_{P_1} = G\ t_P$$

$$t_{P_{N-1}} \propto \frac{C_L}{K_{N-1}} = \frac{G^N\ C_T}{G^{N-1}\ K} \quad \Rightarrow \quad t_{P_{N-1}} = G\ t_P$$

Stadi separatori di uscita

$$t_{P_{TOT}} = \sum_{i=1}^{N-1} t_{P_i} = N \; G \; t_P$$

$$t_{P_{TOT}} = \frac{1}{\ln G} \ln\left(\frac{C_L}{C_T}\right) \; G \; t_P$$

$$\frac{d \; t_{P_{TOT}}}{d \; G} = 0 \quad \Rightarrow \quad \ln G_{opt} = 1$$

$$G_{opt} = e \cong 2.7$$

Stadi separatori di uscita

$$N_{opt} = \ln\left(\frac{C_L}{C_T}\right)$$

$$t_{P_{TOTopt}} = 2.7 \ \ln\left(\frac{C_L}{C_T}\right) \ t_P$$

Da confrontare con:

$$t_P{}' = \frac{C_L}{C_T} \ t_P$$

Stadi separatori di uscita: esempio

$$C_L = 10\ pF$$

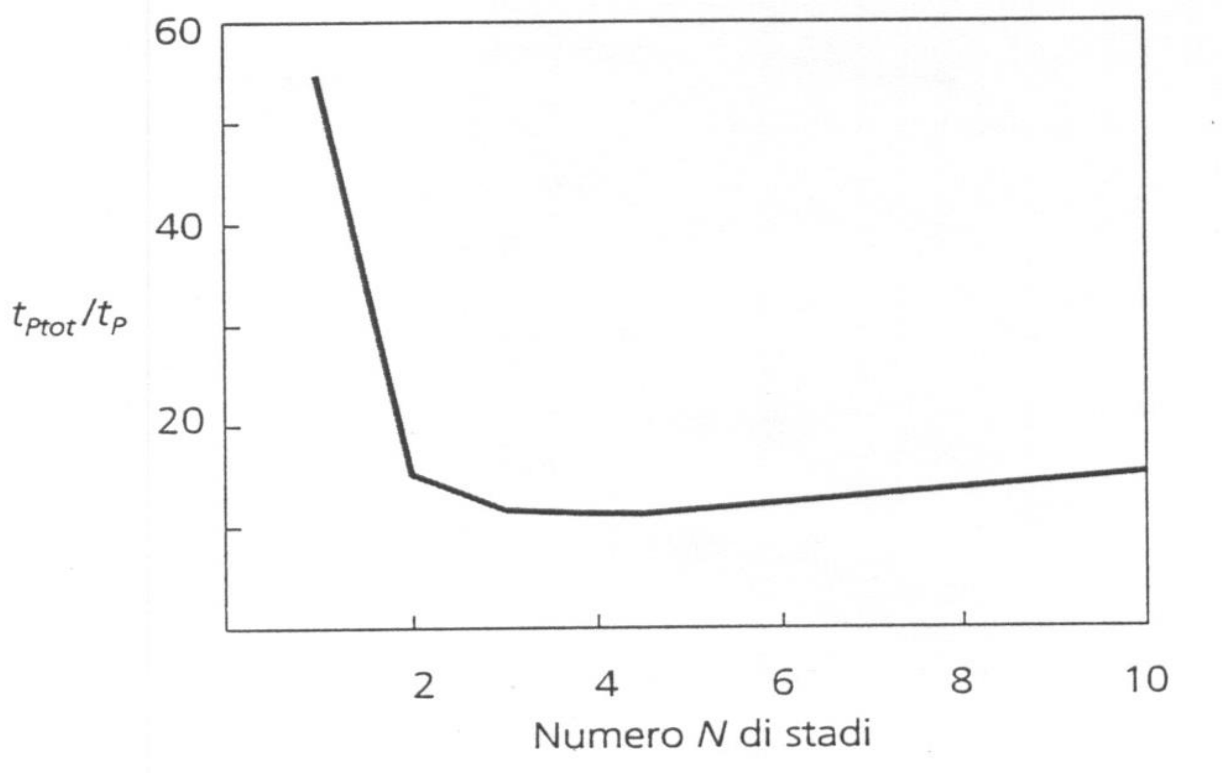
$$C_T = 188\ fF$$

$$\ln\left(\frac{C_L}{C_T}\right) = \ln\left(\frac{10 \cdot 10^{-12}}{188 \cdot 10^{-15}}\right) = \ln 5\,3{,}1 \cong 4 = N$$

$$t_{P_{TOTopt}} = 11 \cdot\ t_P$$

$$t_P{}' = 53 \cdot\ t_P$$

Stadi separatori di uscita: esempio



Riduzione di scala

$$t_P = \frac{3.5\ C_{GN} V_{DD}}{2\ K_N (V_{DD} - V_T)^2}$$

$$P_D = 3.5 f\ C_G\ {V_{DD}}^2$$

$$f = \frac{1}{T}$$

$$P \cdot D = 3.5 \frac{t_P}{T}\ C_G\ {V_{DD}}^2$$

$$C_G = W\ L\ \varepsilon_{ox}/t_{ox}$$

$$K_N = \frac{1}{2} \mu_N \frac{\varepsilon_{ox}}{t_{ox}} \frac{W}{L}$$

Riduzione di scala

Tabella 5.3 Regole di scala per circuiti CMOS.

Grandezza	Scalamento completo
W, L, t_{OX}	$1/x$
V_{DD}, V_T, N_{SI}	$1/x$
C_G	$1/x$
K	x
Ritardo di propagazione t_P	$1/x$
Potenza dissipata P_D	$(1/x)^2$
Prodotto Ritardo-Potenza $P \cdot D$	$(1/x)^3$

Vedere:

- Paolo Spirito, “Elettronica Digitale”, Ed. McGraw-Hill
  - Cap. 5.1-5.3
  - Cap. 5.5-5.9
  - Cap. 5.11