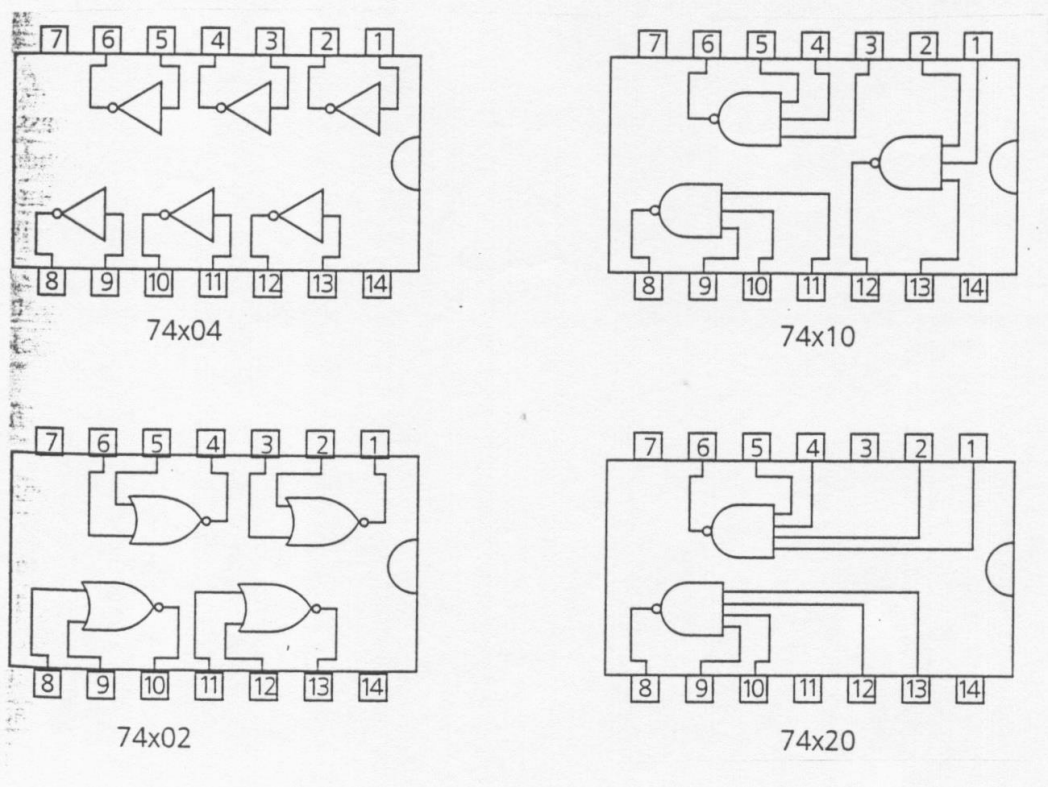
UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

Circuiti di interconnessione e di I/O

A.Carini – Elettronica digitale

Circuiti logici standard

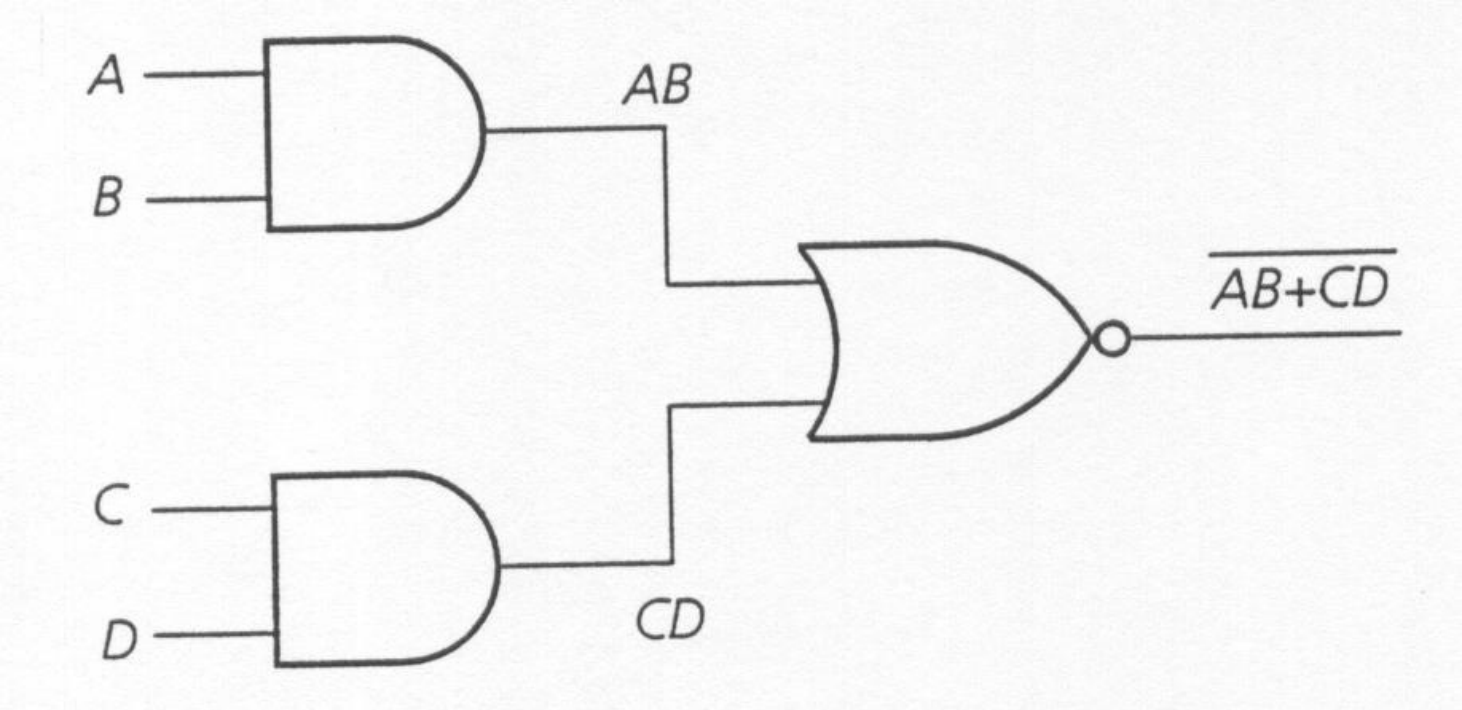


Caratteristiche Porte Standard

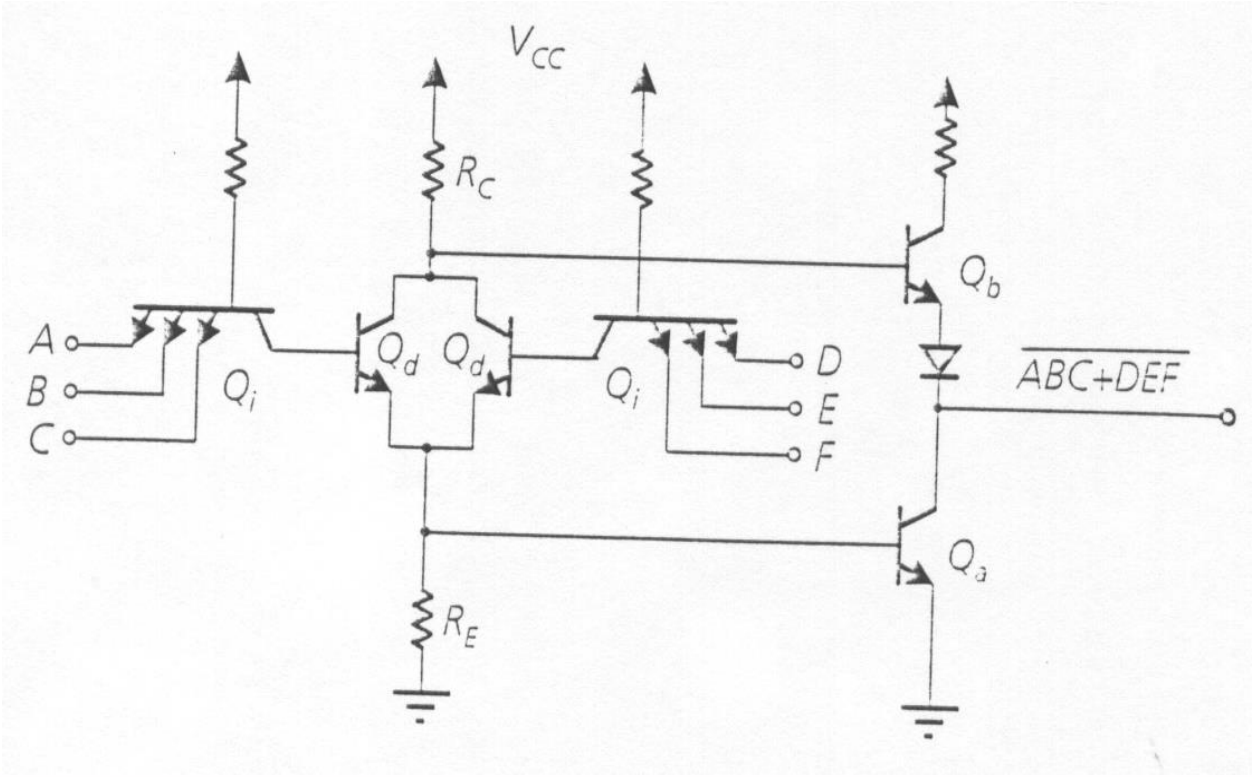
Tabella 9.1 Caratteristiche elettriche di porte standard CMOS, TTL, ECL.

Famiglia logica		CMOS-AC		TTL-ALS	ECL 10 K	ECL 100 K
t_P	(ns)	4.75		4	2	0.7
P_D/porta	(mW)	Statica:	0.005	1.2	(senza carico)	(senza carico)
		Totale:			26	40
		f = 0.1 MHz	0.08			
		f = 1 MHz	0.75			
		f = 10 MHz	7.5			
$t_P \cdot P_D$	(pJ)	f = 0.1 MHz	0.4	5	52	28
		f = 1 MHz	3.6			
		f = 10 MHz	36			

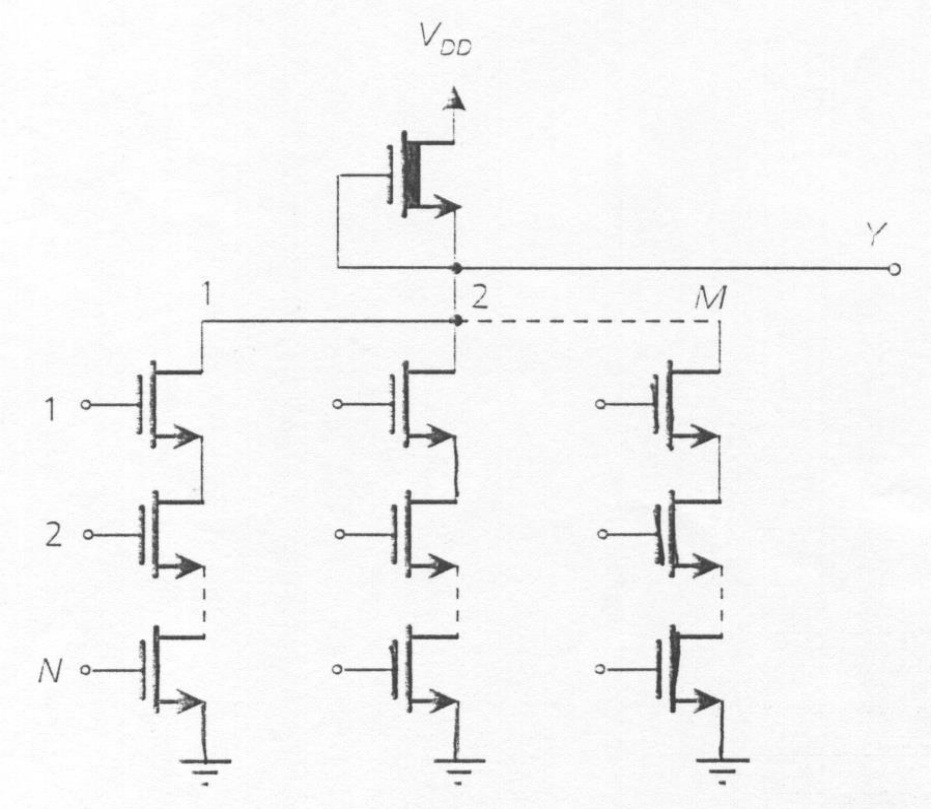
Porta AOI



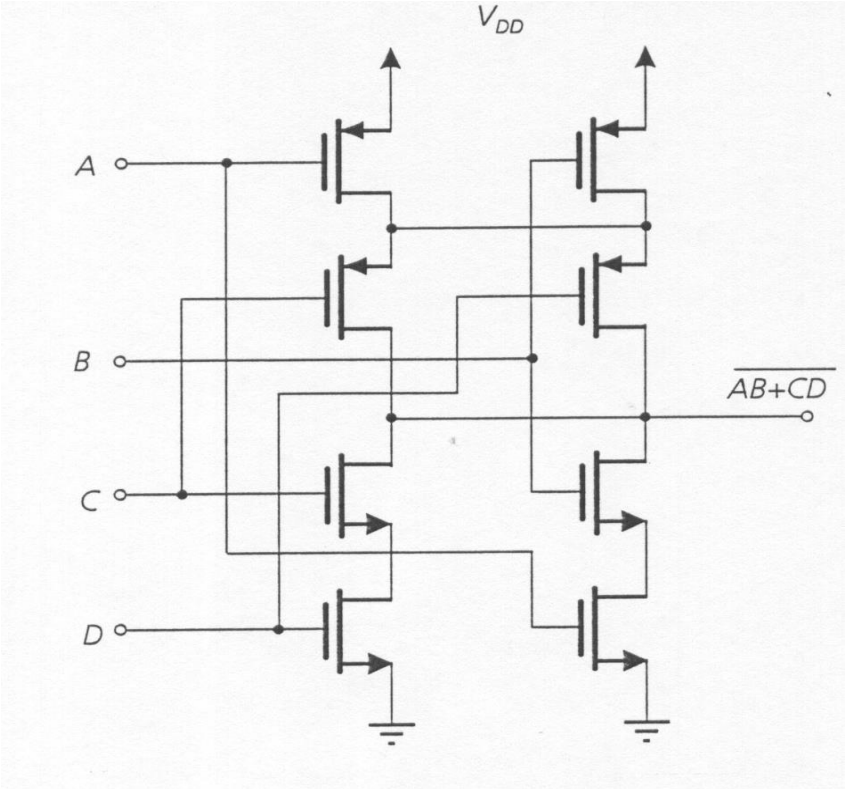
Porta AOI



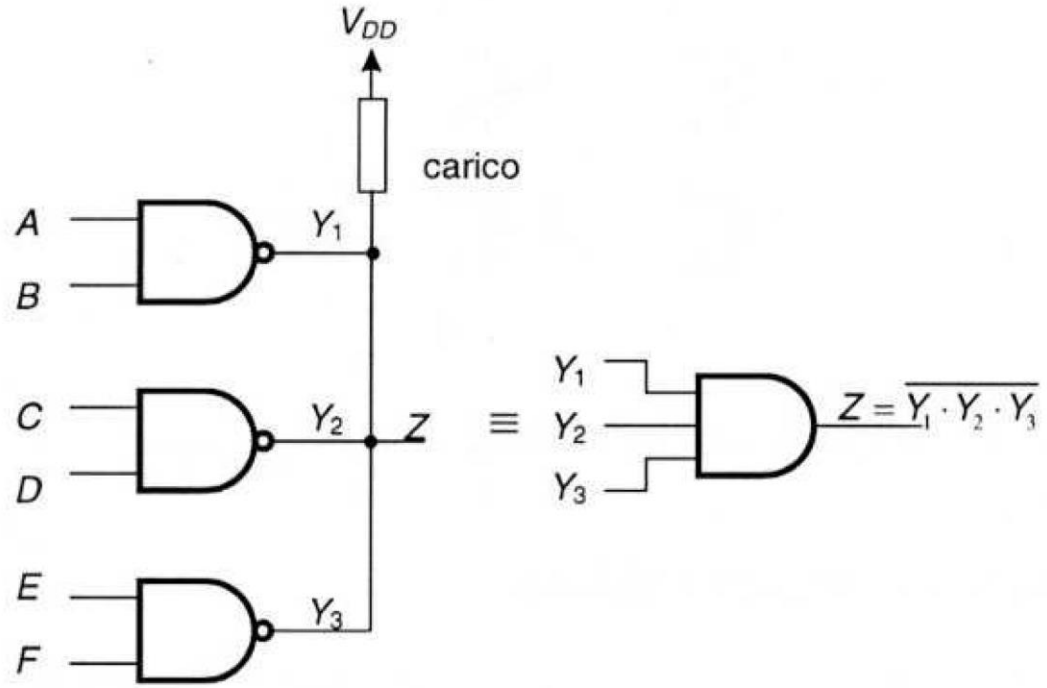
Porta AOI



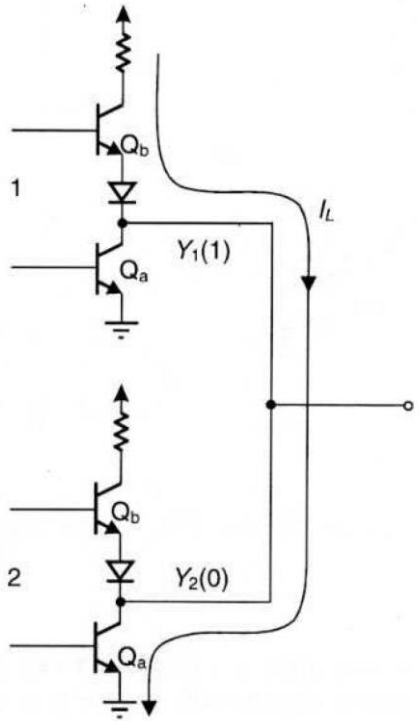
Porta AOI



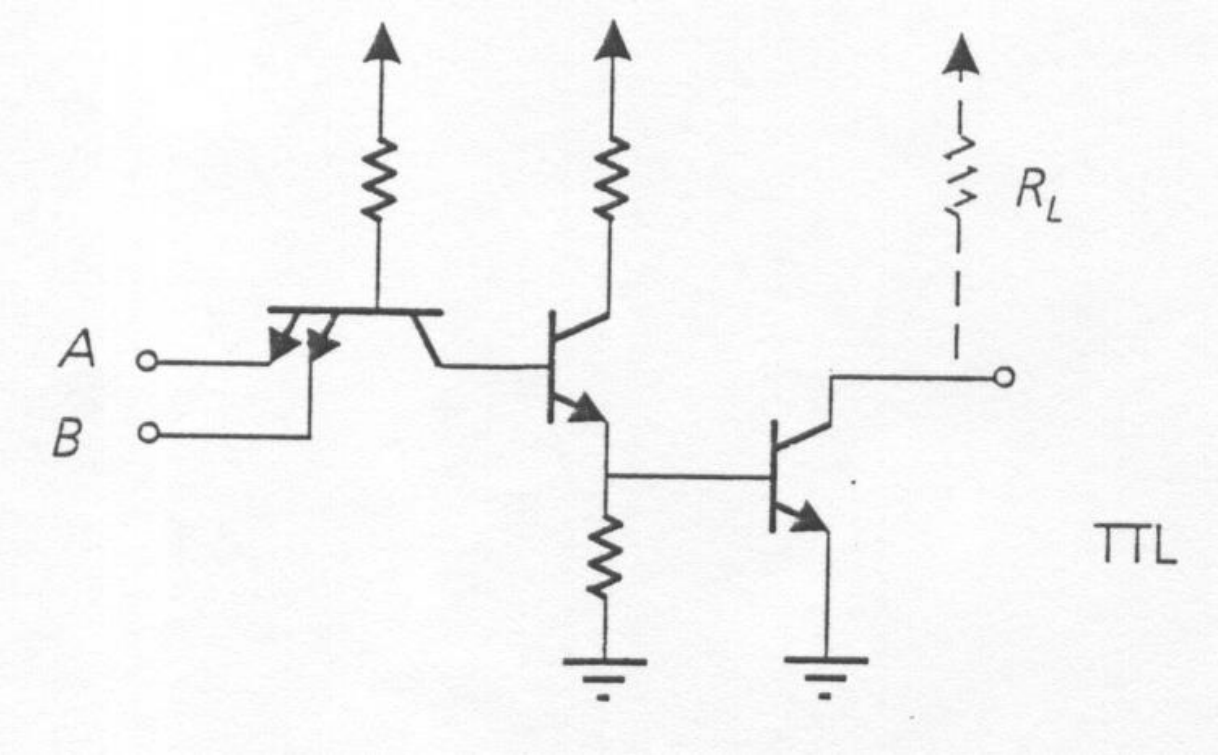
Porte in logica cablata



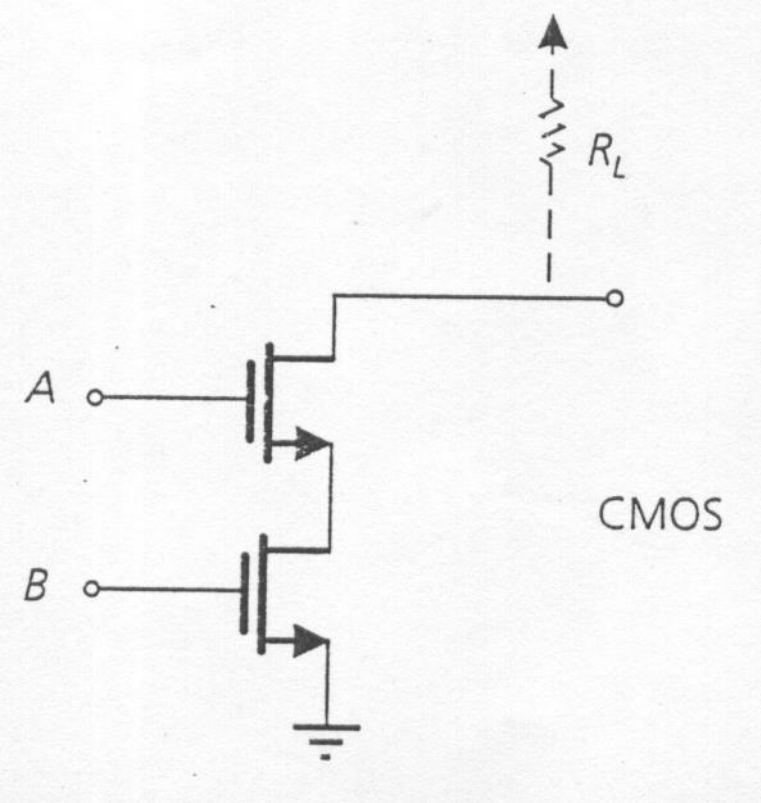
Porte in logica cablata

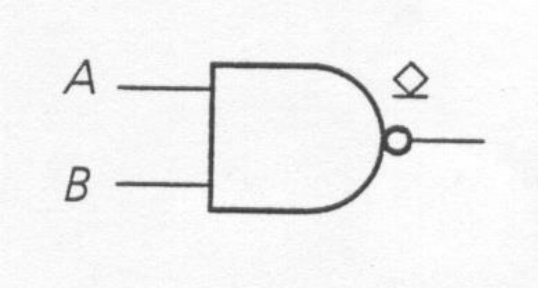


Porte in logica cablata

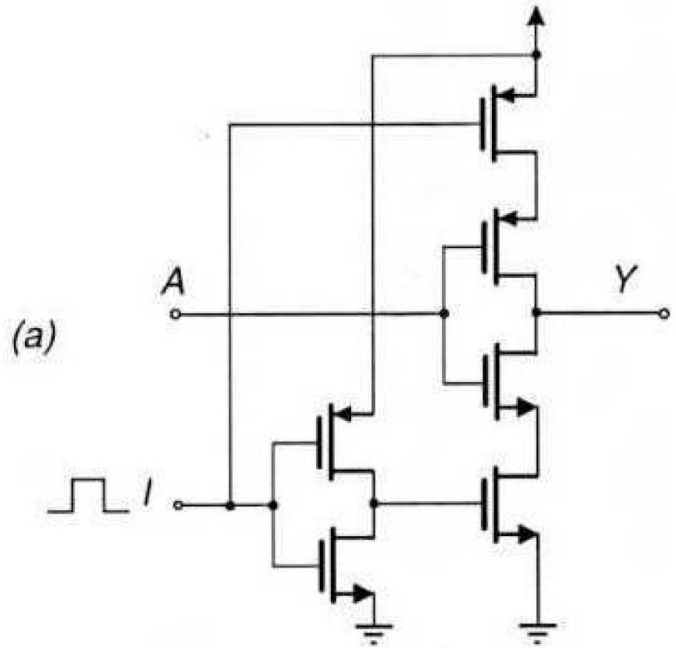


Porte in logica cablata

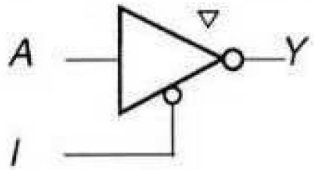




Porte a tre stati

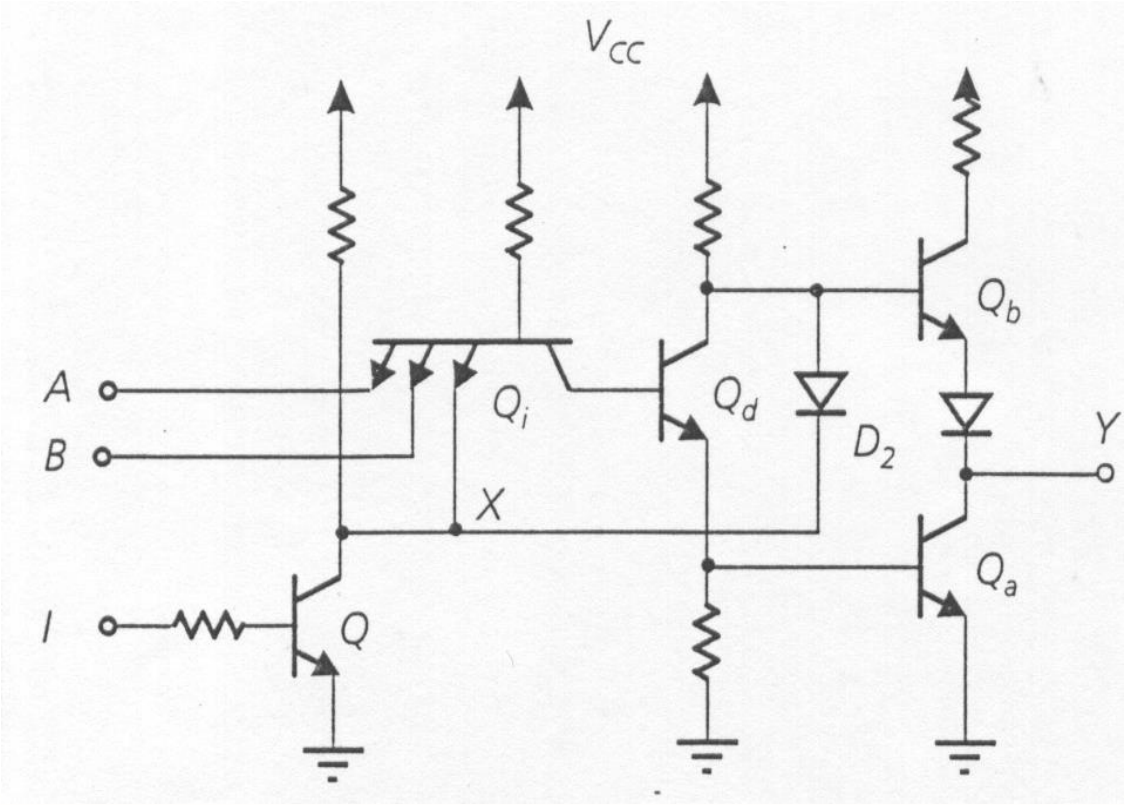


I	A	Y
0	A	$\overline{A}$
1	A	Z

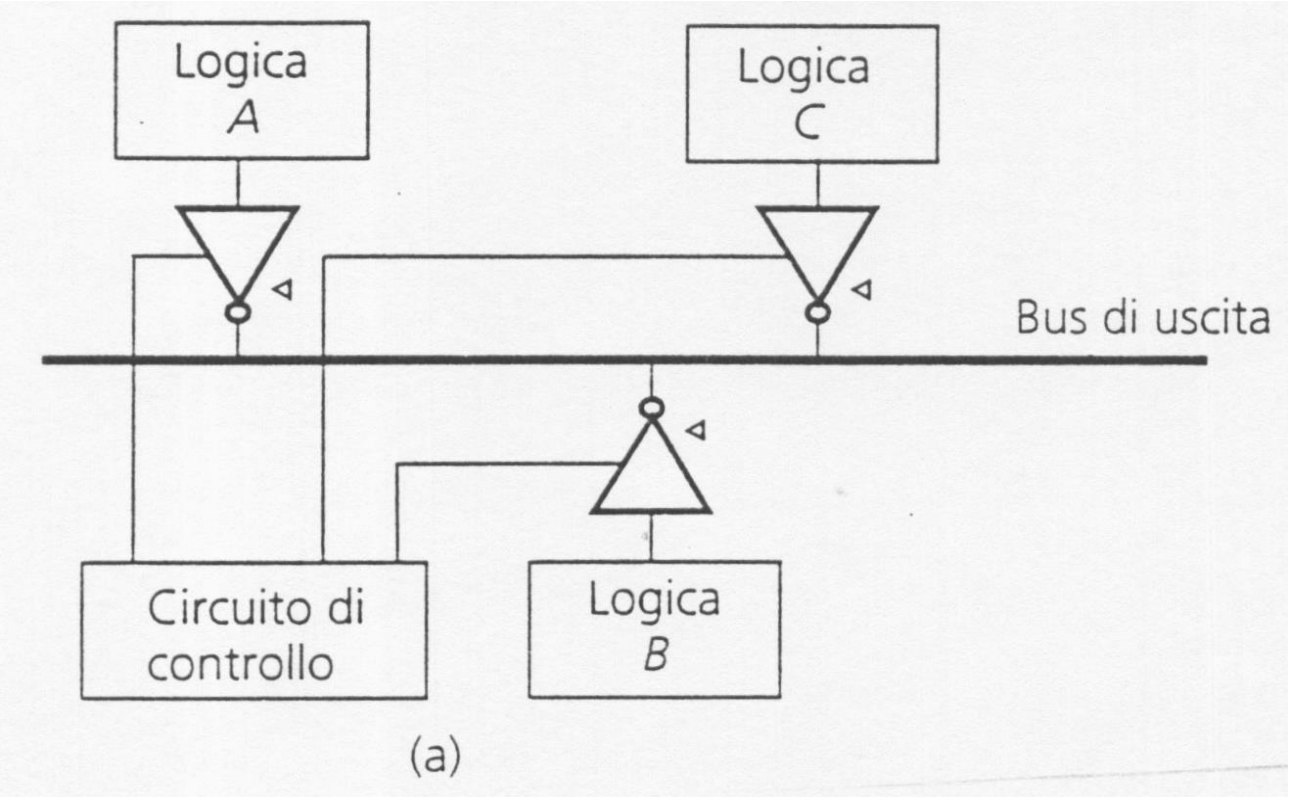


(b)

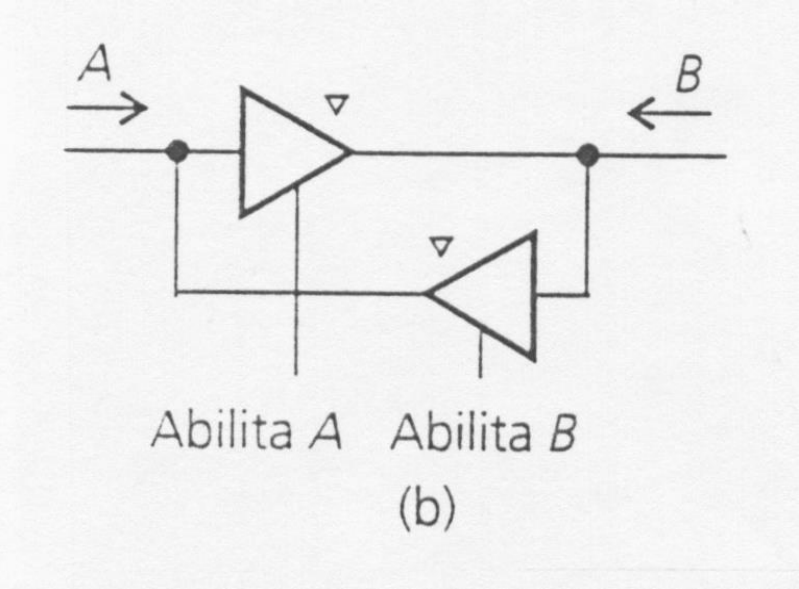
Porte a tre stati

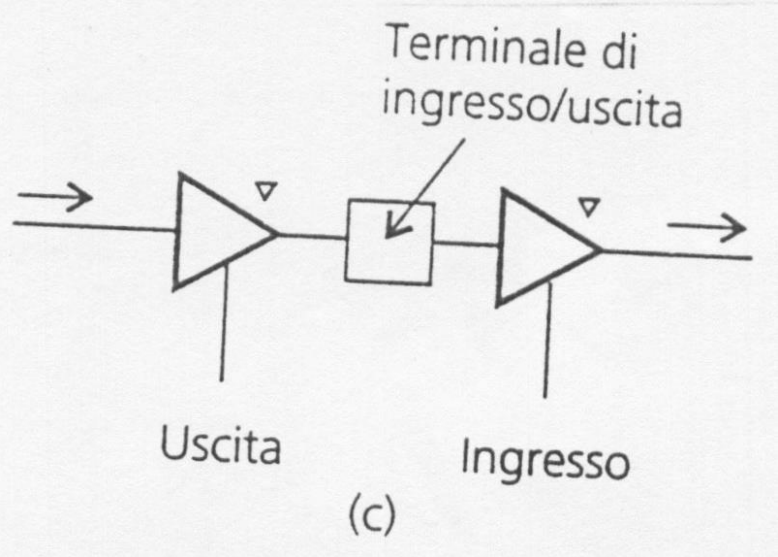


Porte a tre stati



Porte a tre stati





Vedere:

- Paolo Spirito, “Elettronica Digitale”, Ed. McGraw-Hill
  - Cap. 10.1-10.4