UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

Strutture CMOS per VLSI
A.Carini – Elettronica digitale

Progetto di sistemi digitali

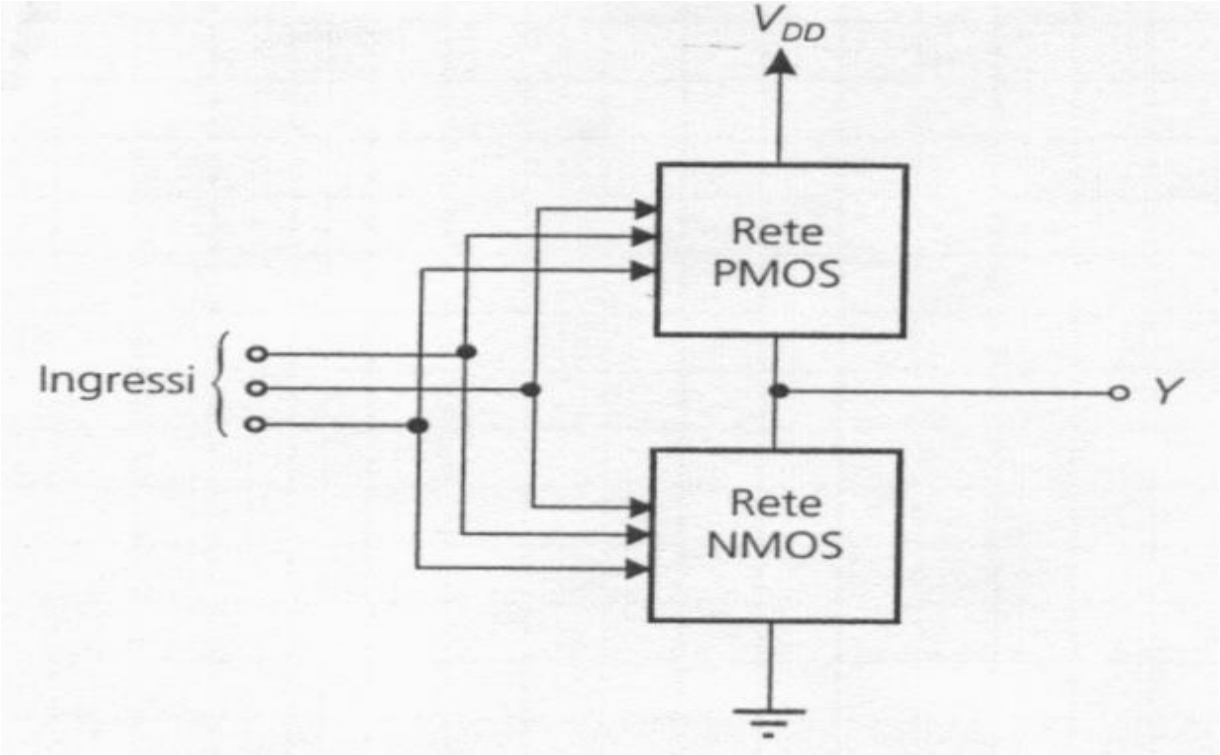
- Circuiti logici standard
- Logiche programmabili (FPGA, CPLD)
- ASIC a Celle Standard
- ASIC Full Custom

Libreria di celle standard

Tabella 13.1 Libreria di celle standard SSI e MSI.

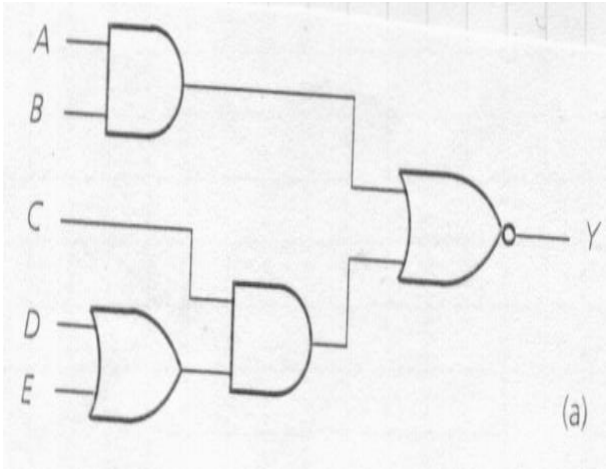
Tipo di cella	Caratteristiche
Inverter/buffer/tristate	
Porta NAND/AND	2-8 ingressi
Porta NOR/OR	2-8 ingressi
Porta XOR/XNOR	2-3 ingressi
Porta AOI/OAI	
Multiplexer	2-8 ingressi
Decoder	2-8 ingressi
Schmitt trigger	invertente, non invertente
Adder	normale, veloce
Bistabile	D, asincrono, sincrono
Registro	D, JK, asincrono, sincrono
Circuiti I/O	In, out, tristate, bidirezionali
ROM	

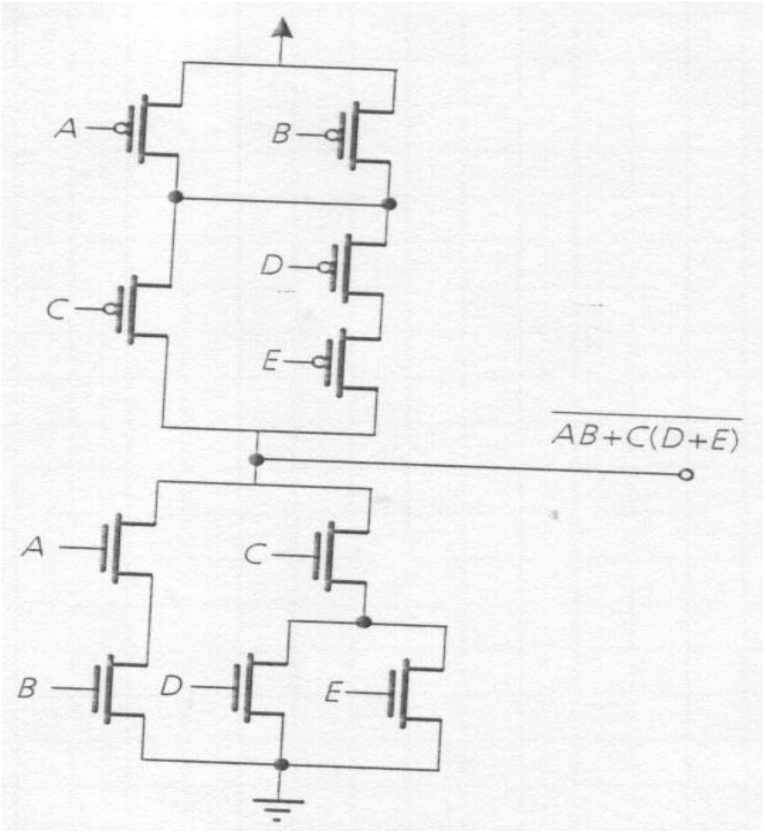
Logiche complesse FCMOS



Logiche complesse FCMOS

$$Y = \overline{AB + C(D + E)}$$





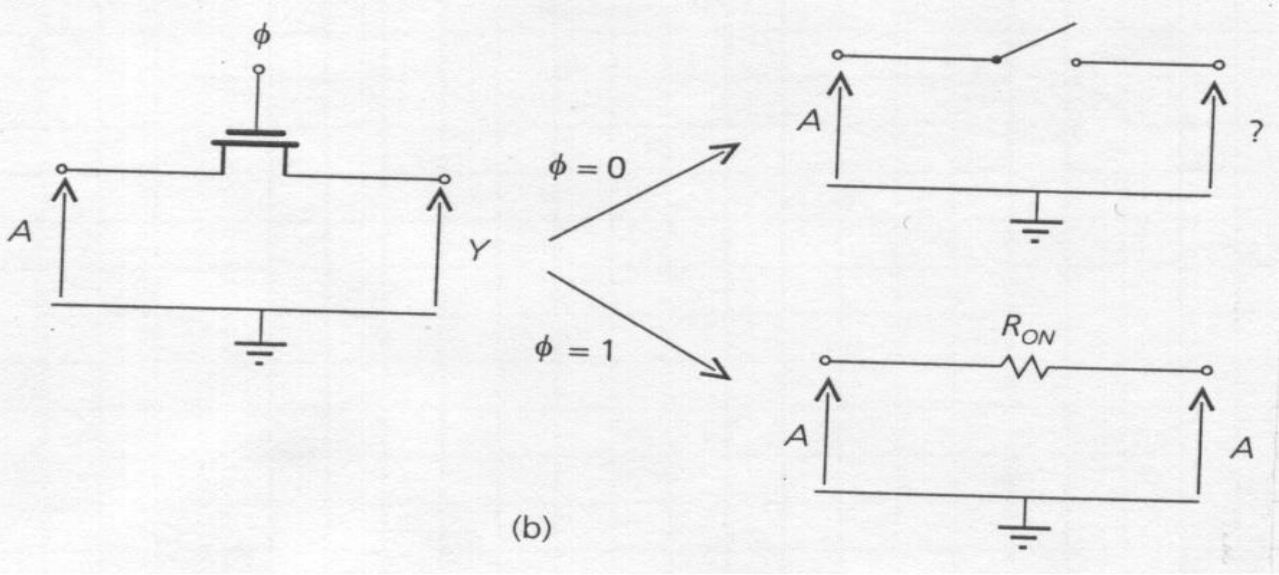
Logiche a porte di trasmissione

- Con transistori MOS, è possibile collegare il dispositivo in serie sulla via del segnale usandolo come un interruttore controllato mediante il terminale di gate.
- Il dispositivo è detto porta di trasmissione.
- Il segnale di controllo viene detto fase.

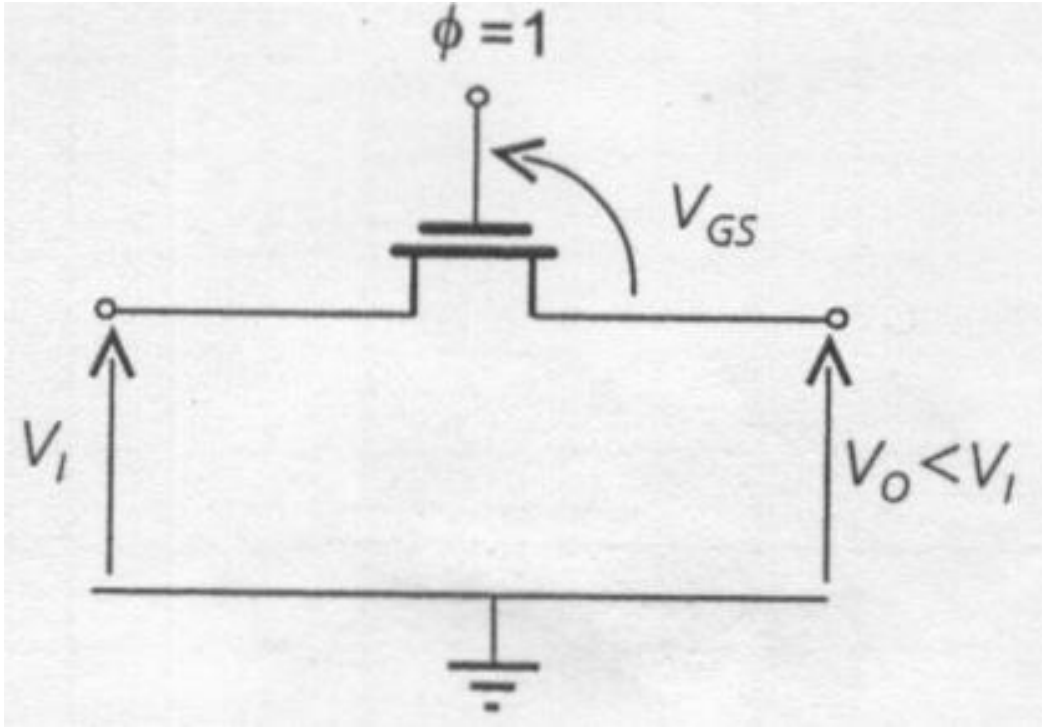
ϕ	A	Y
0	0	aperto
0	1	aperto
1	0	0
1	1	1

Pass Transistor

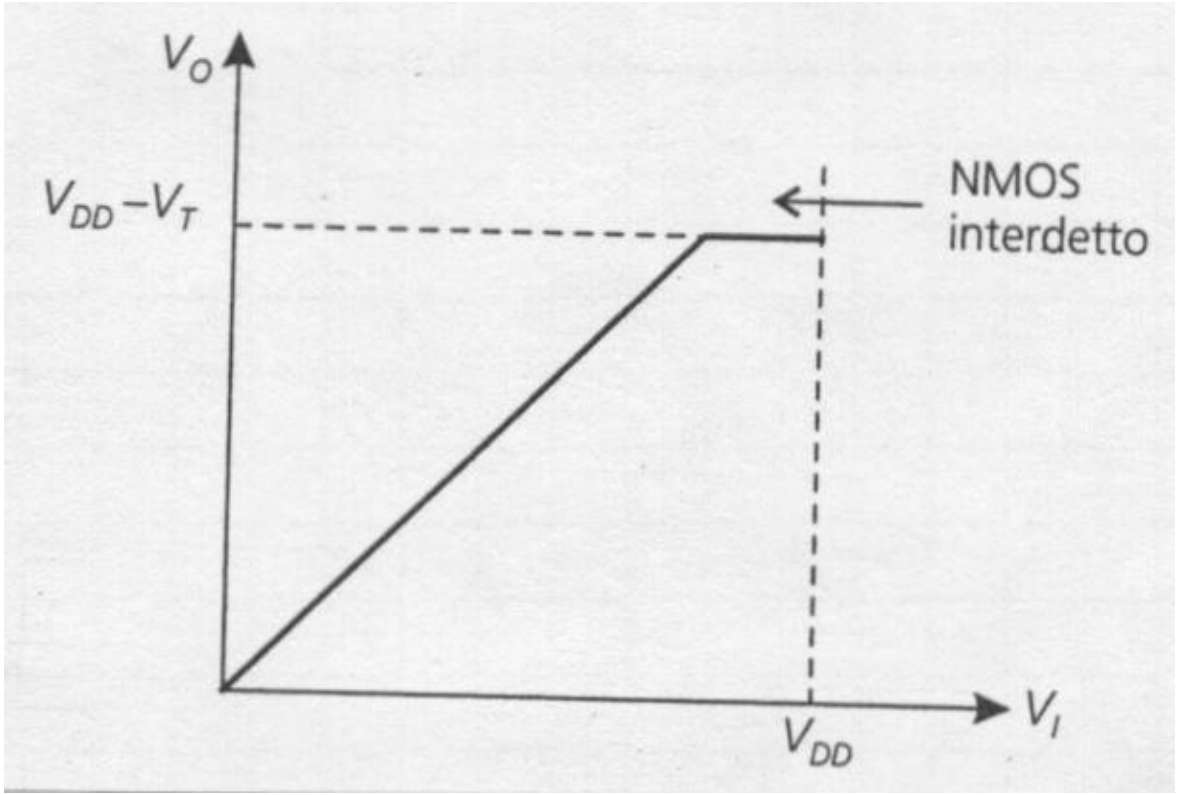
- Con transistori NMOS
  - Realizza bene stato di circuito aperto
  - Realizza male lo stato di cortocircuito



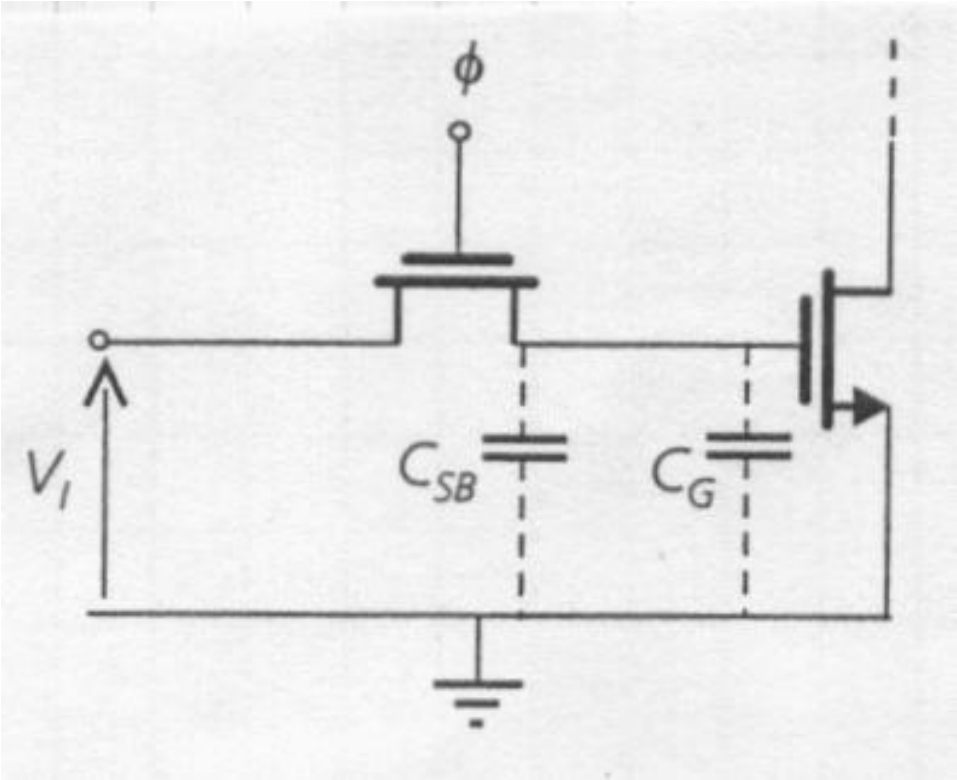
Pass Transistor



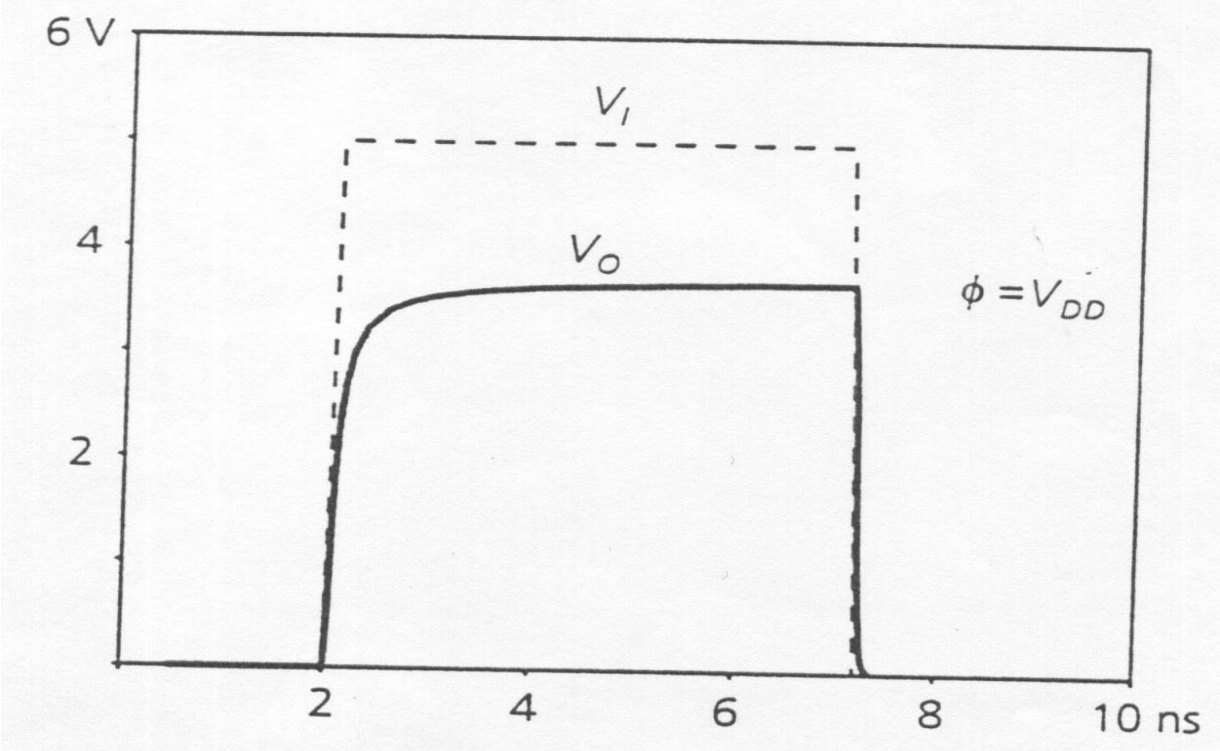
Pass Transistor



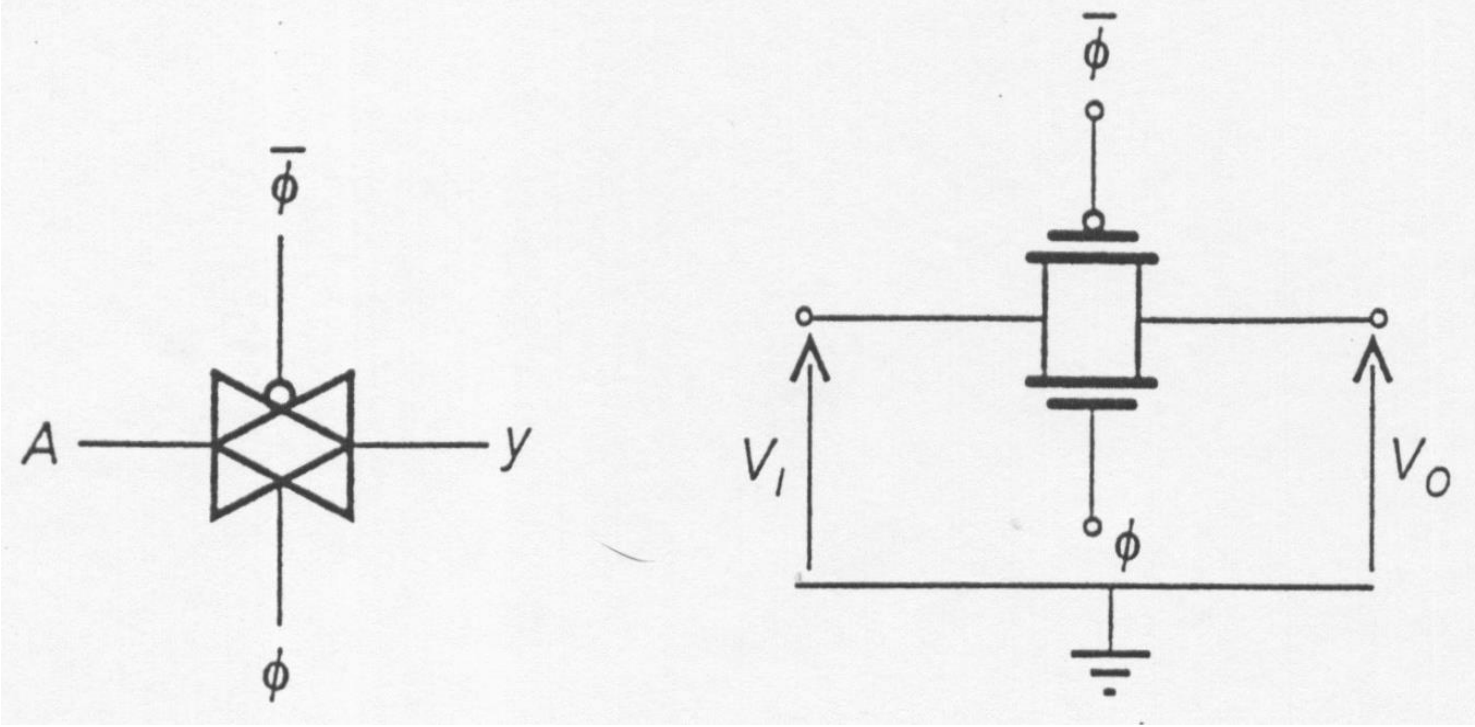
Prestazioni dinamiche



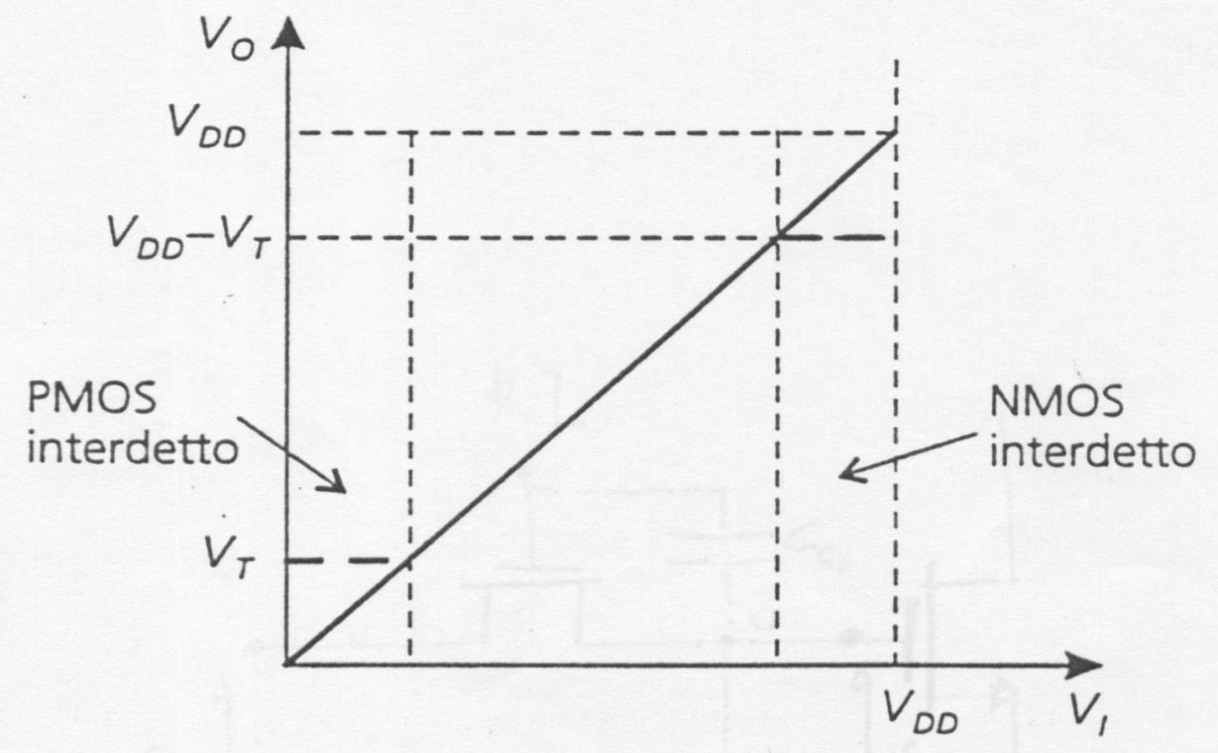
Prestazioni dinamiche



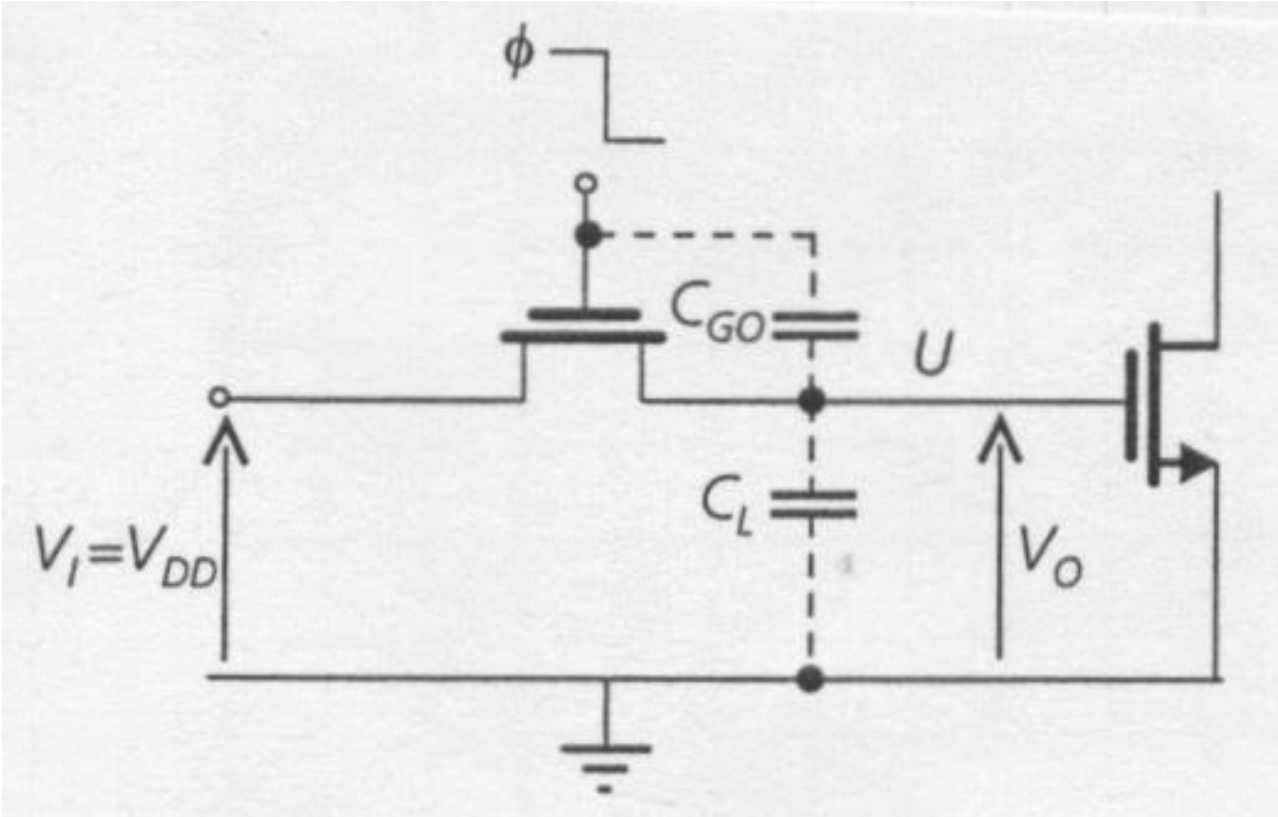
Porte di trasmissione CMOS



Porte di trasmissione CMOS



Disturbo dovuto al segnale di fase



Disturbo dovuto al segnale di fase

$$\phi = V_{DD} \longrightarrow V_O = V_{DD} - V_T$$

$$Q_U = C_L V_O + (-C_{GO} V_T)$$

$$\phi \mapsto 0 \longrightarrow Q'_U = Q_U = (C_L + C_{GO}) V'_O$$

La carica al nodo U (Q_U) si conserva durante la transizione di Φ da V_{DD} a 0.
Il salto di tensione viene trasmesso in uscita.

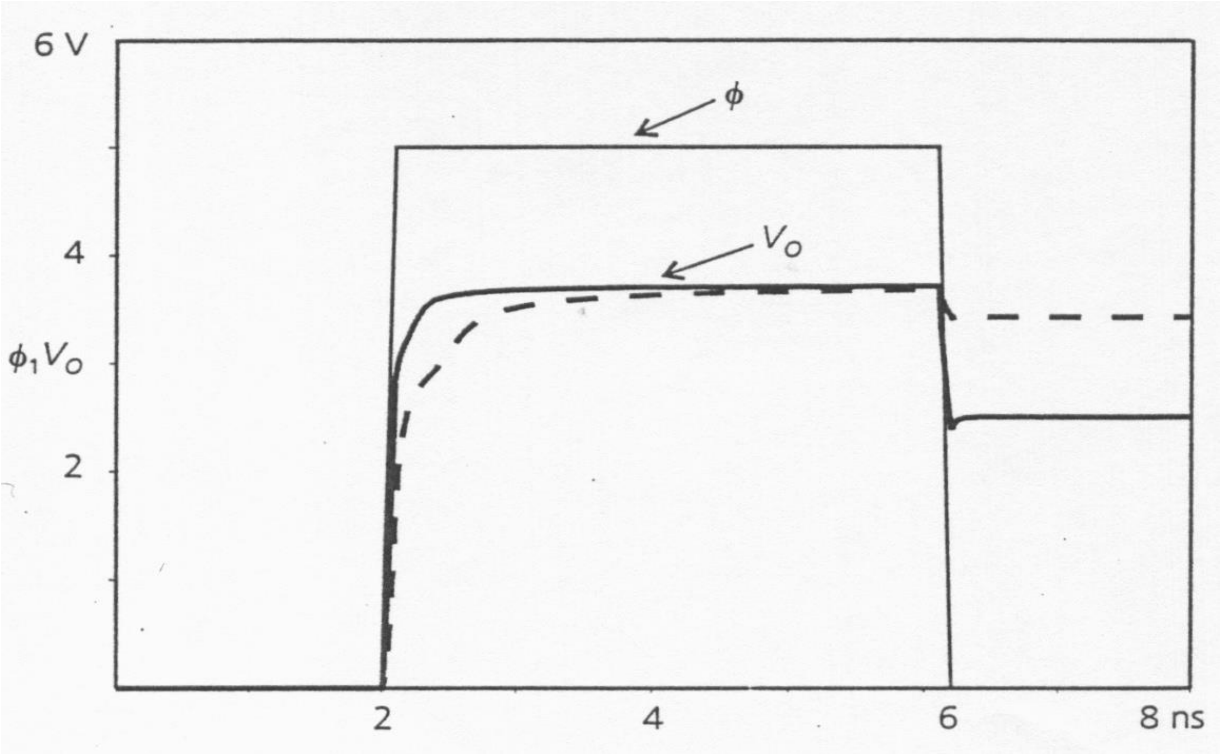
Disturbo dovuto al segnale di fase

$$C_L V_O + (-C_{GO} V_T) = (C_L + C_{GO}) V_O'$$

$$\rightarrow \quad V_O' = \frac{C_L}{C_L + C_{GO}} V_{DD} - V_T$$

$$\Delta V_O = V_O' - V_O = -\frac{C_{GO}}{C_L + C_{GO}} V_{DD}$$

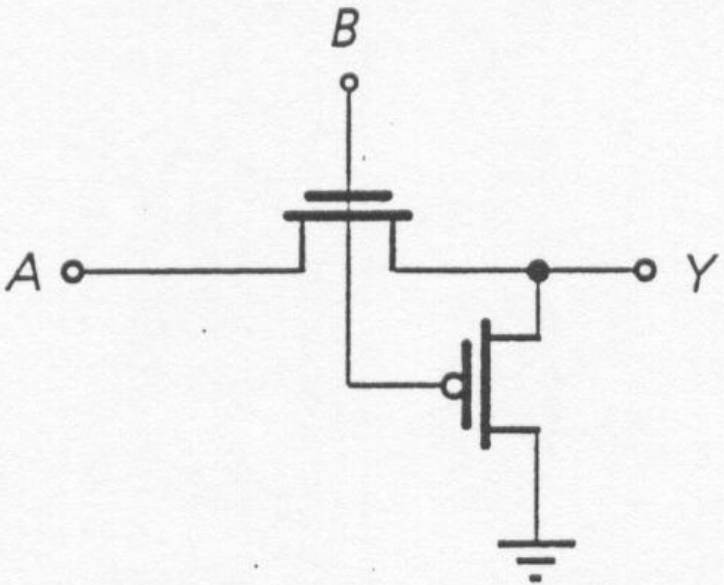
Disturbo dovuto al segnale di fase



Porta AND a pass-transistor

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(a)

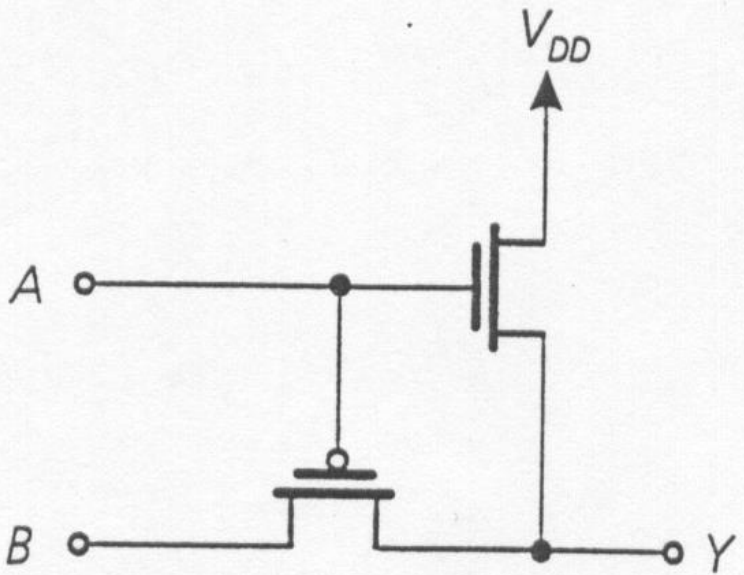


(b)

Porta OR a pass-transistor

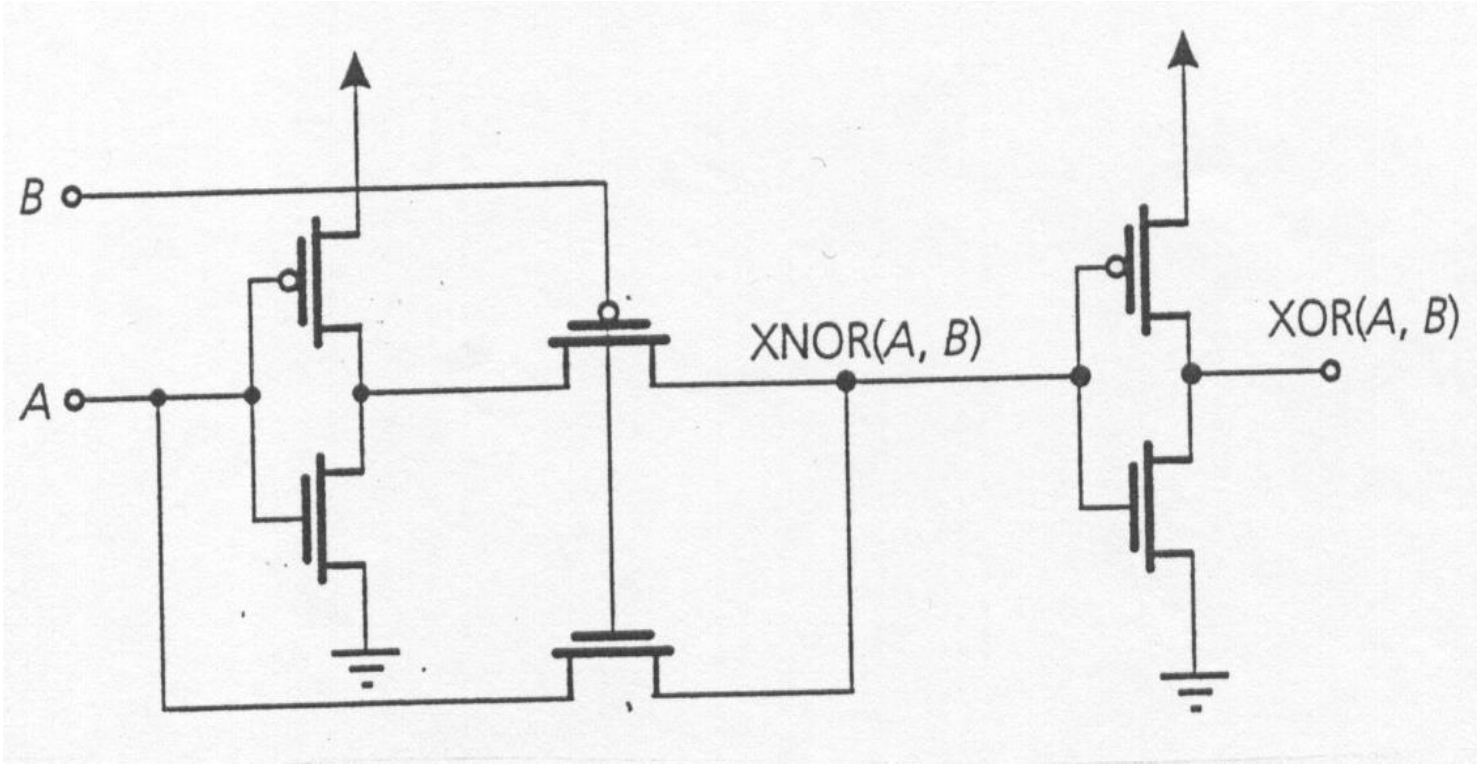
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(a)

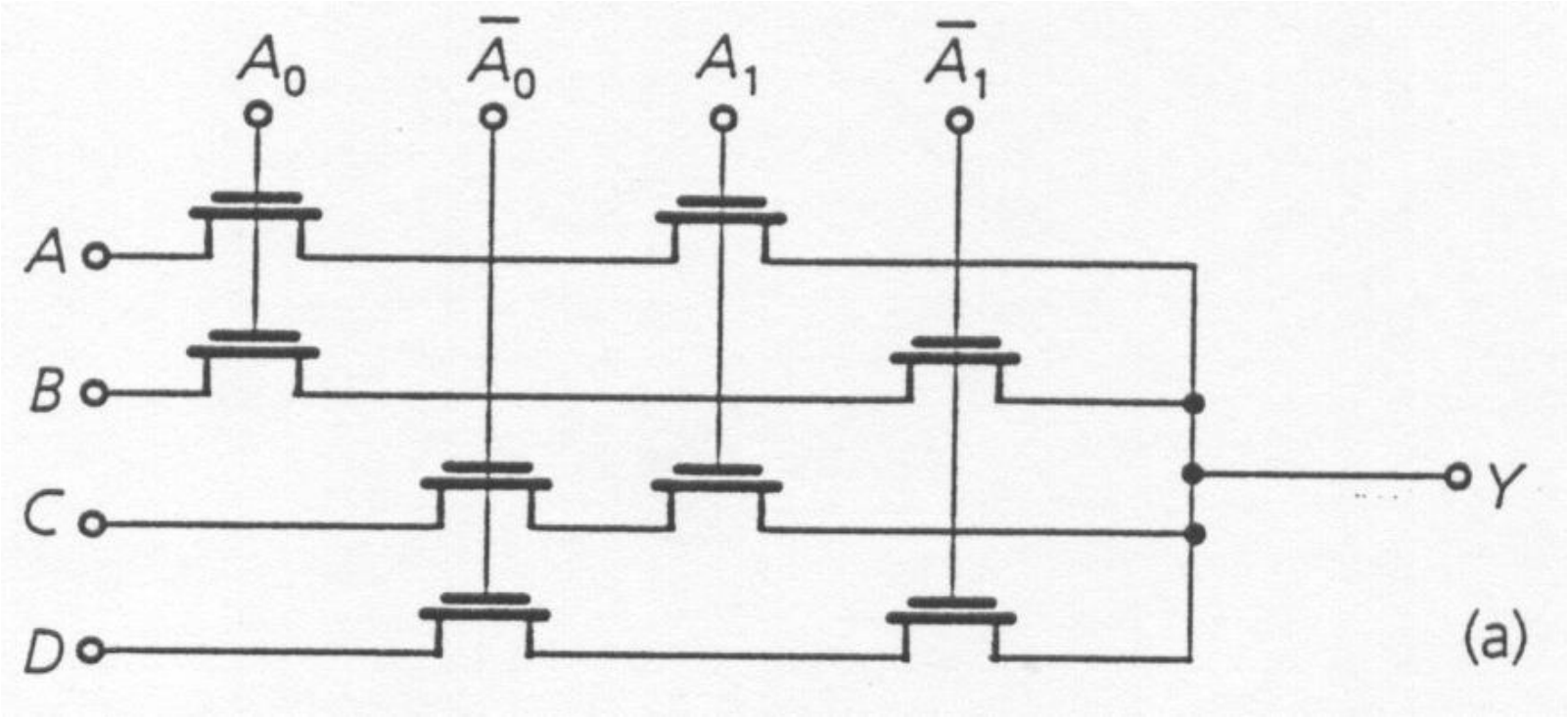


(b)

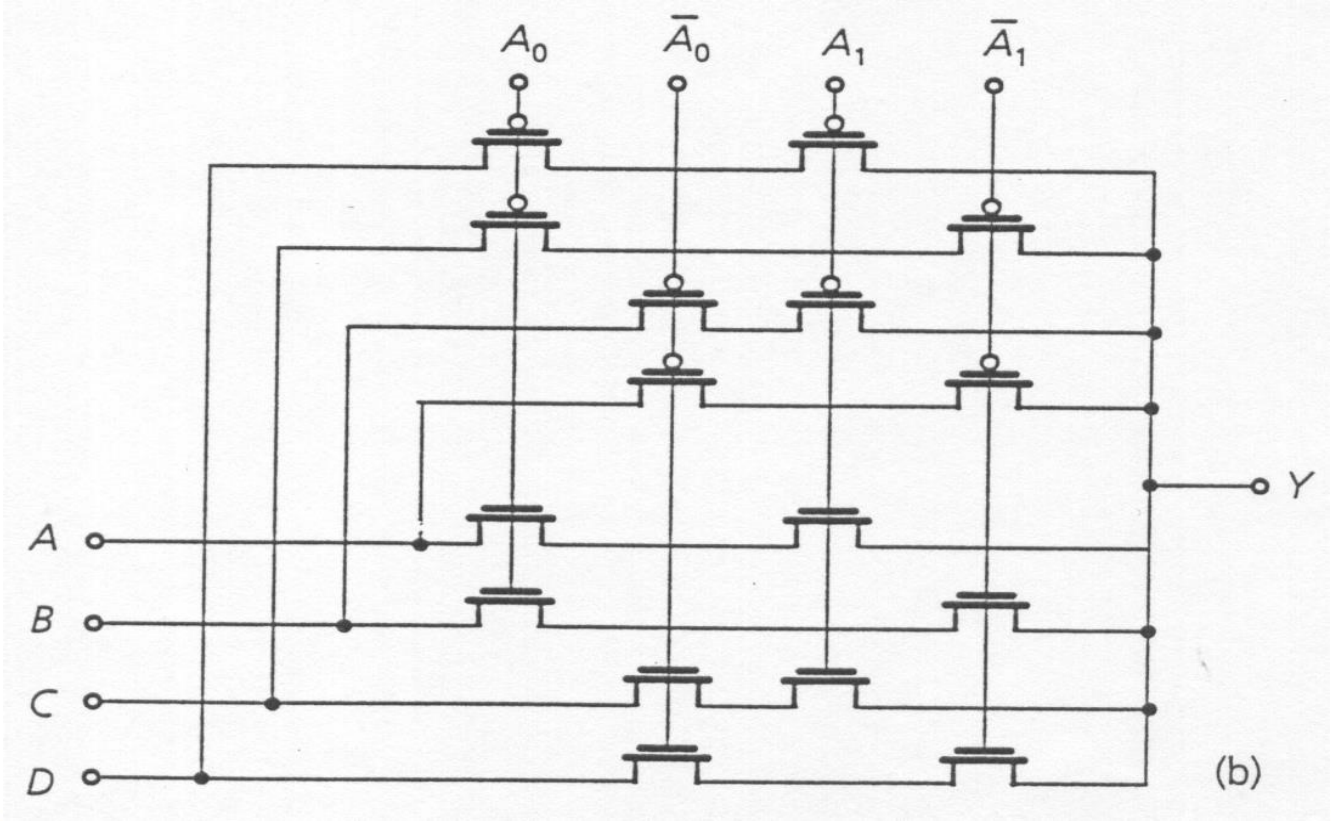
Porta XOR a pass-transistor



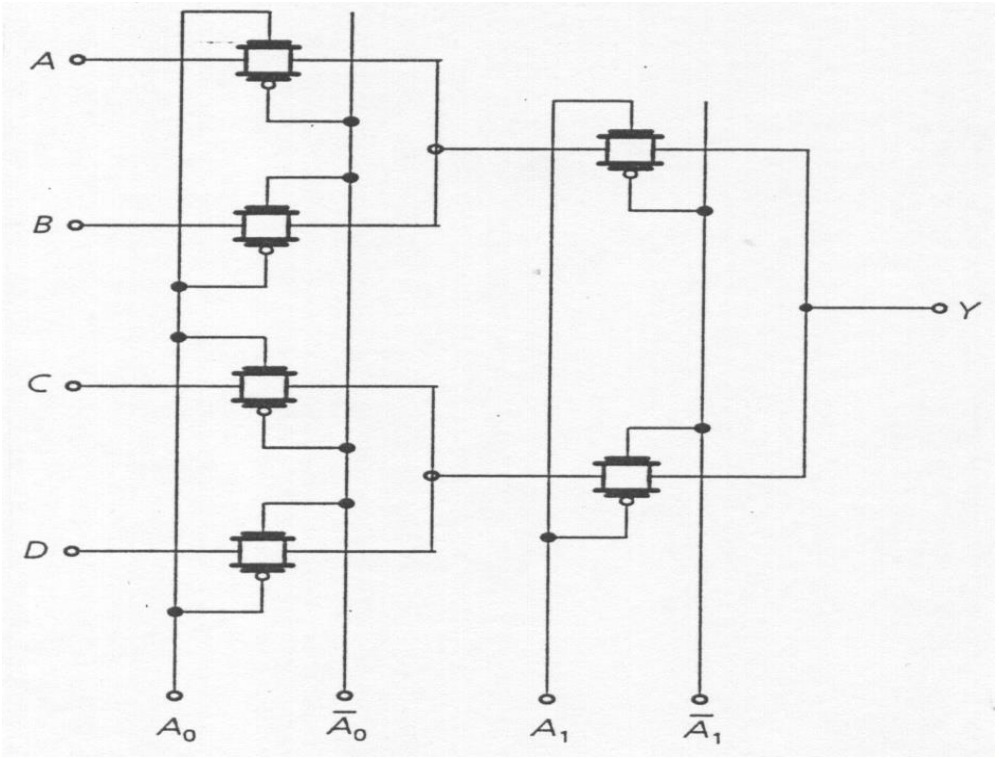
Multiplexer a porte NMOS



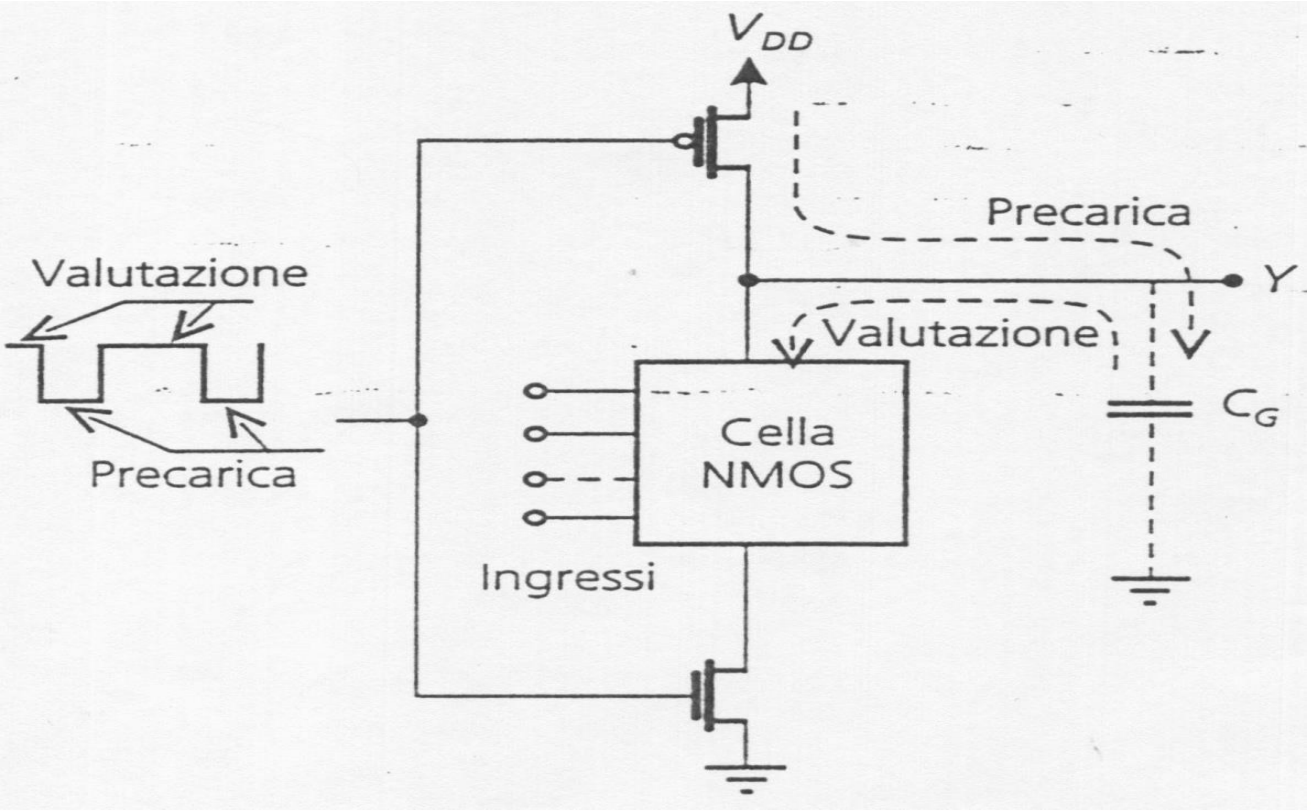
Multiplexer a porte CMOS



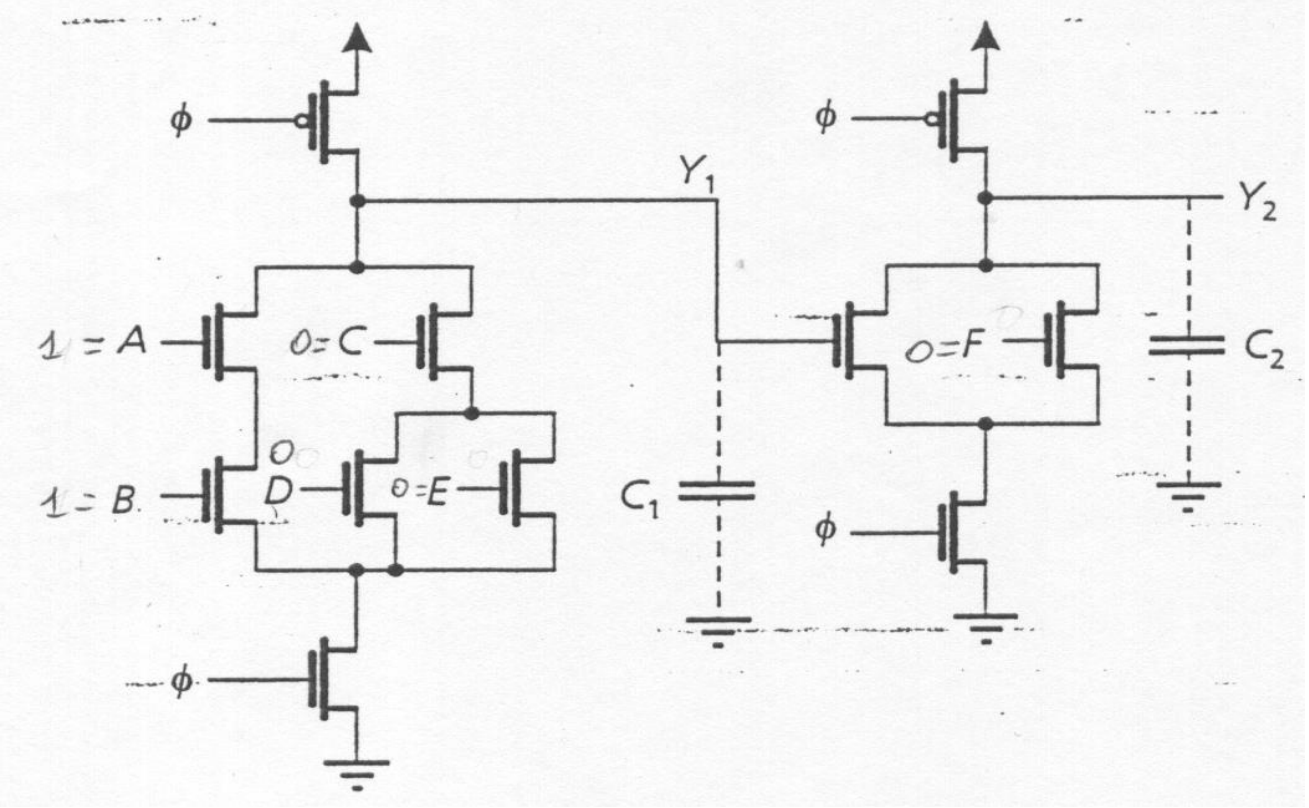
Multiplexer ad albero



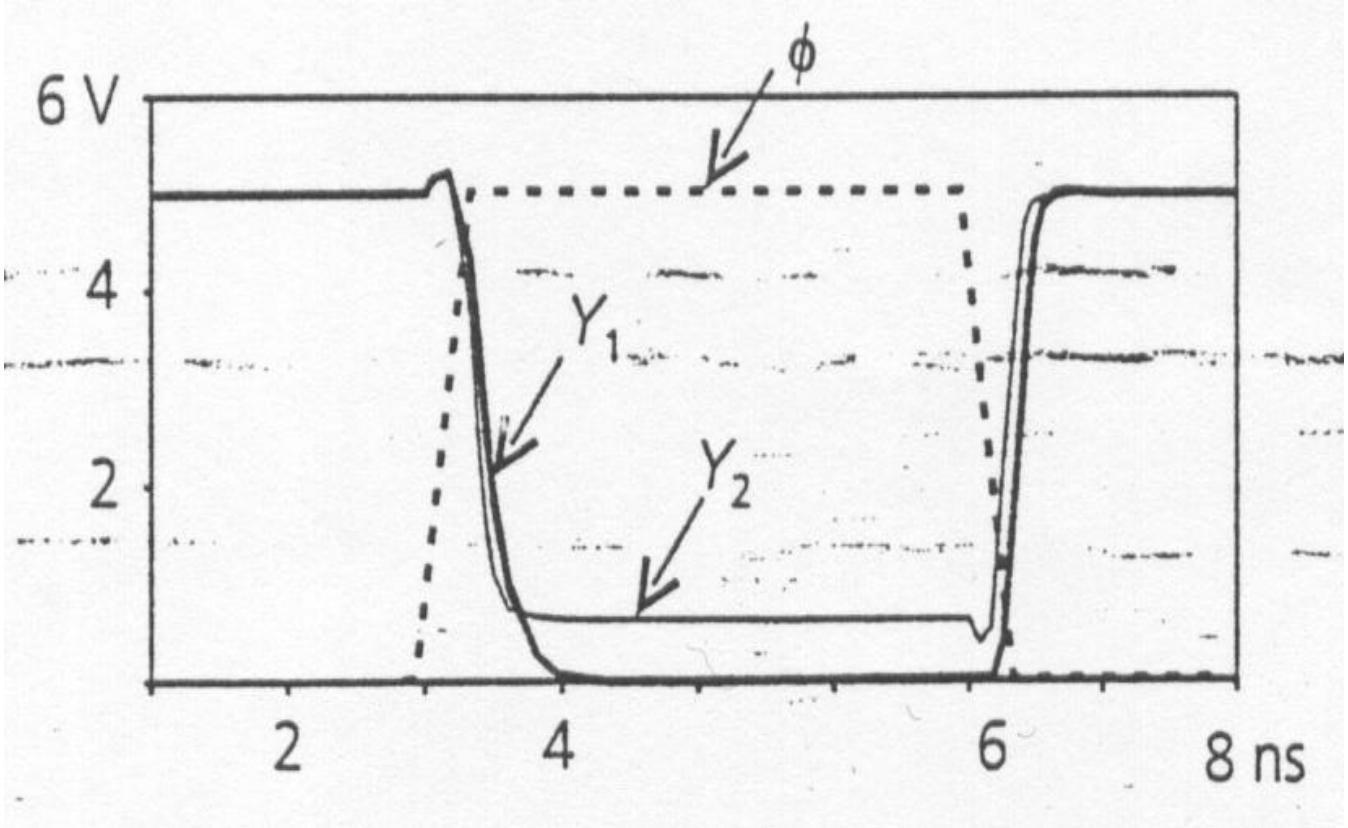
Logica dinamica a 1 fase



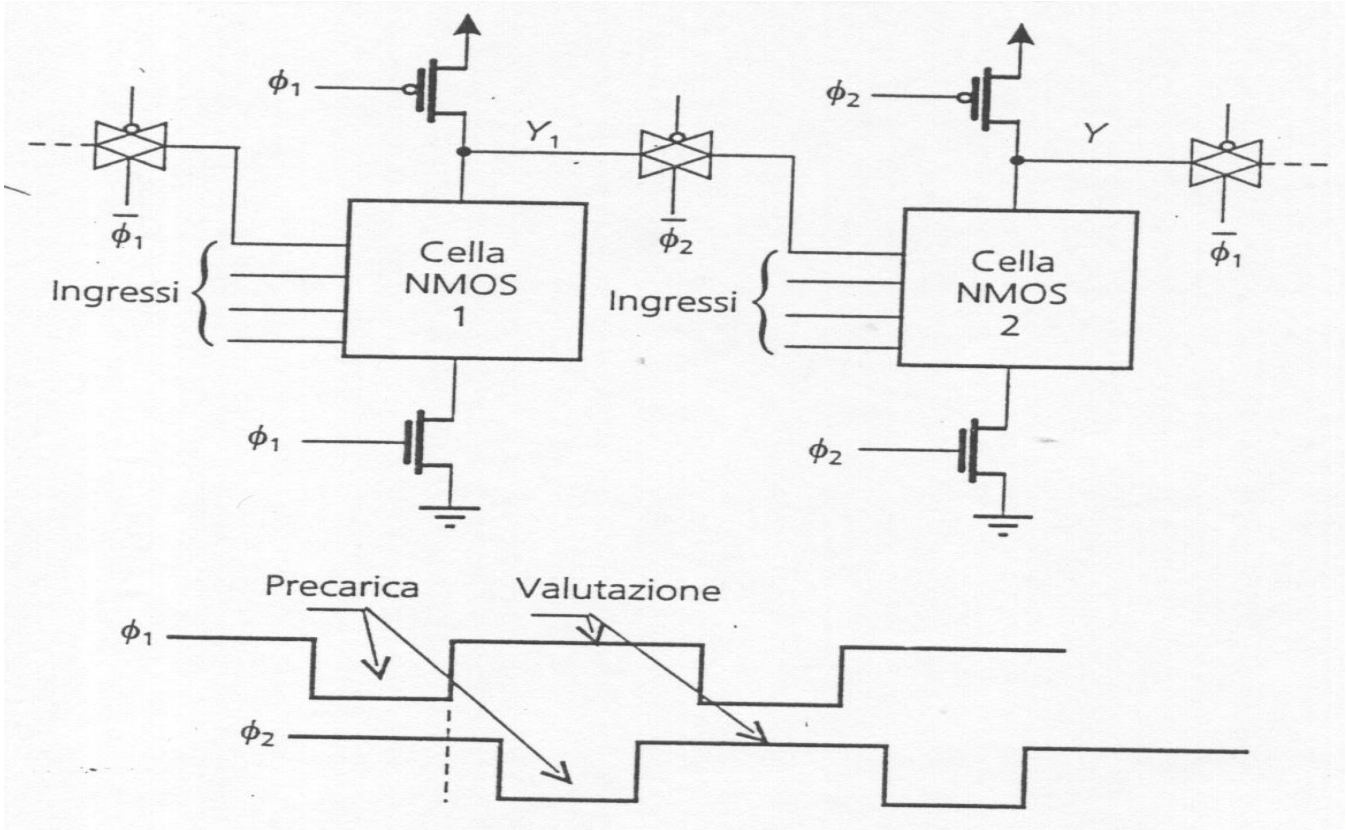
Logica dinamica a 1 fase



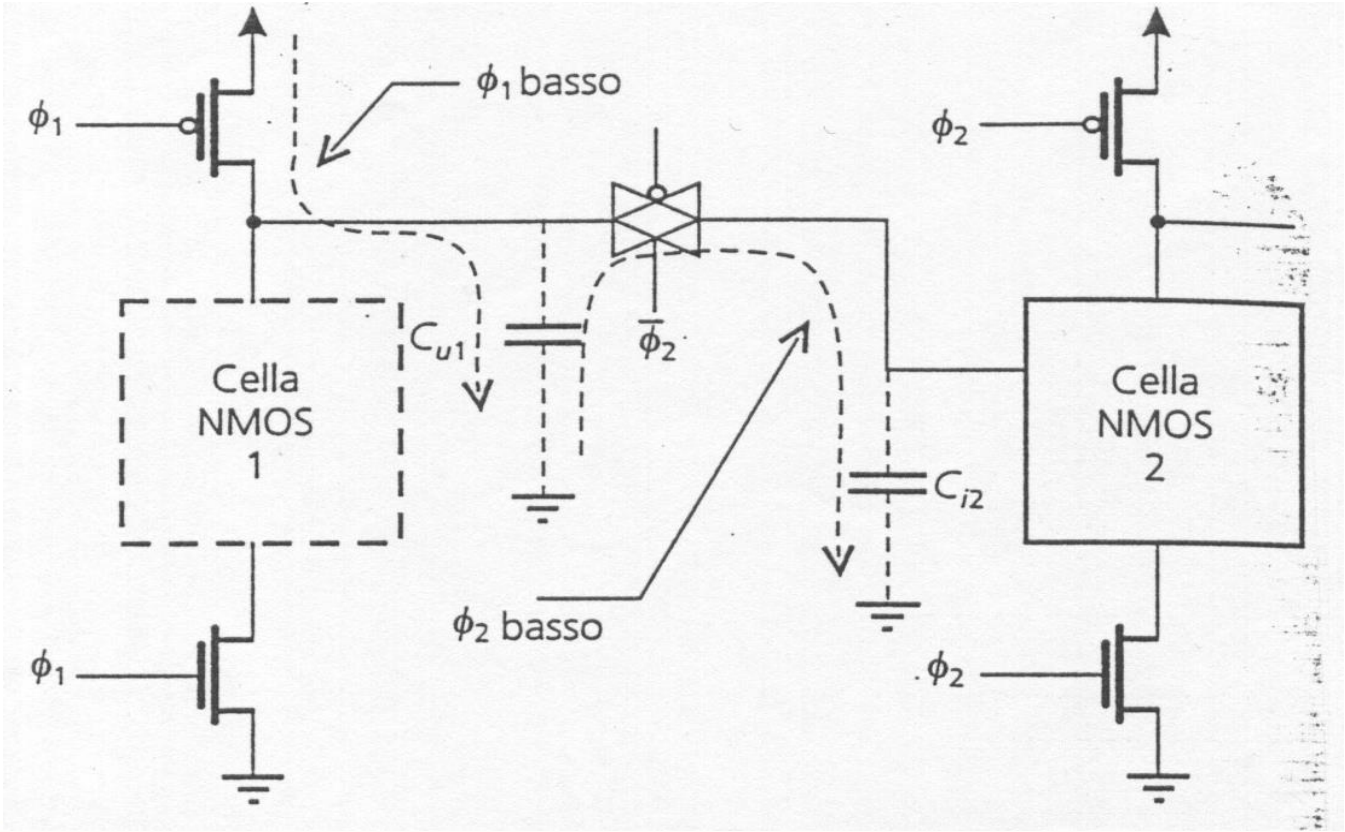
Logica dinamica a 1 fase



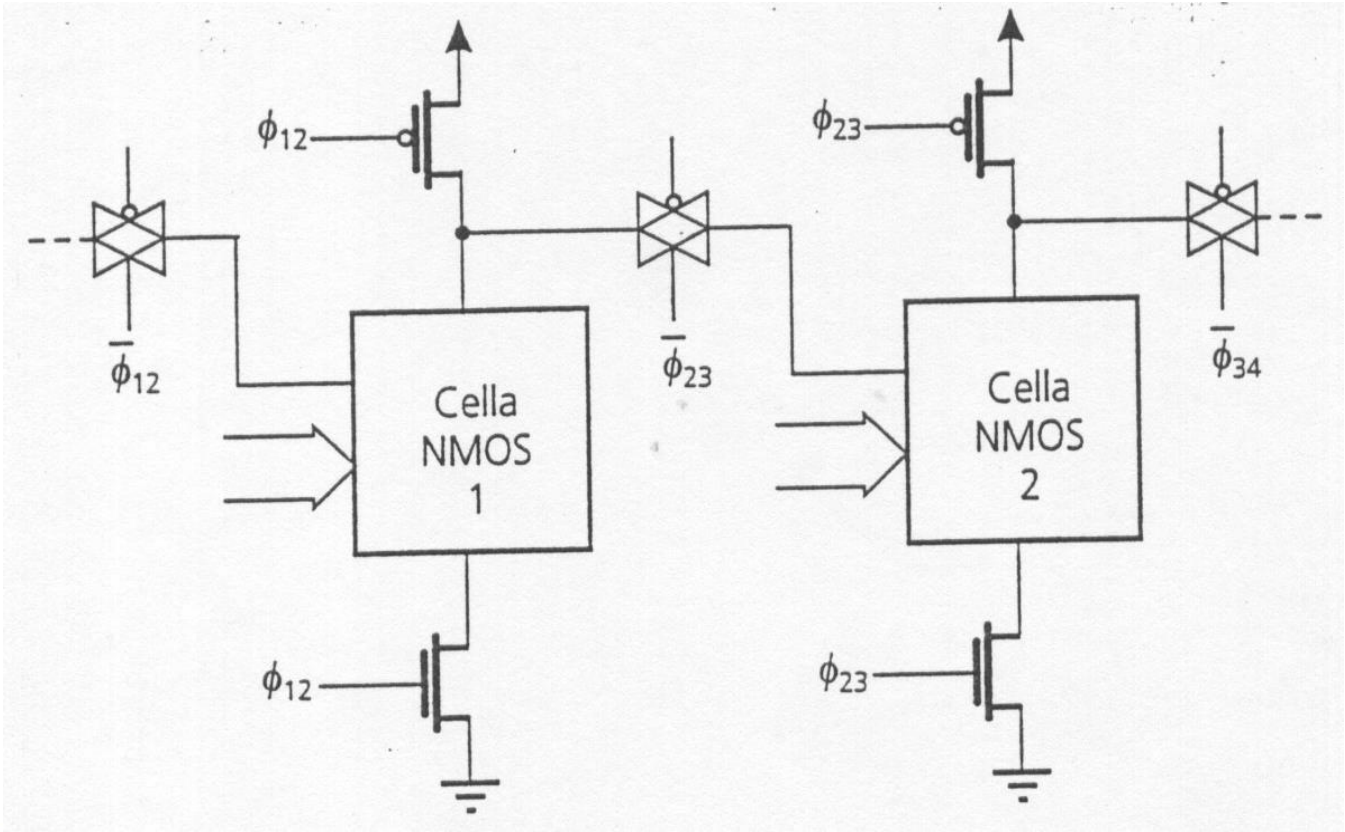
Logica dinamica a 2 fasi



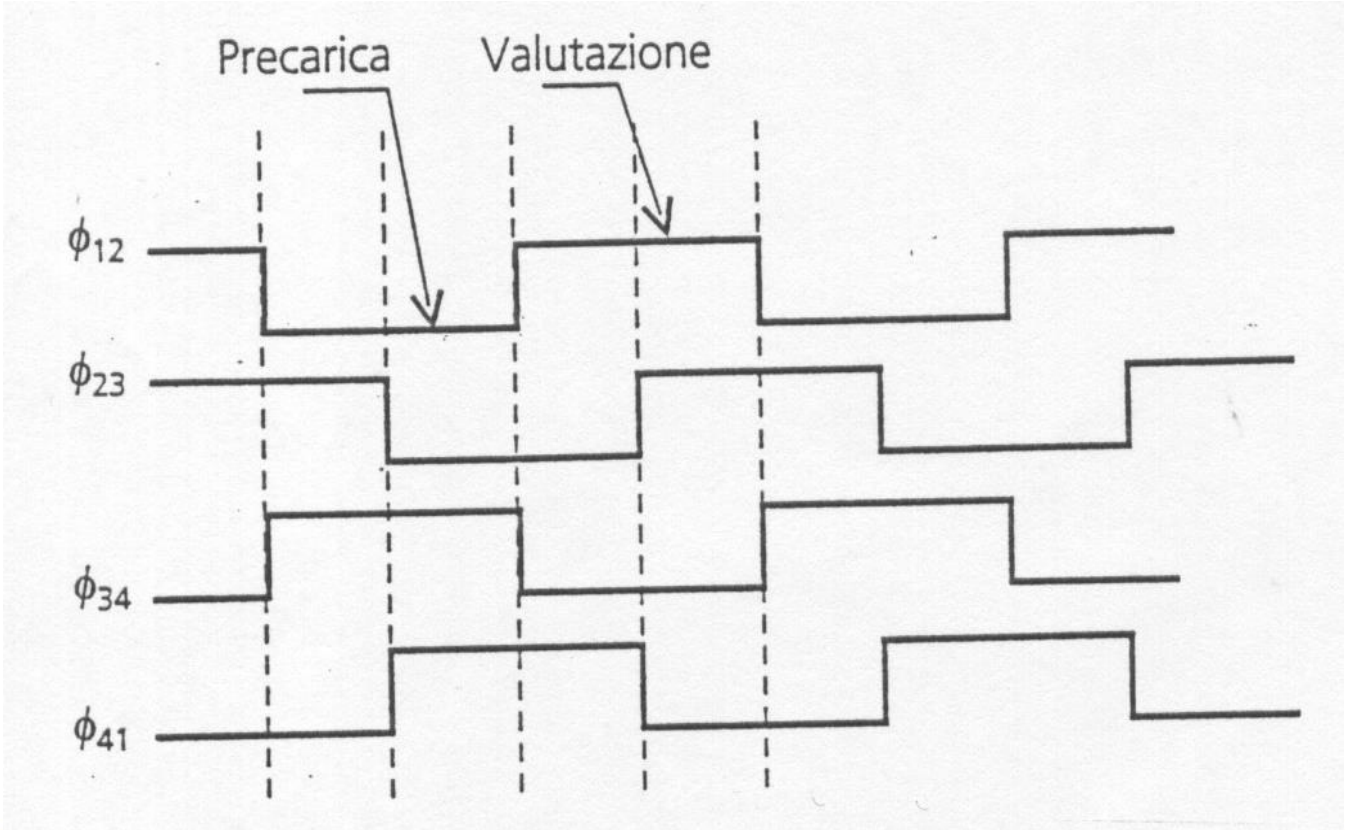
Logica dinamica a 2 fasi



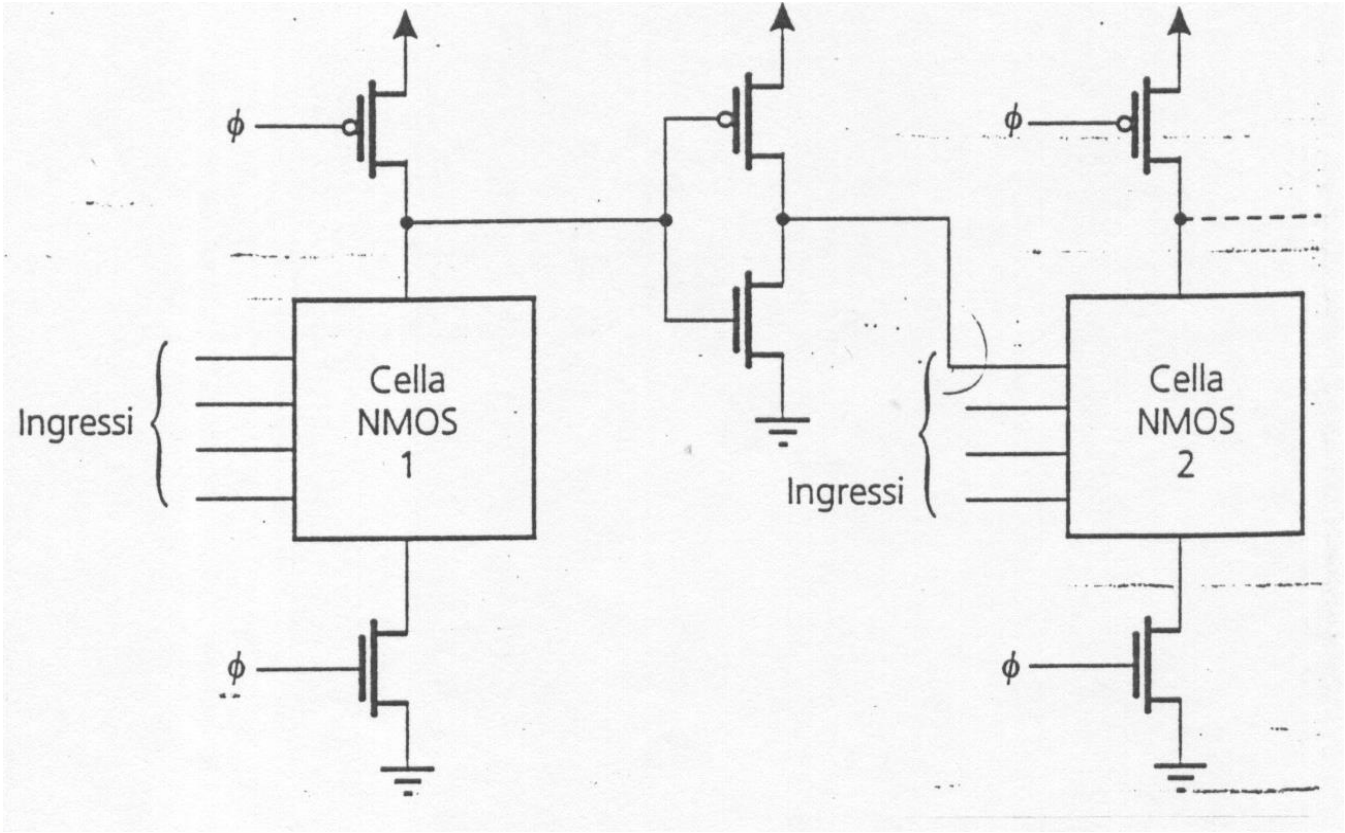
Logica dinamica a 4 fasi



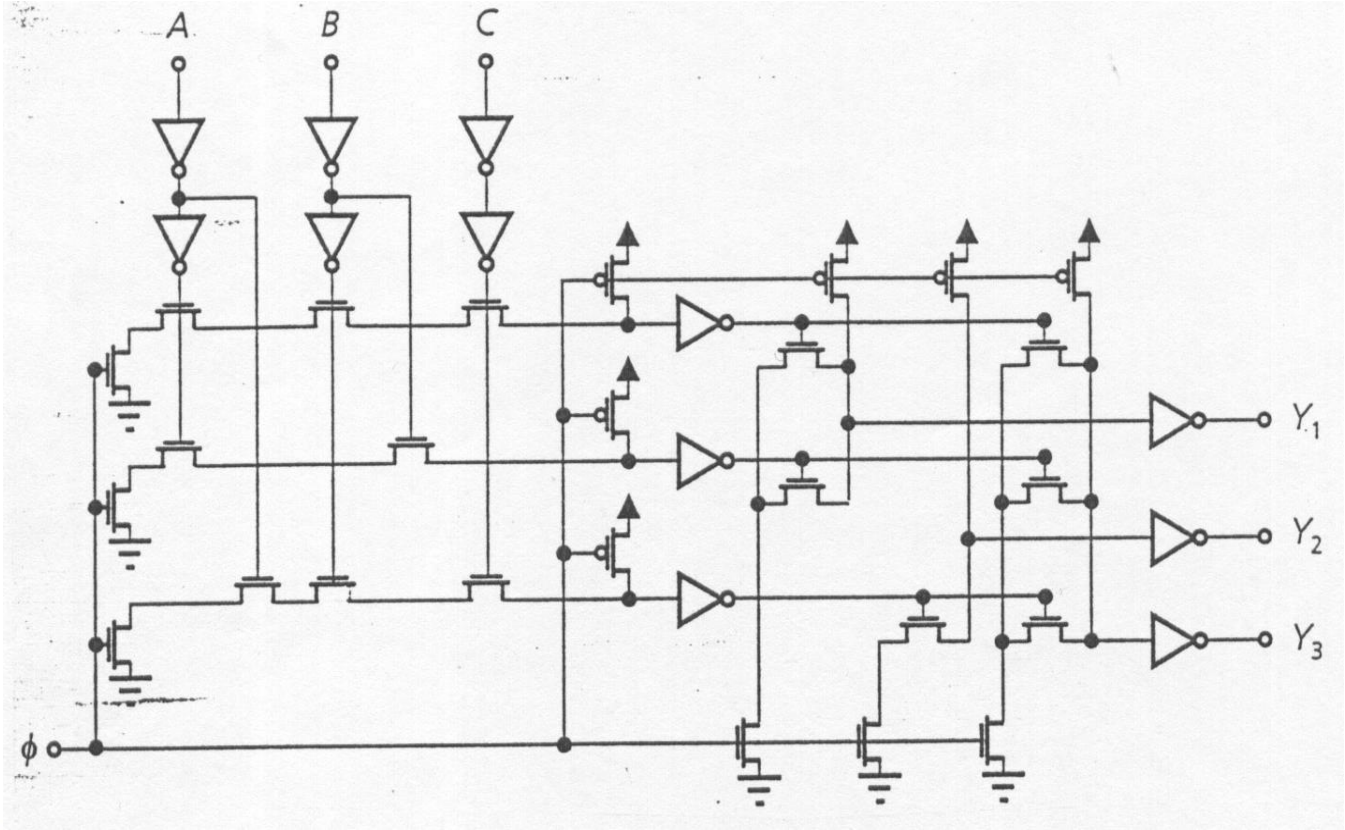
Logica dinamica a 4 fasi



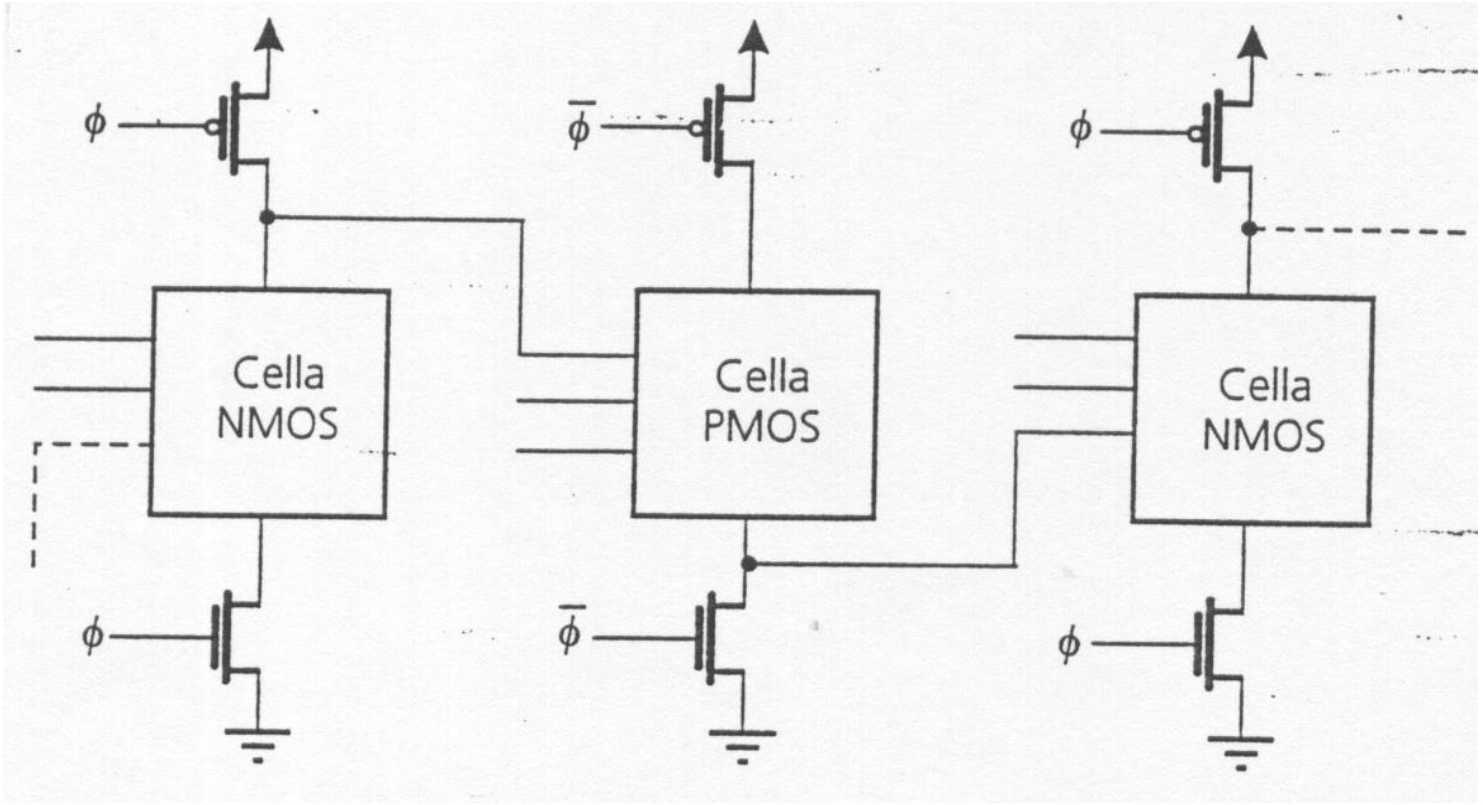
Logica domino



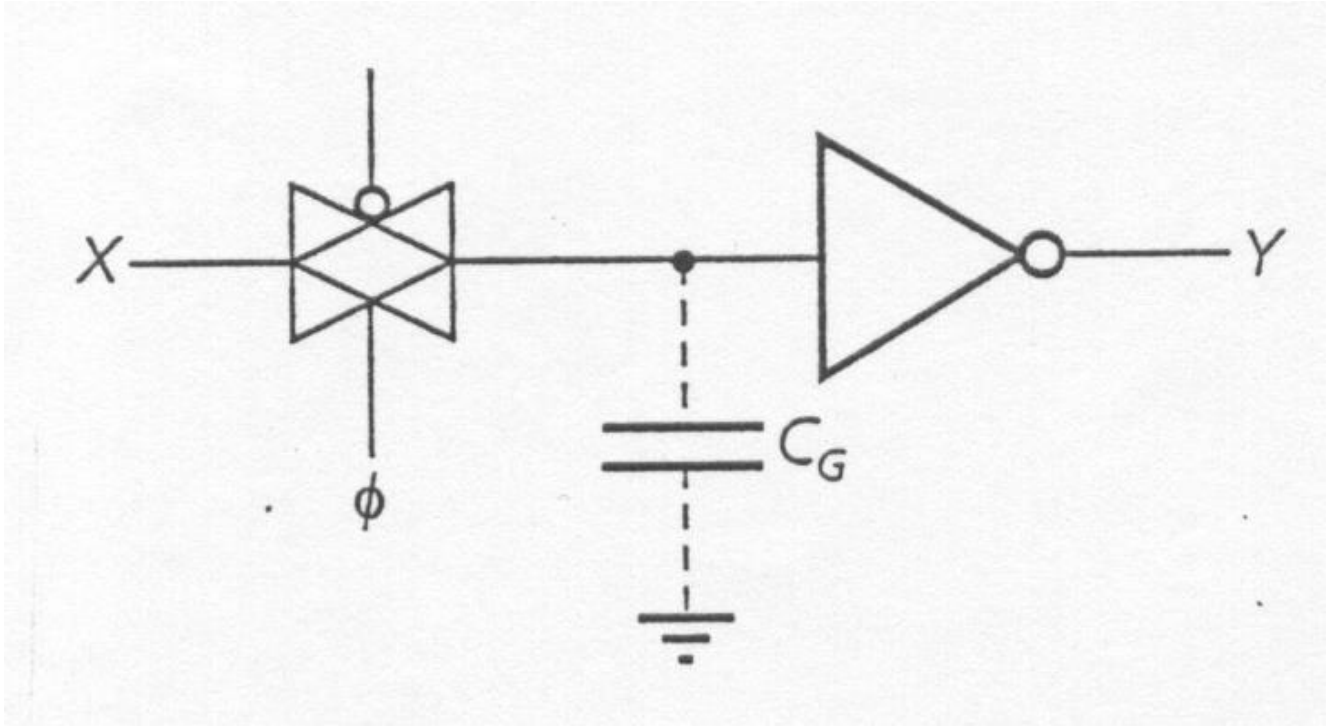
PLA in logica domino



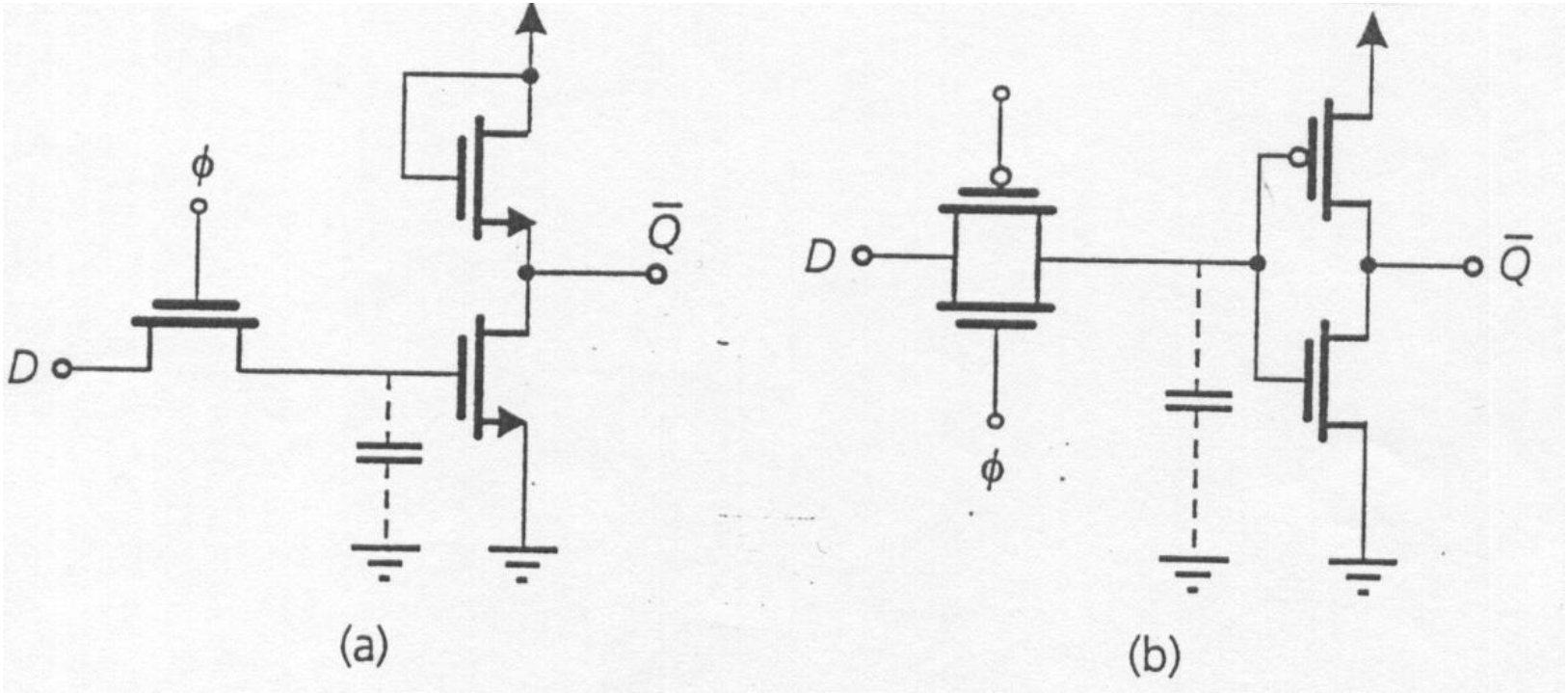
Logica NORA CMOS



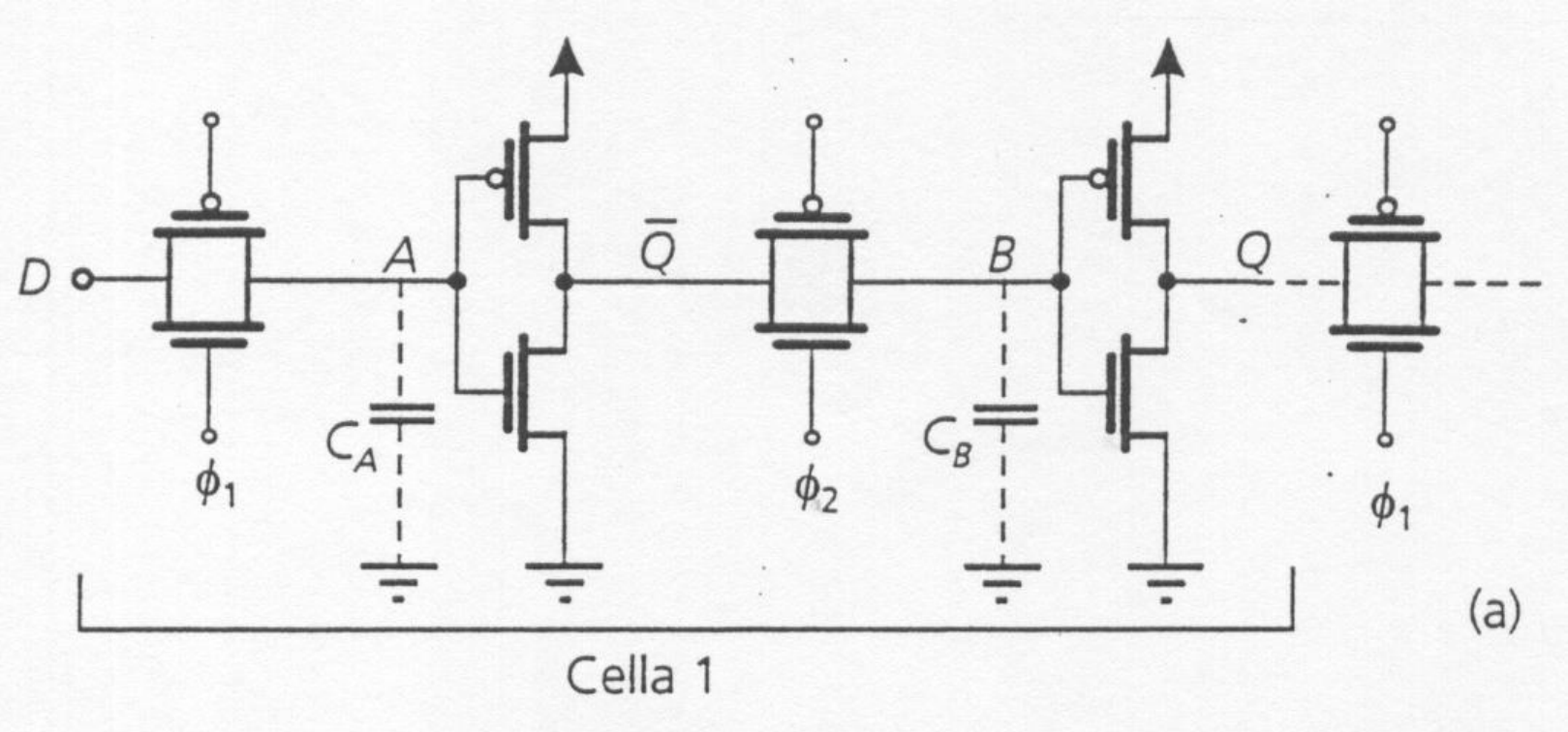
Latch dinamici



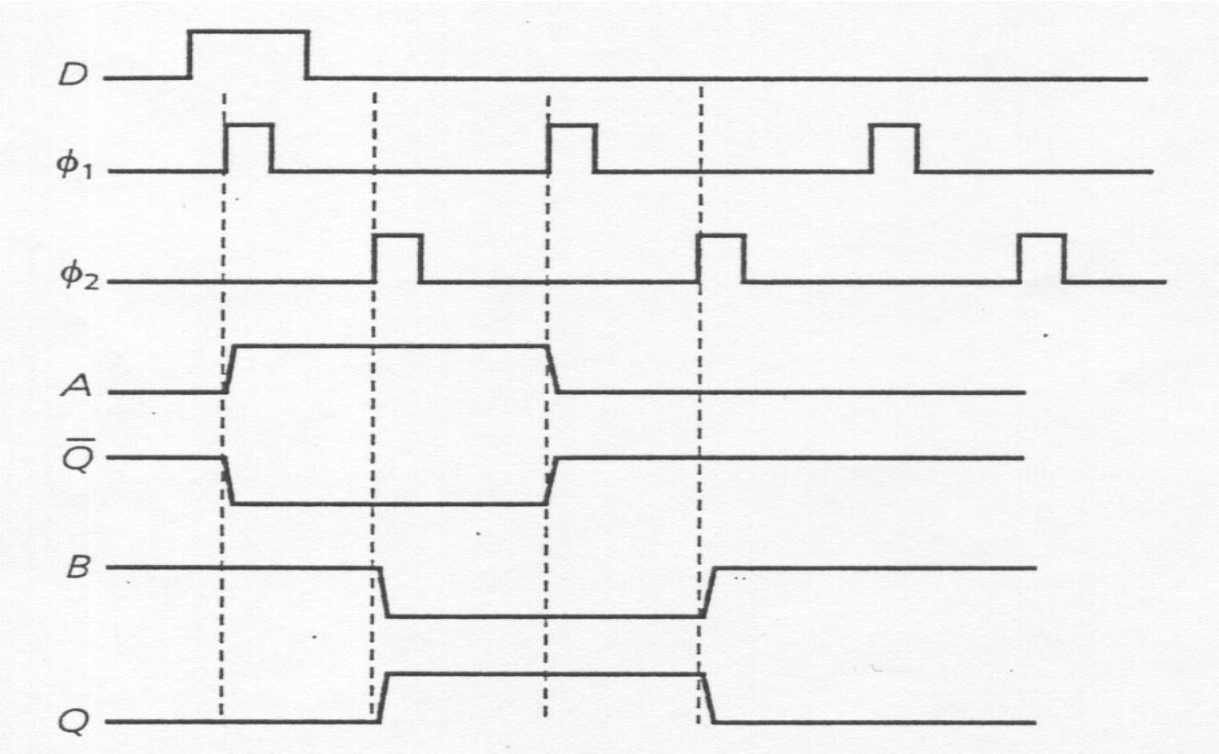
Latch dinamici



Flip-flop tipo D



Flip-flop tipo D



Vedere:

- Paolo Spirito, “Elettronica Digitale”, Ed. McGraw-Hill
  - Cap. 11