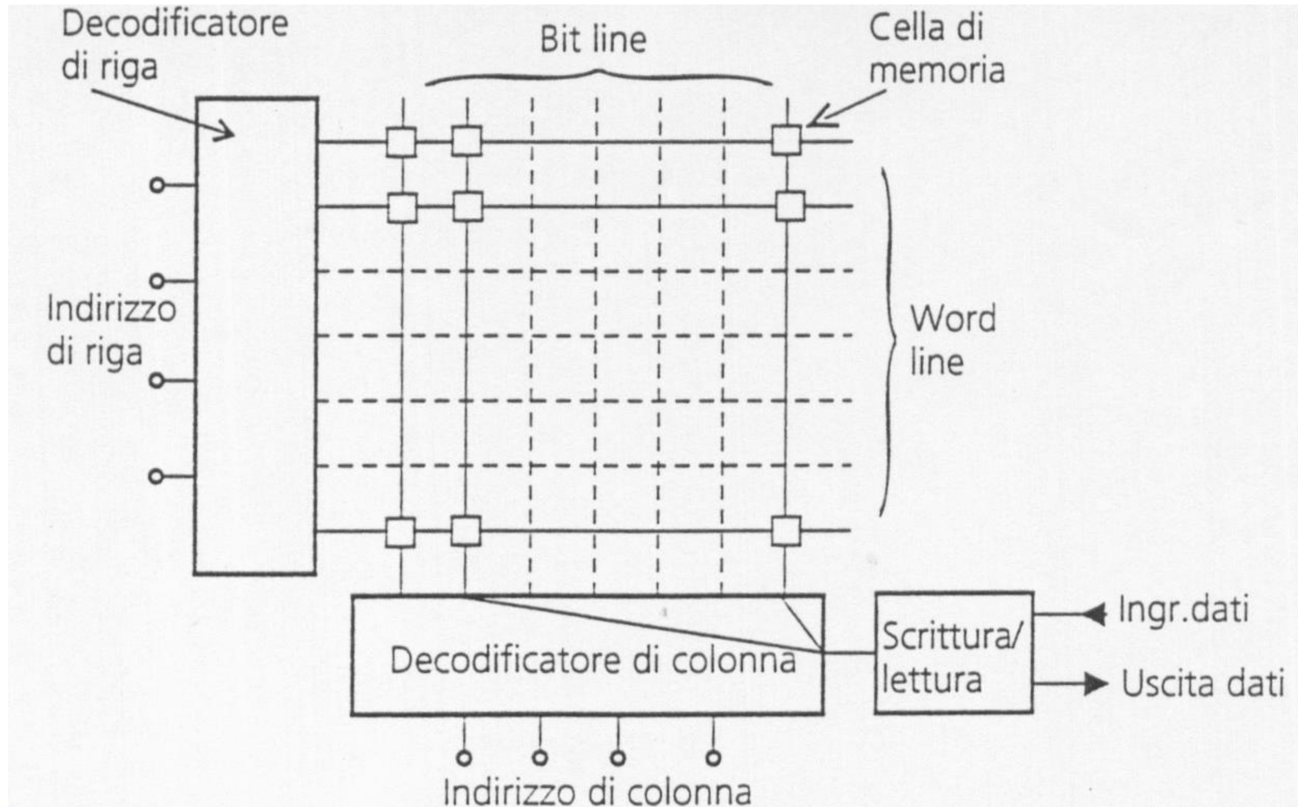
Le memorie RAM

A.Carini – Elettronica digitale

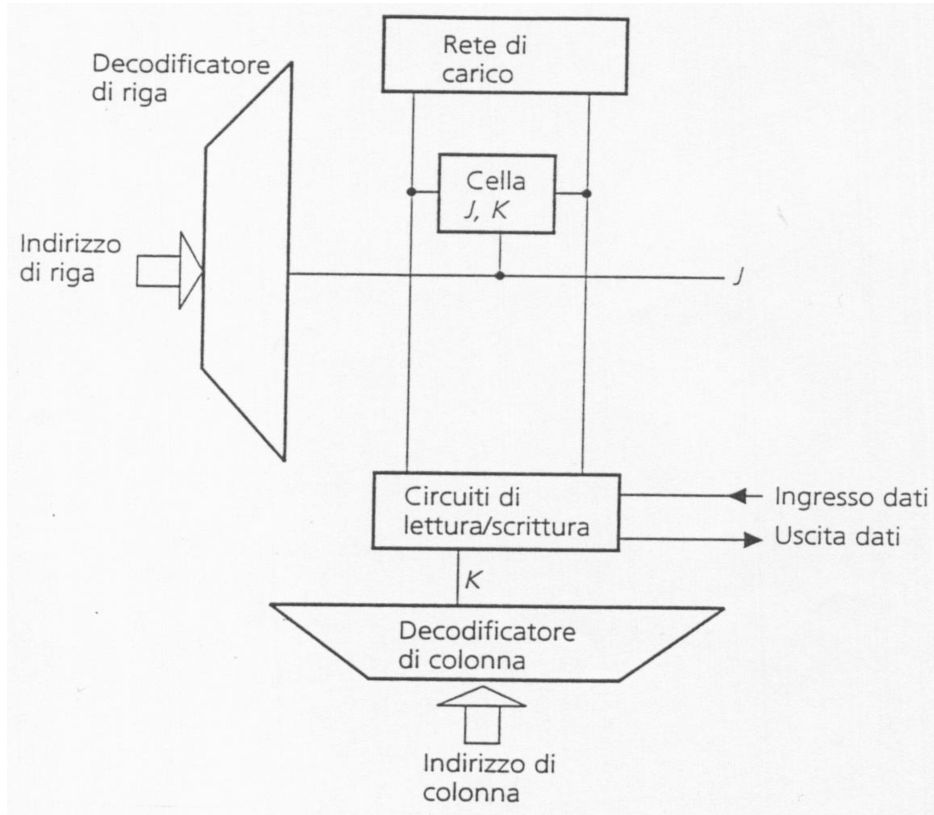
Schema generale



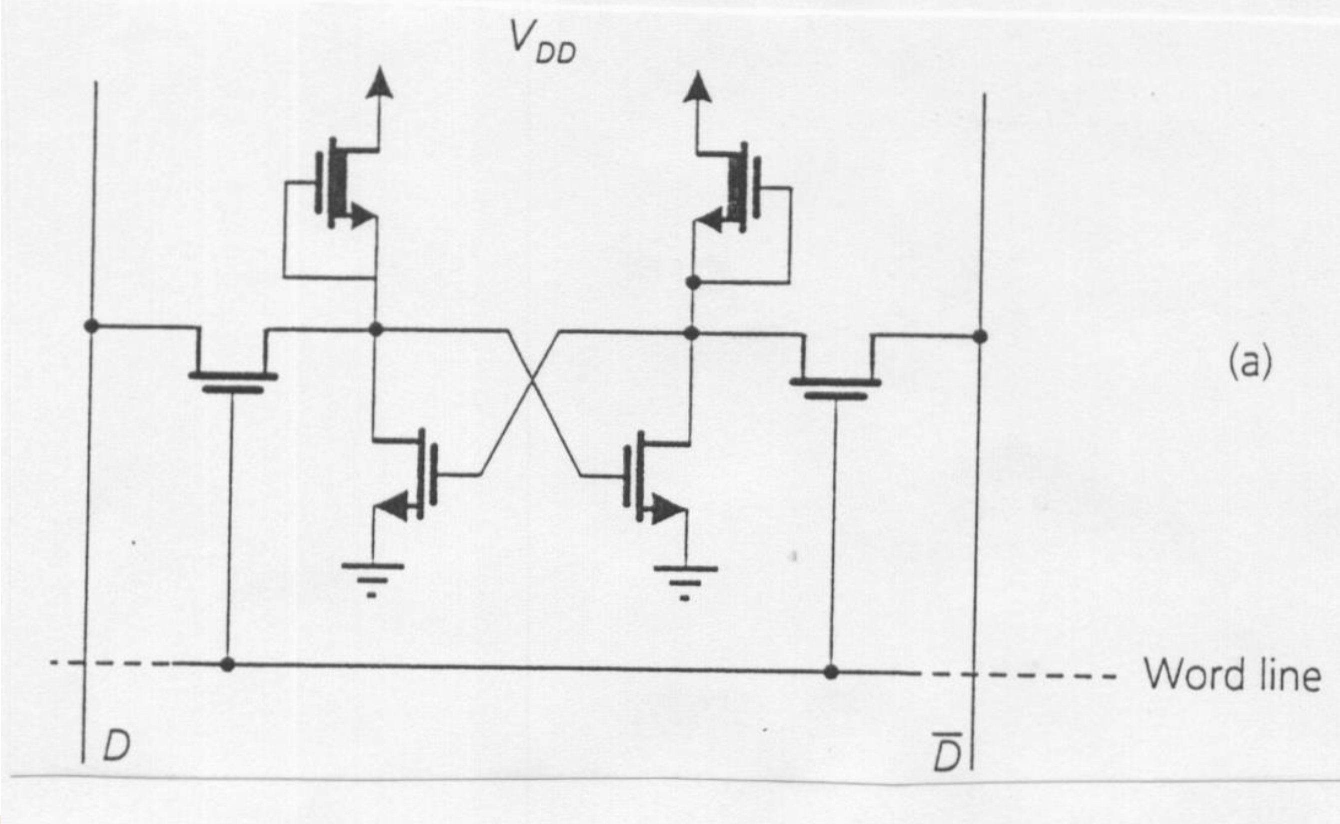
RAM da 64 Kbit

- Indirizzabile con parole da 16 bit
- 8 bit per le righe, 8 per le colonne
- Decodificatori di riga e di colonna(da 8 a 28) richiedono 8 x 256 = 2048 dispositivi
- Amplificatori di lettura / scrittura sono 256
- Celle di memoria sono 65536 !!!

Connessione delle celle elementari



Celle in tecnologia MOS



Celle in tecnologia MOS

- Consideriamo memoria da 128 Kbit
- Package dual in line che dissipa 320 mW

$$P_d = \frac{320\,10^{-3}}{128\,10^{3}} \cong 2.5 \cdot 10^{-6}\ W / cella$$

$$V_{DD} = 5\ V$$

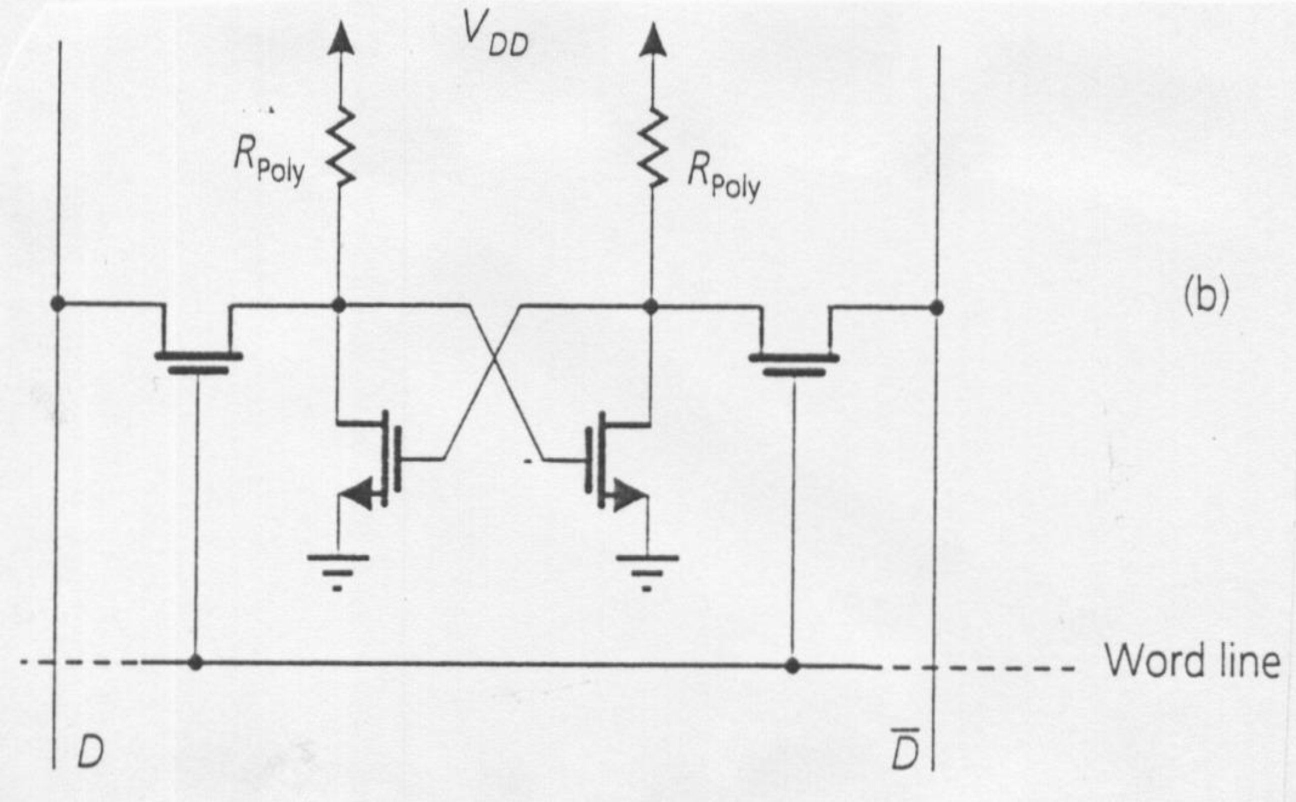
$$P_d = V_{DD}\ I_L$$

$$I_L = \frac{2.5}{5} 10^{-6} A = 0.5\ \mu A$$

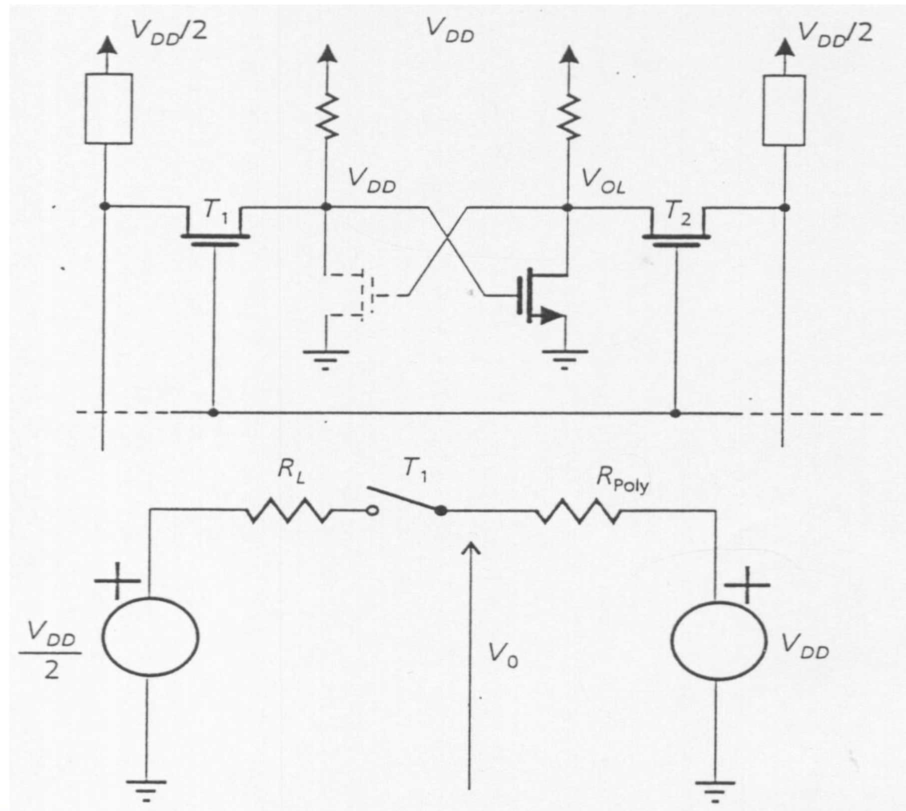
Celle in tecnologia MOS

- Con un carico attivo dovremmo avere W/L<10^{-2} quindi delle lunghezze di canale inacettabili.
- Il carico per questo motivo viene realizzato in polisilicio non drogato, che può assumere valori di resistenza di strato di $10^6 \div 10^8$ Ω/quadro
- Per realizzare una resistenza di 10 MΩ con una resistenza di strato di 5 MΩ/quadro bastano due soli quadri.

Celle SRAM in tecnologia MOS



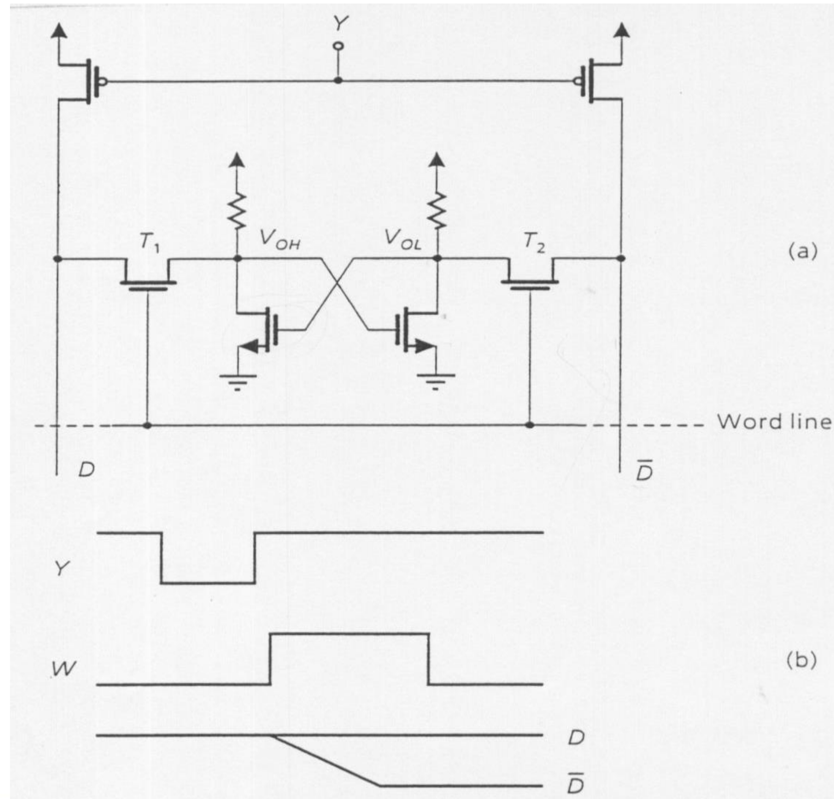
Ipotesi per la lettura



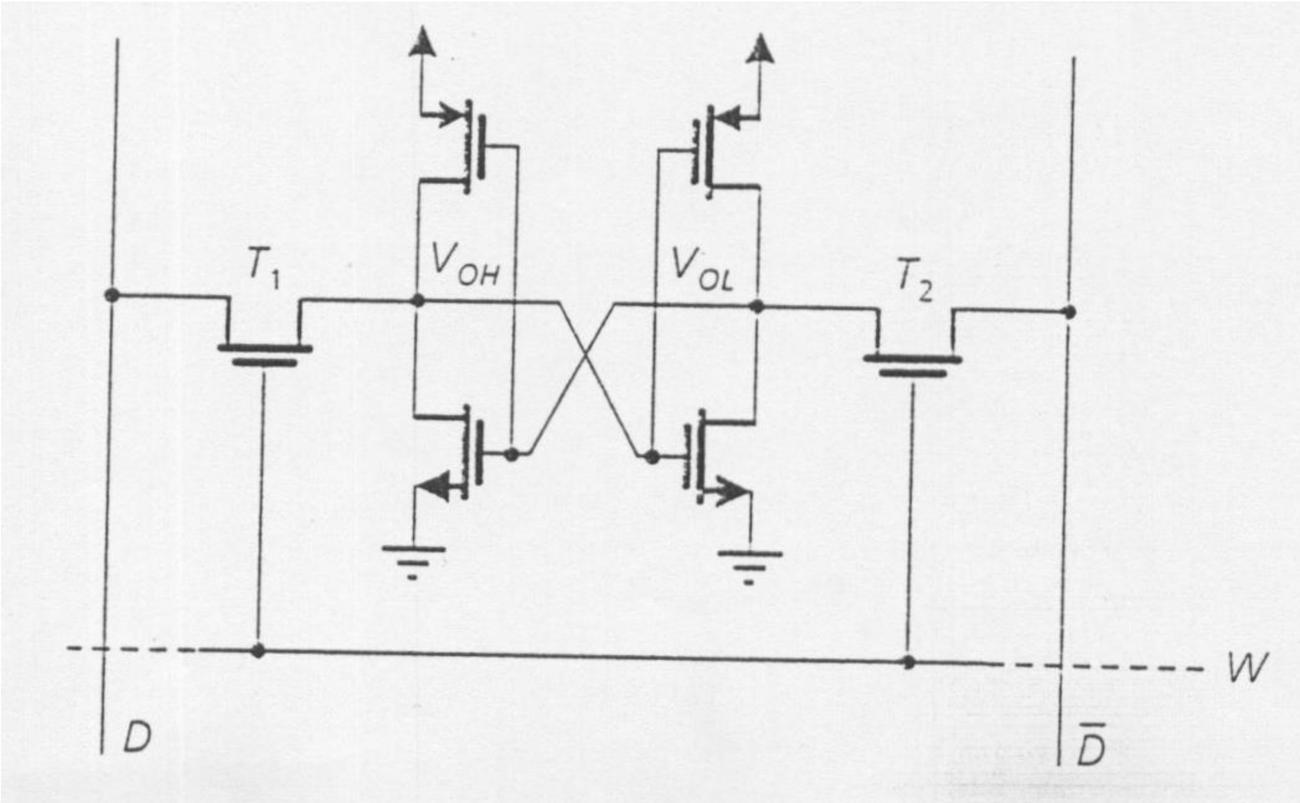
Ipotesi precarica della linea a 0 V

- R_{poly}=10 MΩ
- Chip abbia 1 cm di lato
- Bitline 8mm x 4 µm
- Area della bitline $3.2\ 10^4\ \mu\ m^2$
- t_{OX}=1 µm
- $C_{metal}= 3\ 10^{-5}\ pF / \mu\ m^2$
- $C_{TOT}= 3\ 10^{-5}\ 3.2\ 10^4 \approx 1\ pF$
- $T = R_{poly}\ C_{TOT} = 10\ \mu\ s$ che è inacettabilmente lungo

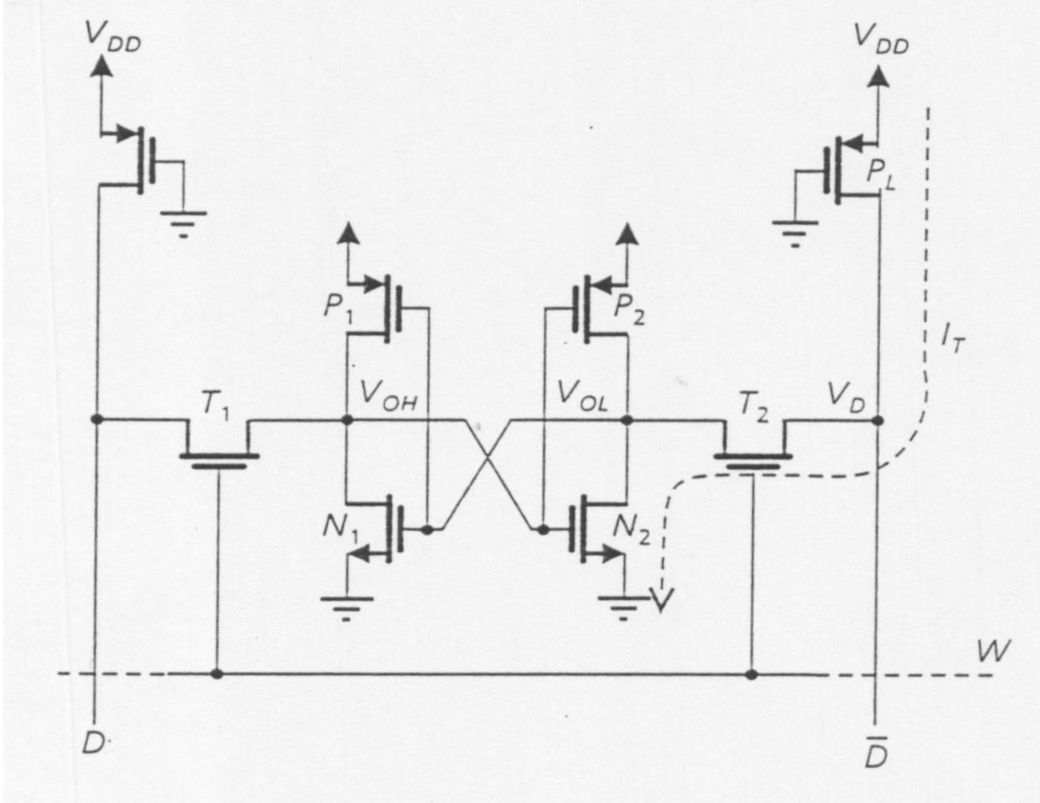
Rete di precarica



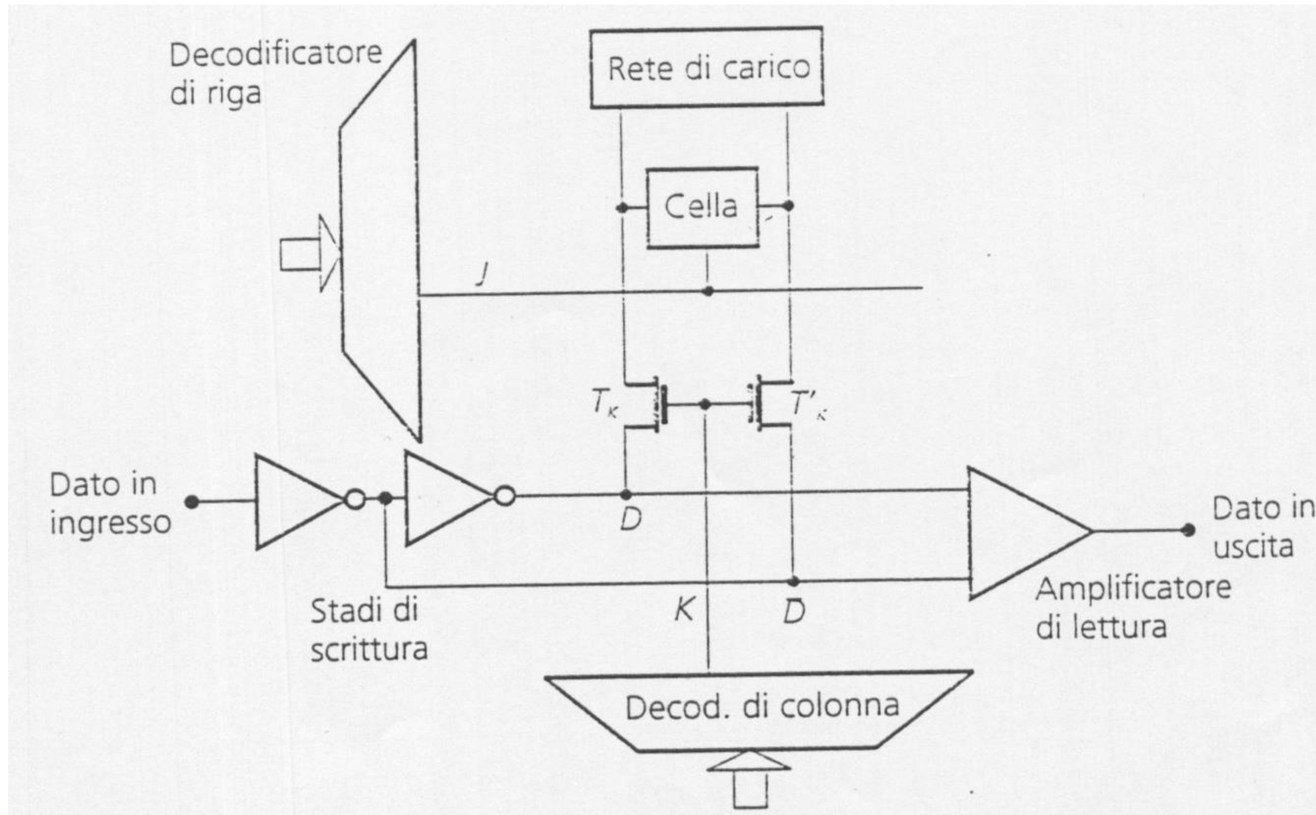
Cella SRAM CMOS



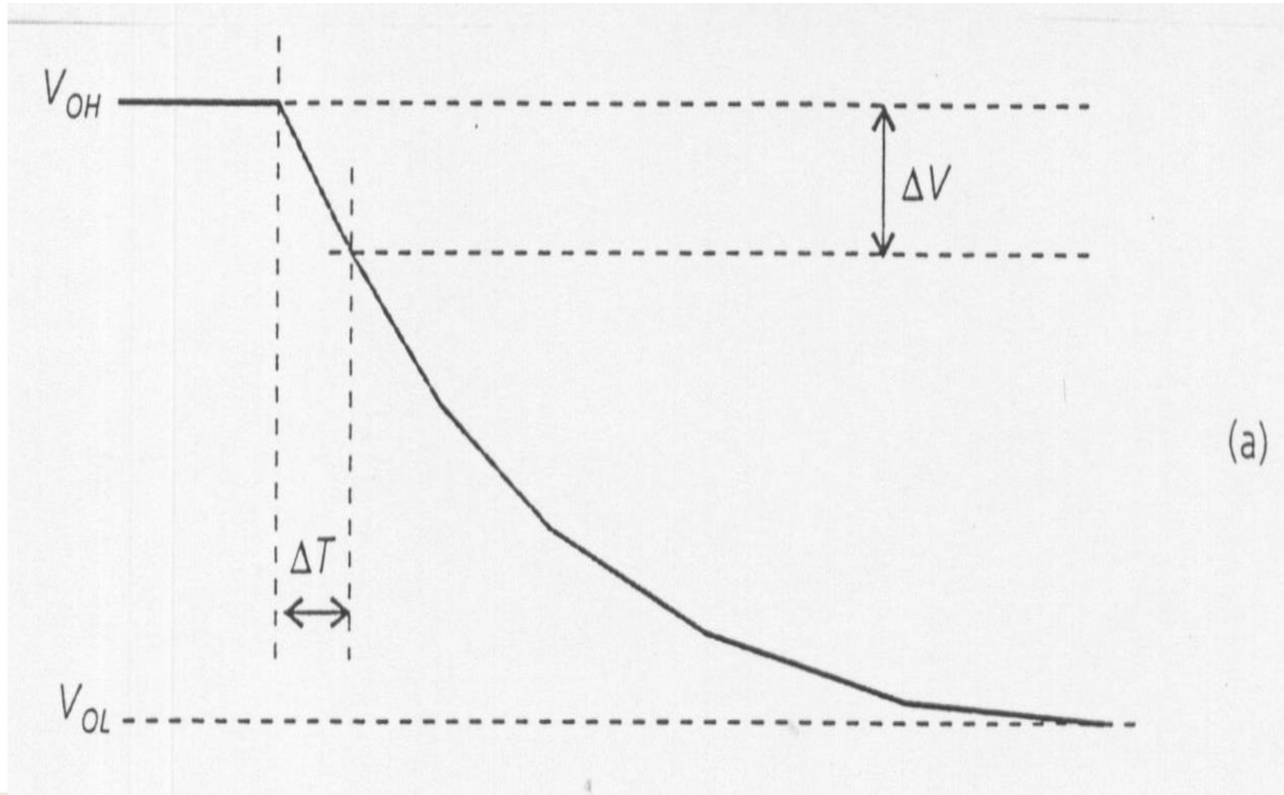
Cella SRAM CMOS



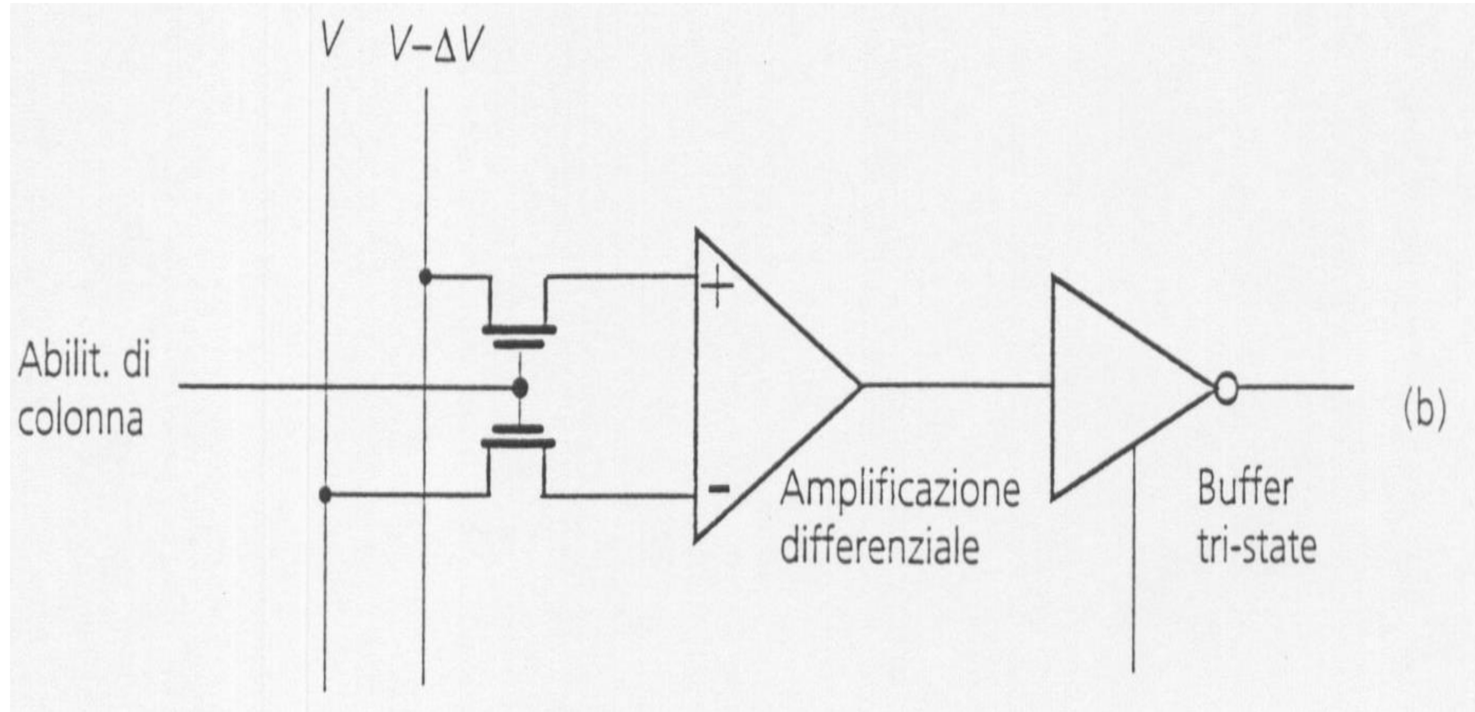
Circuiti di lettura e scrittura



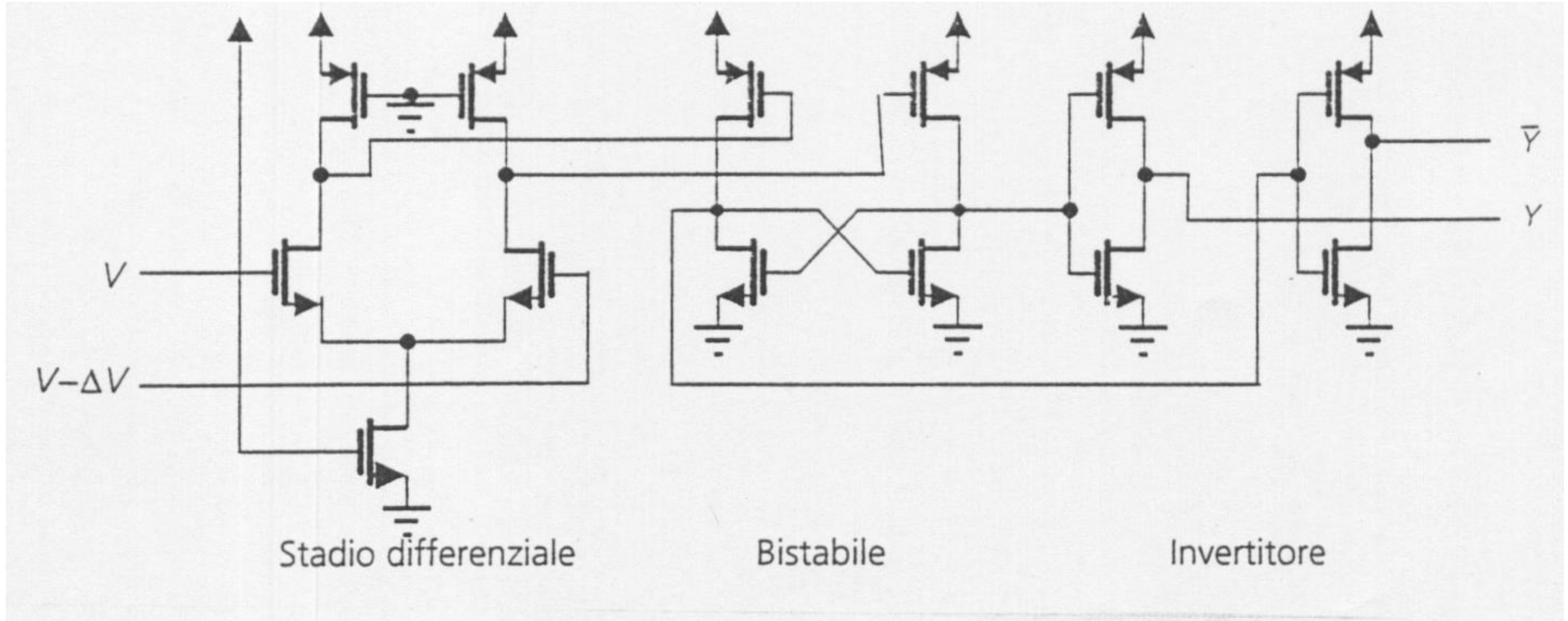
Amplificatore di lettura



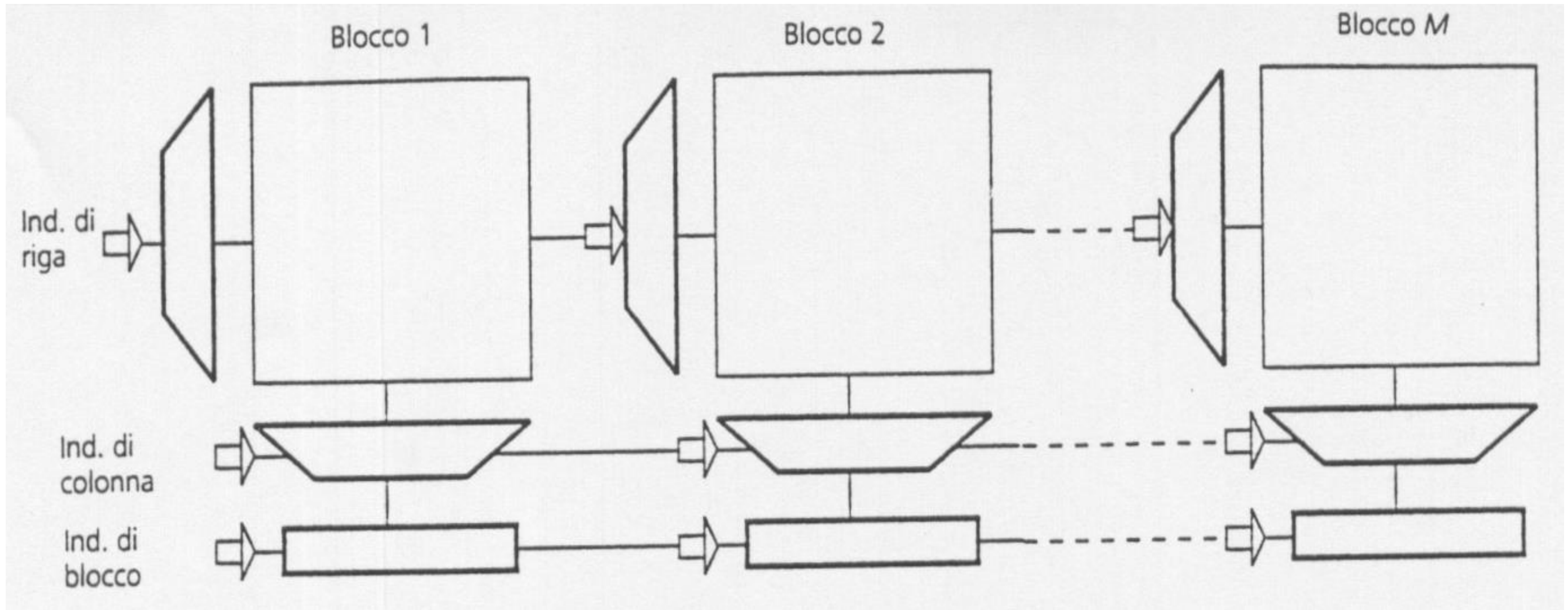
Amplificatore di lettura



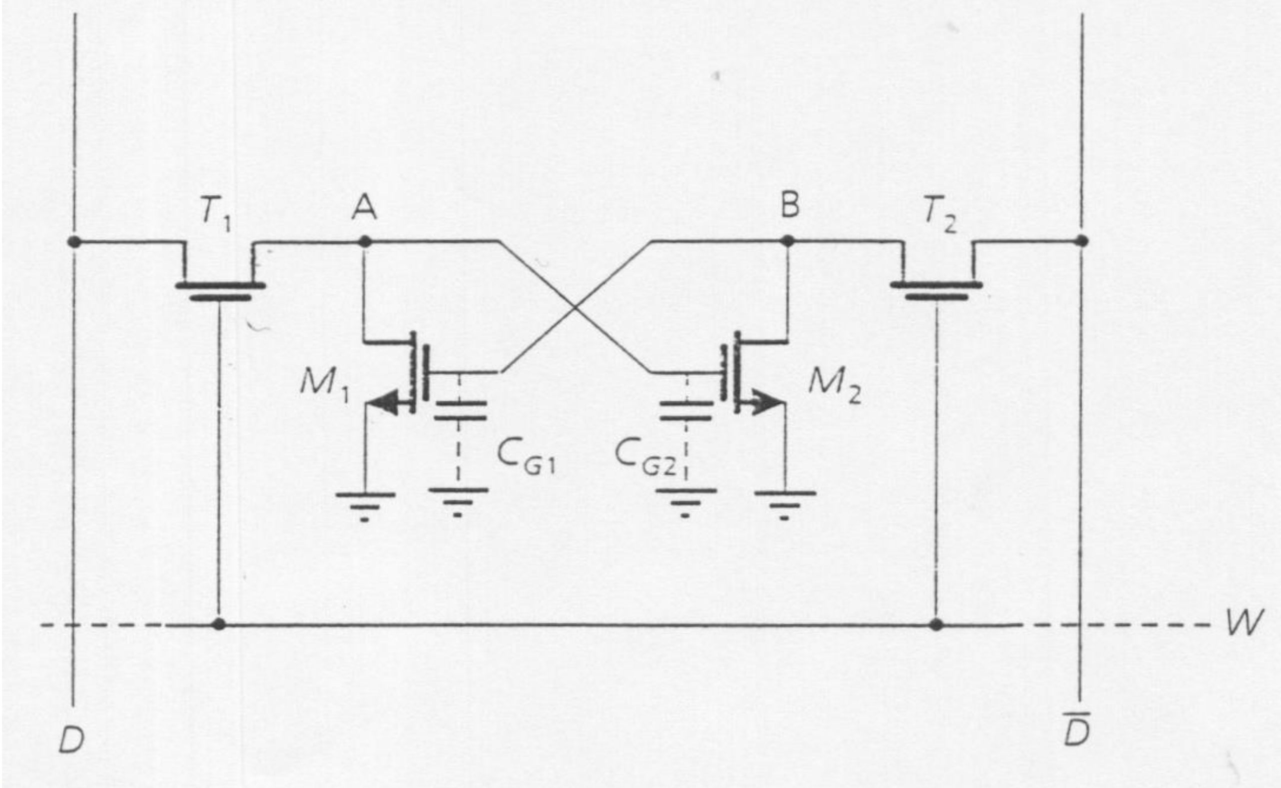
Amplificatore di lettura



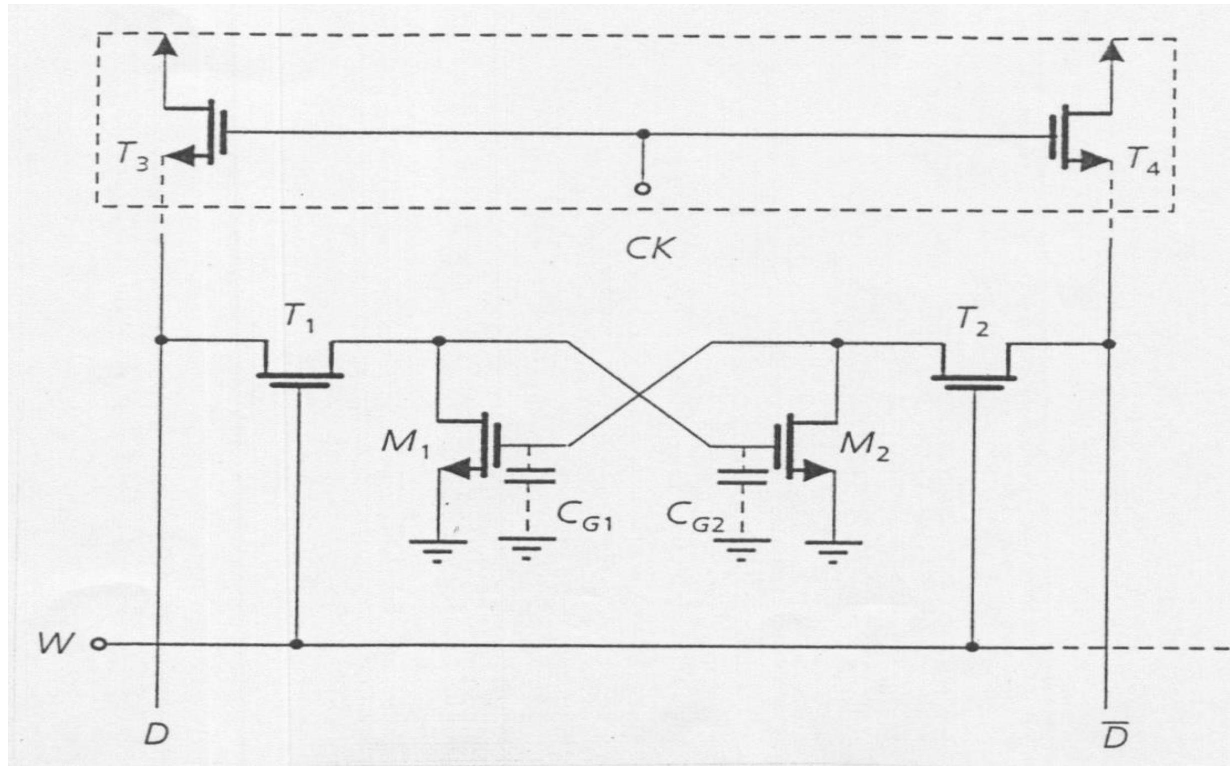
Organizzazione delle RAM



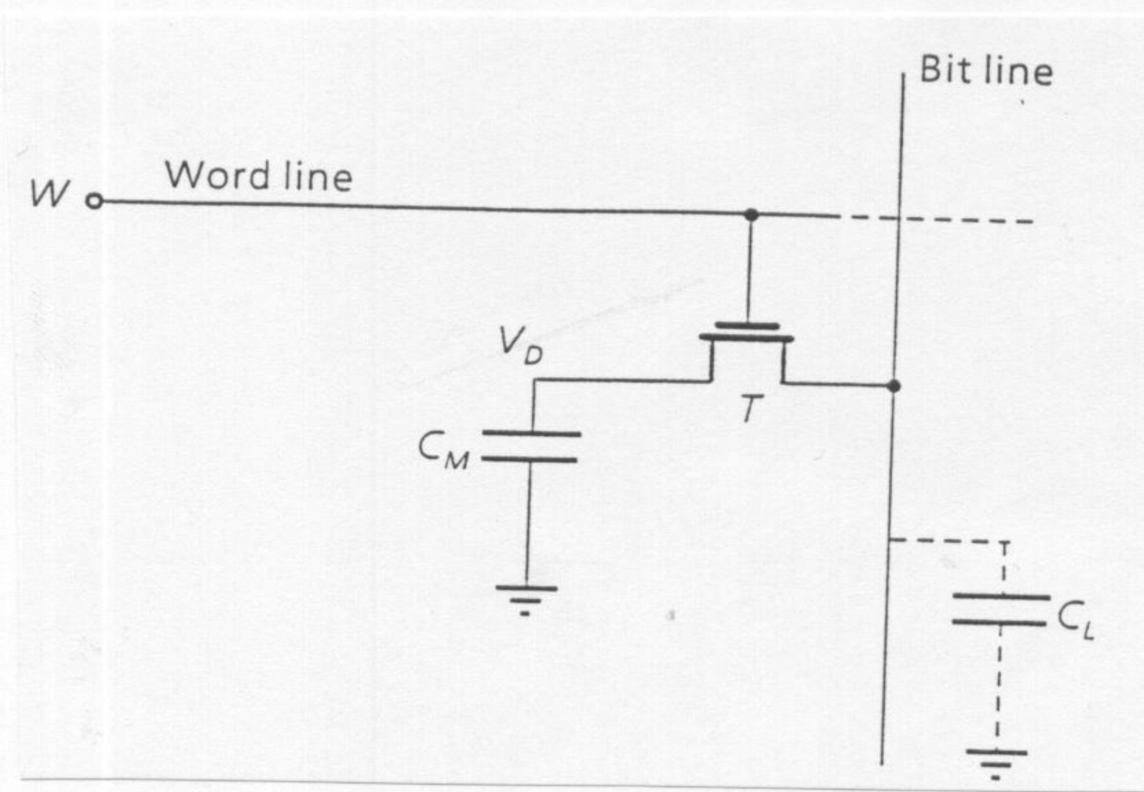
Cella DRAM a 4 transistori



Rete di refresh



Cella dinamica ad 1 transistore



Ridistribuzione della carica in lettura

$$Q = C_L V_R + C_M V_D = V_R'(C_L + C_M)$$

$$V_R' = \frac{C_L}{C_L + C_M} V_R + \frac{C_M}{C_L + C_M} V_D$$

$$\Delta V_R = V_R - V_R' = \frac{C_M}{C_L + C_M}(V_R - V_D)$$

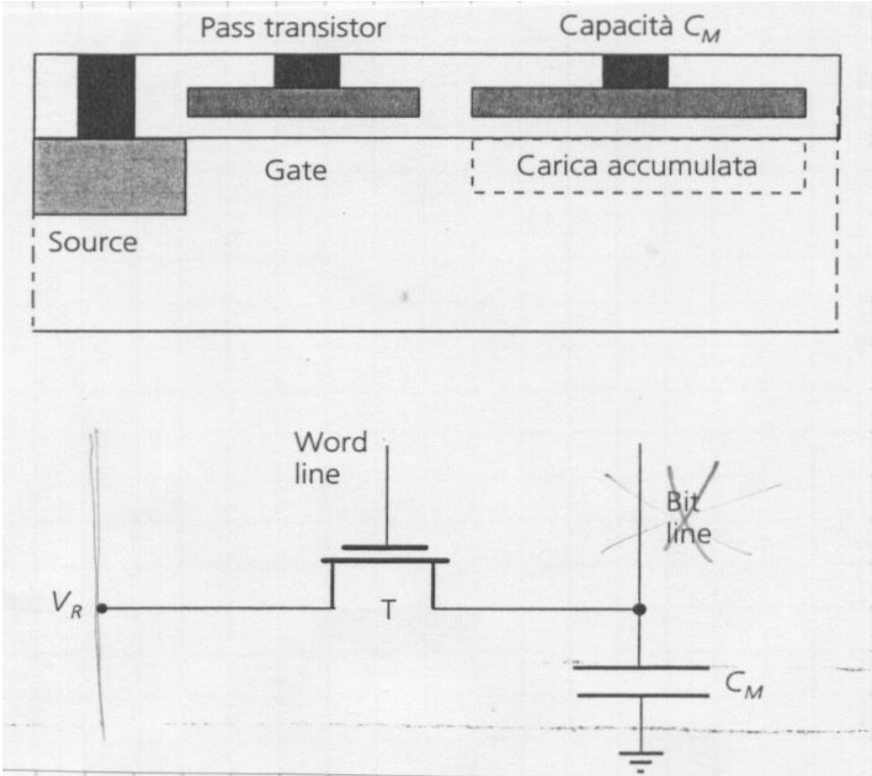
Es:

$$C_M << C_L \qquad C_M = 25\ fF \qquad C_D = 1\ pF$$

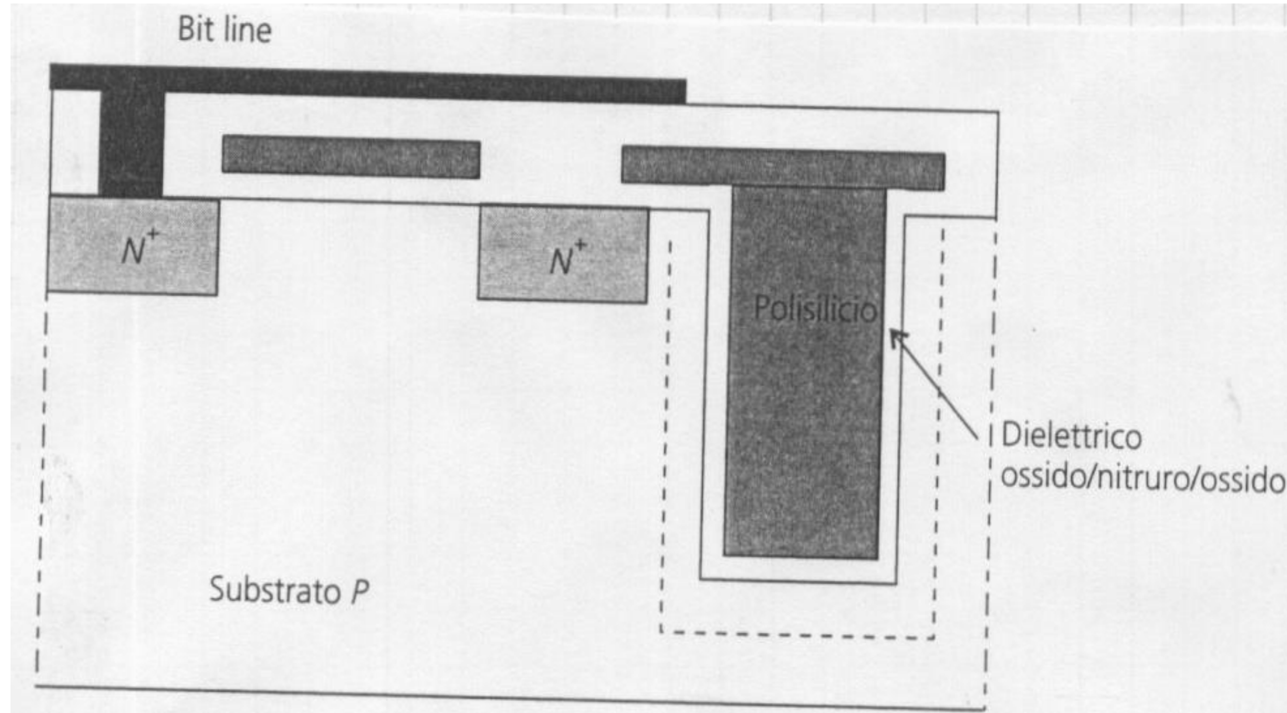
$$V_R = 5\,V$$

$$\boxed{\Delta V_R = 125\,mV}$$

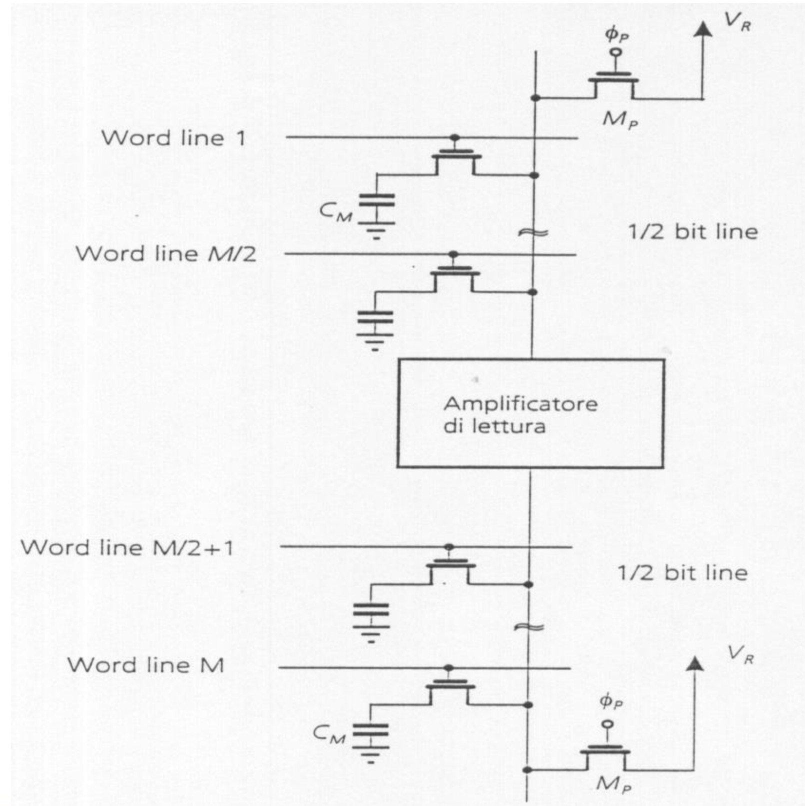
Cella di memoria



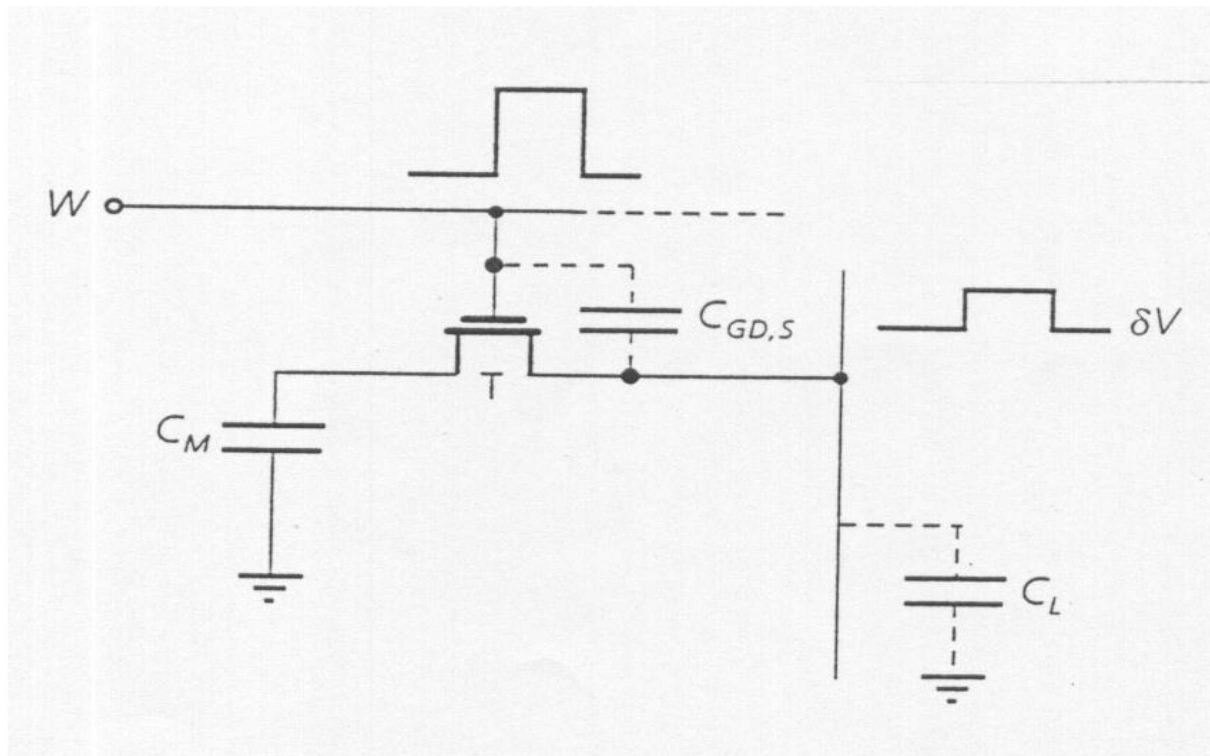
Trench capacitor



Circuiti di lettura per DRAM



Circuiti di lettura per DRAM



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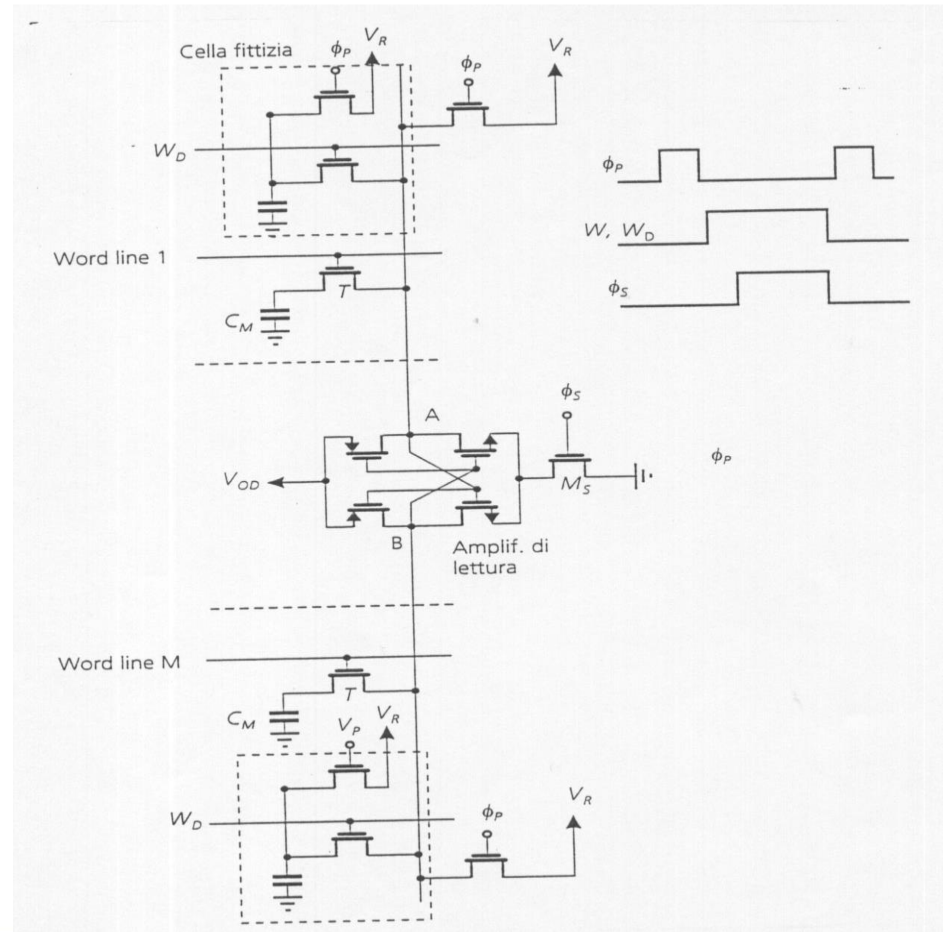
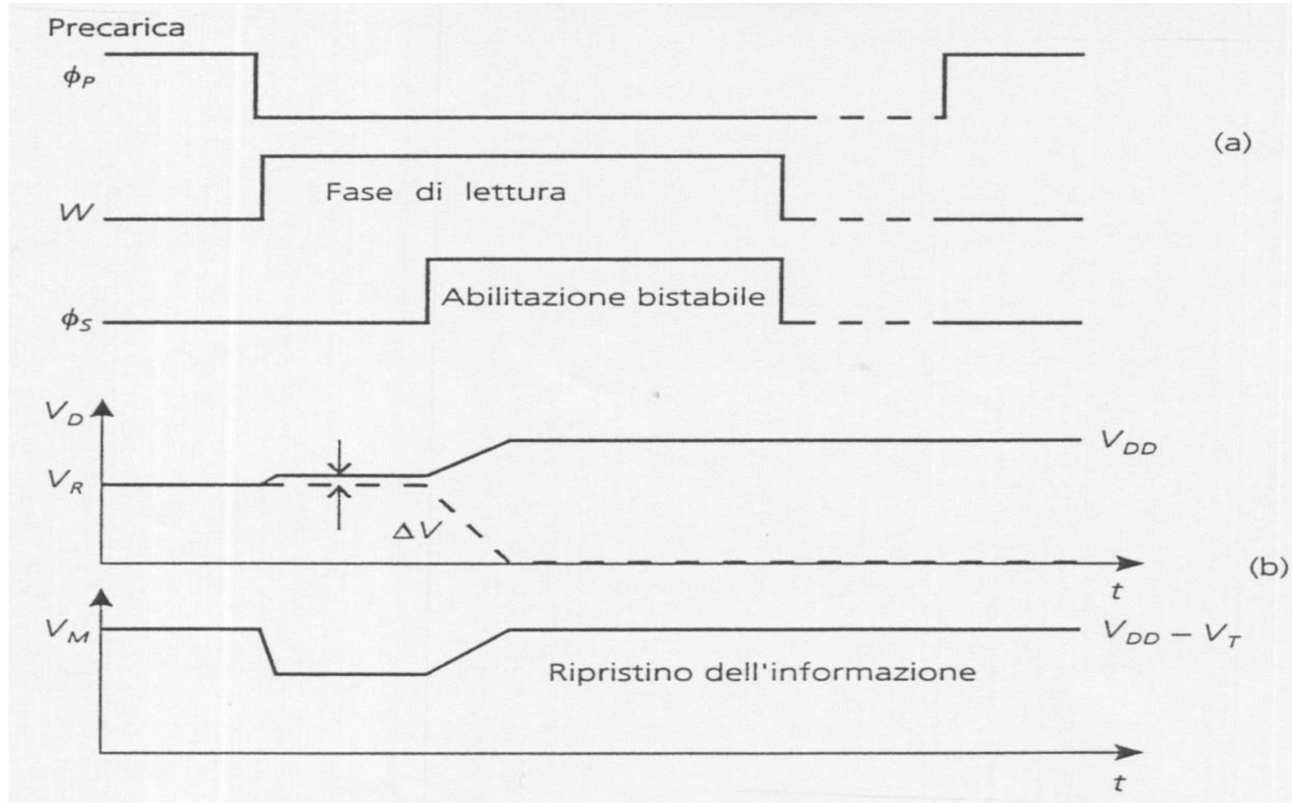
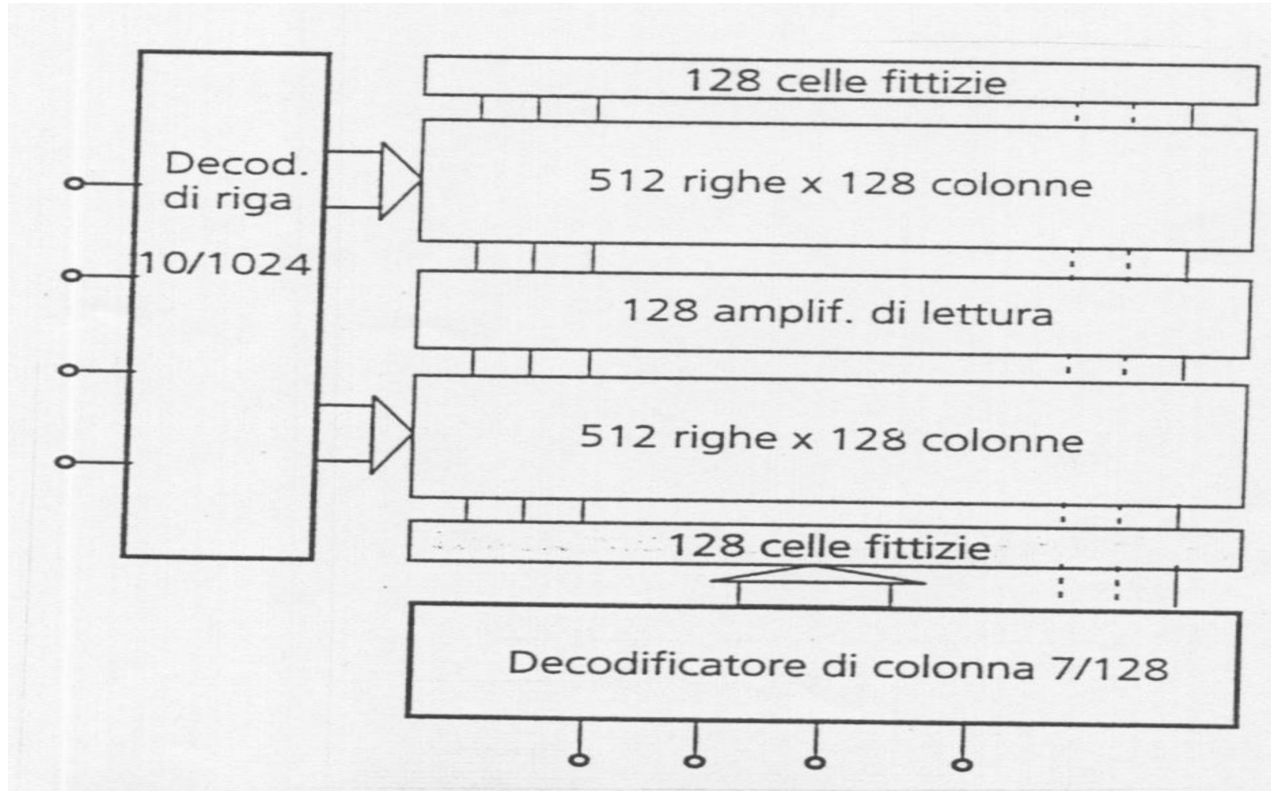


Circuiti di lettura per DRAM



Organizzazione della DRAM



Vedere:

- Paolo Spirito, “Elettronica Digitale”, Ed. McGraw-Hill
  - Cap. 13.4-13.8