



UNIVERSITÀ
DEGLI STUDI DI TRIESTE



Microcontrollers and DSPs

A.Carini – Microcontrollers

Microcontrollers

- A *microcontroller* is a microprocessor optimized for performing tasks of control, temporization, supervision of devices, machinery, industrial processes, i.e. for *embedded control system* applications.
- It is characterized for the availability *on chip* of some essential components:
 - Arithmetic logic unit (ALU)
 - System memory,
 - non-volatile (ROM, Flash) and volatile (SRAM, DRAM).
 - Dedicated peripherals:
 - Analog to digital and digital to analog converters (ADCs and DACs)
 - Timers and counters for time interval measurements
 - Digital modulators (mainly PWMs)
- Microcontrollers are designed for providing reduced complexity, low power dissipation, and low cost.

Microcontrollers

- Microcontrollers are used in automation, automotive, electrical power drives, and in any measurement system.
- Thanks to the great variety of microcontrollers available on the market, designers can always choose the most suitable component for their applications, reducing processing power, memory, and peripherals to what is strictly necessary for the problem at hand.
- There exist microcontrollers with ALU from 4 bits till 32 bits word-length, with different packages, and flexible peripherals.

Microcontroller peripherals

- Most common peripherals:
 - ADCs and DACs, with different number of bits and sampling frequencies.
 - Timers, counters, PWM modulators.
 - Parallel and serial communication interfaces, with both synchronous and asynchronous serial interfaces.
 - Management modules for bus communications, as I2C, SPI, and controller area network (CAN) bus.
 - External memory interfaces towards ROM, EEPROM, and Flash memories.
 - Power management unit (PMU) for the optimization of the power consumption.

Digital signal processors (DSPs)

- A DSP is a microprocessor optimized for efficiently performing in real-time the operations required by digital signal processing.
- It is characterized by high processing power, and at the same time by a low cost compared to a general purpose processor having the same performance.
- In these devices, used for embedded control systems, particular attention is devoted to the reduction of the power dissipation.
- Common characteristics of DSPs:
 - Availability of a multiplier in the CPU to allow multiply and accumulate (MAC) operations.
 - Capability of multiple memory accesses in the same clock cycle.
 - Specific addressing modes for vectors, circular addressing, and other data structures.
 - Availability of devices for the efficient management of peripherals (DMA).

Digital signal processors (DSPs)

- They are principally used for signal processing :
 - Modulation/demodulation, spectral analysis, FIR and IIR filtering,
 - Coding and decoding
 - Compression and decompression
 - Encryption and decryption
- Applications go from:
 - Audio processing,
 - Image and video processing,
 - Telecommunication
- Employed in many common use products (smartphones, TV, hi-fi, ...)
- There is a significant overlap between the applications of microcontrollers and DSPs.

Microcontrollers vs DSPs

- Traditionally, microcontrollers were employed almost exclusively for control, process supervision, and man-machine interface. Their processing power was quite limited since CPUs were with 8 (even 4) bits and did not have a multiplier.
- Consequently, for signal processing only DSPs were used, which could count on 16, 24, 32 bit CPUs. But these in turn were costly and did not have the peripherals needed for control and interface applications.
- Thus, there was a clear role division of these devices.
- Nowadays, thanks to the continuous development of digital technologies and the cost reduction in microprocessor fabrication, this division is more nuanced.
- Current DSPs include many of the peripherals of microcontrollers.
- At the the same time, many microcontrollers offer processing powers similar to DSPs.

Microcontrollers vs DSPs

- Nowadays, the market shares of microcontrollers and DSPs at 32 bits have exceeded those of 8 and 16 bit.
- Cost and performance of microcontrollers and DSPs are for many applications equivalent.
- A novel category of processors is emerging capable of performing control and/or real-time signal processing, the *Digital Signal Controller (DSCs)*.
- DSCs offer high processing powers, with arithmetic units having 16 or more often 32 bits, hardware multipliers, and sometime floating-point ALUs, but includes also timers, counters, PWM modulators with high resolutions.

DSCs

Tabella 1.1: Principali venditori e caratteristiche di alcuni DSC disponibili sul mercato

Venditore	Chip	Flash [kbyte]	Clock [MHz]	Canali PWM		
				N°	Risoluzione	
Microchip	DSPIC30F	6-144	30	4-8	16 bit,	1 ns
	DSPIC33F	12-256	40	18	16 bit,	12.5 ns
	DSPIC33E	64-512	70	16	16 bit,	8.32 ns
Texas Instruments	TMS320F28x	32-512	60-150	16	13 bit,	150 ps
	TMS320LF240x	16-64	40	7-16	11 bit,	150 ps
NXP (ex Freescale)	MC56F83x	48-280	60	12	15 bit,	10 ns
	MC56F80x	12-64	32	5-6	15 bit,	10 ns
	MC56F81x	40-572	40	12	15 bit,	10 ns
STM	STM32F41x	512-2000	100	10	16 bit,	10 ns
	STM32F334x	64-256	72	10	16 bit,	217 ps
	STM32F21x	128-1000	120	12	16 bit,	8.32 ns
	STM32F10x	768-1000	72	10	16 bit,	14 ns
	STM32F03x	16-256	48	6	16 bit,	21 ns

The choice of a microprocessor

- The choice of the device is influenced by many factors:
 - Cost of the device (depending also on volumes),
 - Design cost (e.g., time to market, availability of an IDE (integrated development environment), ...)
 - Performance needed by the application.
 - Necessary peripherals.
 - Operation conditions (maximum power dissipation, working temperature,...)

Processing power measurement

- The processing power of a processor can be evaluated in the most simple and direct way *measuring the time necessary to execute a program*.
- In microcontrollers and DSPs, the *response time* of a program almost often coincides with the *runtime* (also called *execution time* , *CPU time*) dedicated by the processor to execute the instructions that compose the program.
- In general purpose processors, the two times do not coincide: The *operative system* manages different tasks (*multi-tasking*) simultaneously in *time-sharing*.
- The runtime can be a priori estimated with the following formula

$$T_{calcolo} \cong T_{clock} \cdot \sum_{i=1}^{N_{CL}} N_i \cdot NC_i$$

where T_{clock} is the clock period, N_i is the number of instruction of class i , NC_i is the number of clock cycles of the instructions of class i , N_{CL} is the classes number.

Processing power measurement

- Processing power can be increased *reducing the clock period*, but the solution increases the *power dissipation*.
- The number of instructions of a program depends on the processor *architecture*, meaning all the resources available to the programmer, i.e. instructions of the assembly language, data addressing modes, etc..
- The same architecture can be implemented at circuit level in different ways.
- The number of cycles of an instruction varies according to the control logic, which could be *micro-programmed, cabled, pipelined*, and with parallelism.
- Architectures with complex instruction sets (CISC) require long cycle times for the instructions. Architectures with reduced instruction sets (RISC) require shorter cycle times, also as short as a clock period, but often require more instructions for a single operation of CISCs.
- Performance depends on both *logic architecture* and *circuit organization*.

Benchmarking

- Benchmarking with a sample program is often used to evaluate general purpose processors.
- The technique is applied also to DSPs and DSCs, but less frequently to the most simple microcontrollers.
- The sample programs are typical algorithms for DSP applications (i.e., FFTs, FIR and IIR filters, ...), not full applications as in general purpose processors.
- For DSPs we talk about *kernel benchmarking*, which must provide
 - Strong relevance with regards to DSP/DSC applications,
 - Detailed and unique definition of the algorithm implemented (e.g. FFT),
 - Maximum simplicity,
 - High degree optimization for the under-test device.

Benchmarking

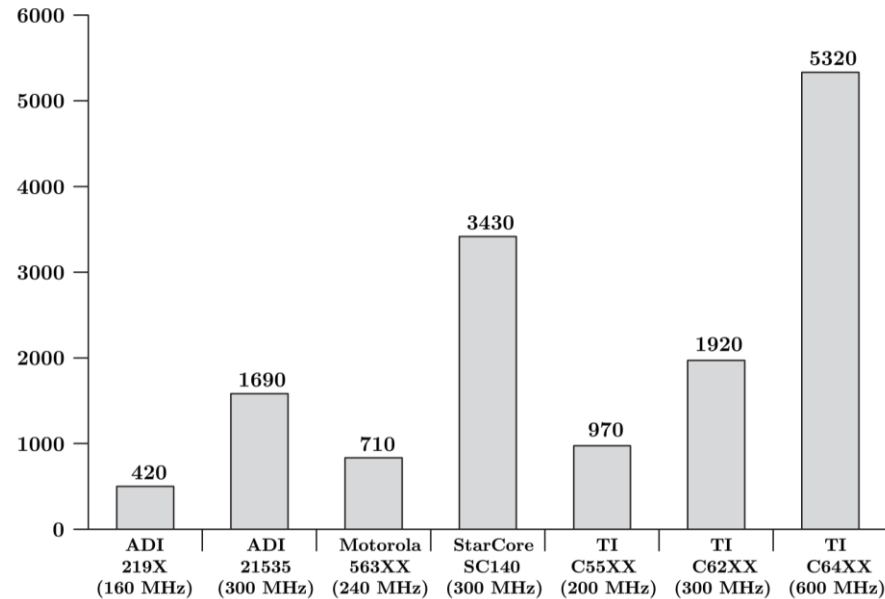


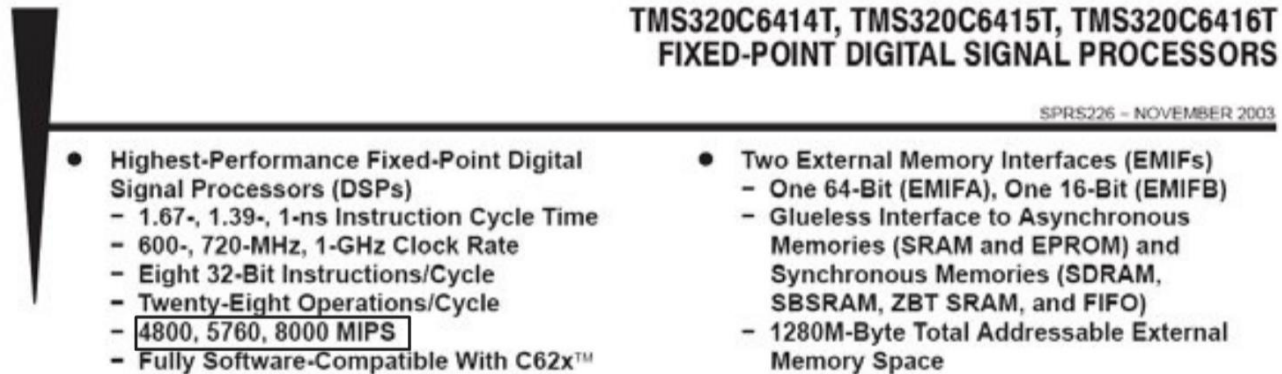
Figura 1.1: Risultati del “kernel benchmarking” di alcuni DSP secondo la società di analisi *Berkeley Design Technology, Inc.*. Un indice più elevato corrisponde a maggiore velocità nell’esecuzione dei codici di prova.

Performance indexes

- *MIPS*: millions of instructions per second.
- *DMIPS*: millions of instructions per second for a specific benchmark algorithm, called Dhrystone;
- *CoreMark*: performance index obtained from the execution of a combination of standard algorithms (including research and sorting, matrix manipulation, string recognition, CRC,...).
- *FLOPS*: millions of floating points operations per second.

- All these indexes are unreliable: they consider only the maximum number of operations that can be performed without specifying conditions.
- They simply allow a comparison of performance within the same family.

Performance indexes



**TMS320C6414T, TMS320C6415T, TMS320C6416T
FIXED-POINT DIGITAL SIGNAL PROCESSORS**

SPRS226 – NOVEMBER 2003

- **Highest-Performance Fixed-Point Digital Signal Processors (DSPs)**
 - 1.67-, 1.39-, 1-ns Instruction Cycle Time
 - 600-, 720-MHz, 1-GHz Clock Rate
 - Eight 32-Bit Instructions/Cycle
 - Twenty-Eight Operations/Cycle
 - **4800, 5760, 8000 MIPS**
 - Fully Software-Compatible With C62x™
- **Two External Memory Interfaces (EMIFs)**
 - One 64-Bit (EMIFA), One 16-Bit (EMIFB)
 - Glueless Interface to Asynchronous Memories (SRAM and EPROM) and Synchronous Memories (SDRAM, SBSRAM, ZBT SRAM, and FIFO)
 - 1280M-Byte Total Addressable External Memory Space

Figura 1.2: Estratto del foglio tecnico di un DSP di Texas Instruments. Viene indicata la potenza di calcolo massima di 8000 MIPS.

Performance indexes



dsPIC30F

dsPIC30F Enhanced FLASH 16-bit Digital Signal Controllers Motor Control and Power Conversion Family

High Performance Modified RISC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set architecture
- 88 base instructions
- 24-bit wide instructions, 16-bit wide data path
- Linear program memory addressing up to 4M Instruction Words
- Linear data memory addressing up to 64 Kbytes
- Up to 144 Kbytes on-chip FLASH program space
 - Up to 48K Instruction Words
- Up to 8 Kbytes of on-chip data RAM
- Up to 4 Kbytes of non-volatile data EEPROM
- 16 x 16-bit working register array
- Three Address Generation Units that enable:
 - Dual data fetch
 - Accumulator write back for DSP operations
- Flexible Addressing modes supporting:
 - Indirect, Modulo and Bit-Reversed modes
- Two, 40-bit wide accumulators with optional saturation logic
- 17-bit x 17-bit single cycle hardware fractional/integer multiplier
- Single cycle Multiply-Accumulate (MAC) operation
- 40-stage Barrel Shifter
- Up to 30 MIPS operation
 - DC to 40 MHz external clock input

Peripheral Features (Continued):

- Addressable UART modules supporting:
 - Interrupt on address bit
 - Wake-up on START bit
 - 4 characters deep TX and RX FIFO buffers
- CAN bus modules

Motor Control PWM Module Features:

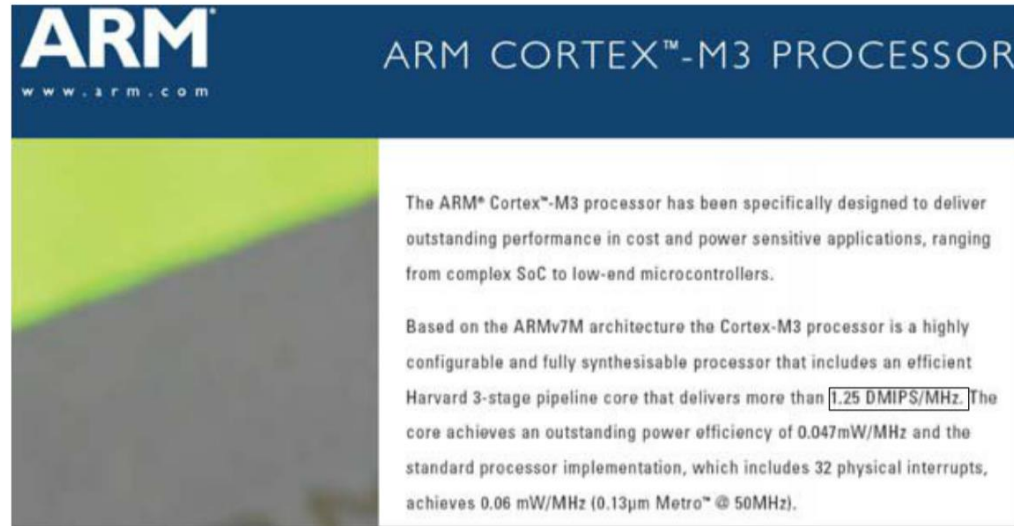
- Up to 8 PWM output channels
 - Complementary or Independent Output modes
 - Edge and Center Aligned modes
- 4 duty cycle generators
- Dedicated time-base with 4 modes
- Programmable output polarity
- Dead-time control for Complementary mode
- Manual output control
- Trigger for A/D conversions

Quadrature Encoder Interface Module Features:

- Phase A, Phase B and Index Pulse input
- 16-bit up/down position counter
- Count direction status
- Position Measurement (x2 and x4) mode
- Programmable digital noise filters on inputs
- Alternate 16-bit Timer/Counter mode

Figura 1.3: Estratto del foglio tecnico di un DSC di Microchip. Viene indicata la potenza di calcolo massima di 30 MIPS.

Performance indexes



The image shows a technical document snippet for the ARM Cortex-M3 processor. It features the ARM logo and the text 'ARM CORTEX™-M3 PROCESSOR'. The document describes the processor's performance in cost and power-sensitive applications, highlighting its efficiency and power consumption. A hand cursor is visible on the right side of the document, pointing to the performance metrics.

ARM
www.arm.com

ARM CORTEX™-M3 PROCESSOR

The ARM® Cortex™-M3 processor has been specifically designed to deliver outstanding performance in cost and power sensitive applications, ranging from complex SoC to low-end microcontrollers.

Based on the ARMv7M architecture the Cortex-M3 processor is a highly configurable and fully synthesisable processor that includes an efficient Harvard 3-stage pipeline core that delivers more than **1.25 DMIPS/MHz**. The core achieves an outstanding power efficiency of 0.047mW/MHz and the standard processor implementation, which includes 32 physical interrupts, achieves 0.06 mW/MHz (0.13µm Metro™ @ 50MHz).

Figura 1.4: Estratto del foglio tecnico di un processore ARM Cortex-M3. Viene indicata la potenza di calcolo di 1.25 DMIPS normalizzati.

Performance indexes

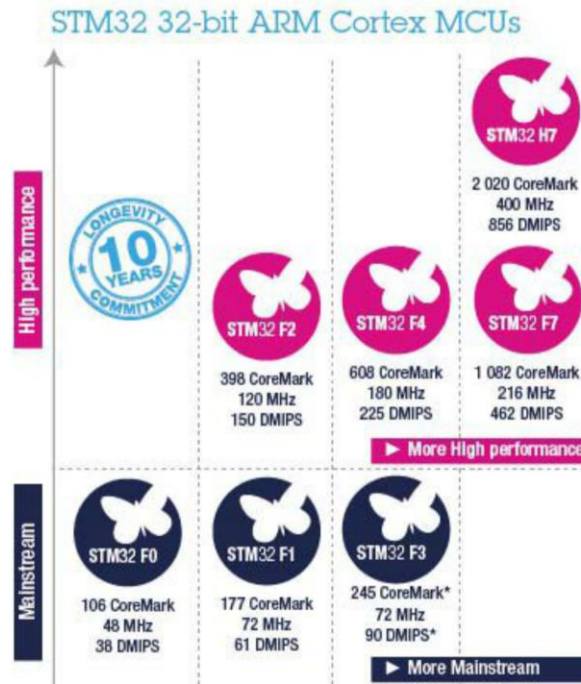


Figura 1.5: Caratteristiche di alcuni DSC di fabbricazione STM. Vengono indicati DMIPS e valori di CoreMark. Si noti la stretta correlazione tra le due serie di valori.

See:

- Simone Buso, «Introduzione alle applicazioni industriali di Microcontrollori e DSP» Società editrice Esculapio, 2018
 - Chapter 1