UNIVERSITÀ DEGLI STUDI DI TRIESTE

dipartimento di ingegneria e architettura

Pulse width modulation

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Modulation and PWM modulation

- The *modulation* is a signal processing technique where the information associated to a signal, called *modulating signal,* exploiting an auxiliary signal called *carrier,* is transferred to a *modulated signal.*
- The modulated signal should have more convenient characteristics for its transmission over the available transmission medium, and is often a power amplified signal.
- In *pulse width modulation (PWM)* the modulated signal is a *square-wave,* of assigned amplitude and frequency, but with *pulse width* which is proportional to the modulating signal.
- In PWM modulation and transmission a high amplification can be easily achieved, simply increasing the levels of the modulated signal.

Analog PWM modulation

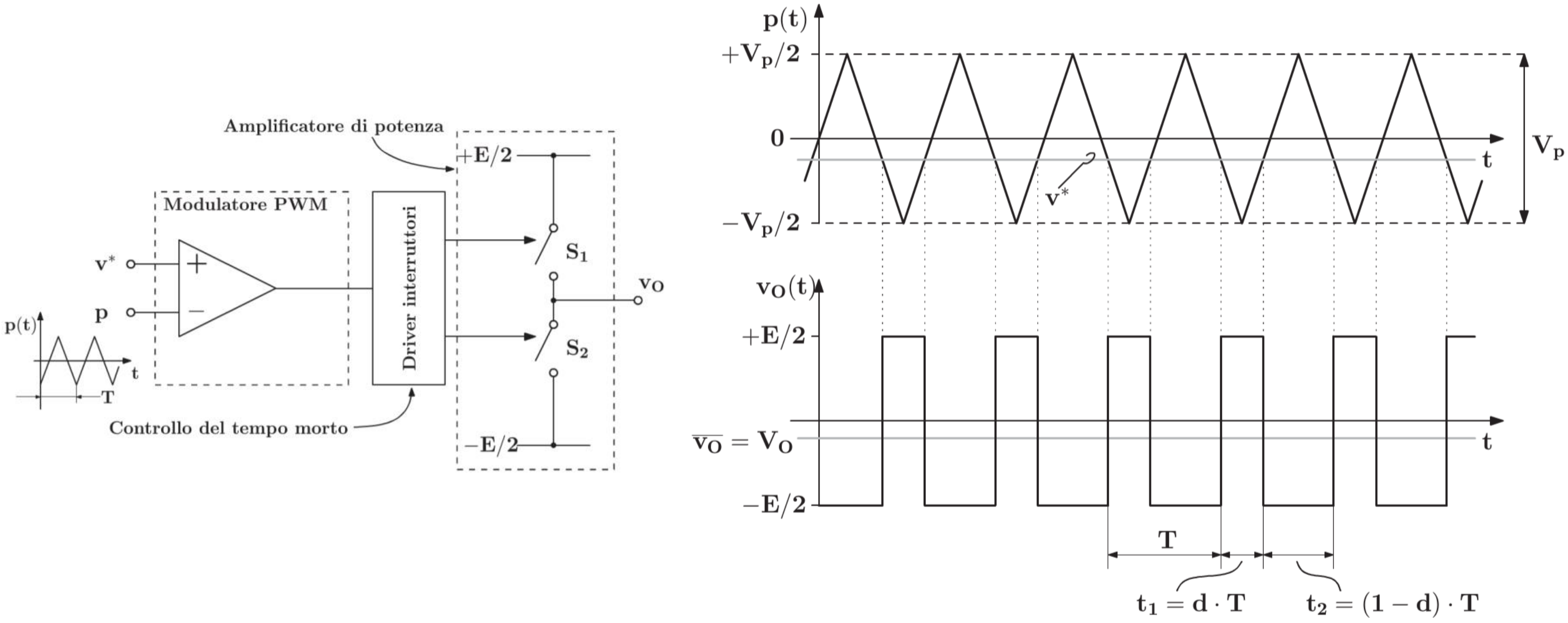


Figura 12.1: Schema semplificato di un modulatore PWM analogico.

Analog PWM modulation

- The modulation is realized by an analog comparator, which compare the instantaneous value of the modulating signal v^*, here constant, with the carrier $p(t)$, which usually is a triangular wave.
- The carrier determines the frequency of the output signal and transfer the information from v^* to the output signal.
- The output stage is just a buffer, which replicates the comparator logic level and provides high output voltage *E/2* and high output currents.
- The intermediate state indicated as *driver* translates the comparator logic level in the activation signals of the two switches and manages the *dead time*, introduced between positive and negative output to avoid the contemporary activity of both switches.

Analog PWM modulation

- The period *T* is the sum of two intervals, t_1 where $v_O(t) = +E/2$, and t_2 where $v_O(t) = -E/2$.
- $d = t_1/T$ is called *duty-cycle* of the modulator.
- The moving average over a period *T* is constant and equal to

$$\overline{v_O}(t) = \frac{1}{T}\int_{t-T}^{t} v_O(\tau)\,d\tau = \left(d - \frac{1}{2}\right)\cdot E = v^* \cdot \frac{E}{V_P}.$$

- The information of the signal v^* has been transferred to $v_O(t)$, proportional to v^*
- By varying t_1 from 0 to T, i.e., *d* from 0 to 1, the average output voltage change from $-E/2$ till $+E/2$.
- v^* does not need to be constant. If it is *slowly varying* we still have:

$$\overline{v_O}(t) = \left(d(t) - \frac{1}{2}\right)\cdot E \cong \frac{E}{V_P}\cdot v^*(t),$$

Analog PWM demodulation

- The spectral properties of PWM modulated signal allow an easy reconstruction of v^*(t).
- Let us consider a sinusoidal modulating signal with frequency f_m much lower than that of the PWM carrier f_{PWM}.
- The spectrum of the modulated signal is given by the spectrum of the original signal plus some periodic repetitions centered around multiples of f_{PWM}.
- The spectrum repetitions fast decay at higher frequencies.
- We have a similar spectrum with any band-limited signal v^*(t), provided the maximum bandwidth is much lower than f_{PWM}.
- The original signal spectrum is embedded in the modulated signal and can be recovered by low-pass filtering the modulated signal.
- To facilitate the extraction f_{PWM} is often 20 to 50 times larger than the modulating signal bandwidth.

Analog PWM demodulation

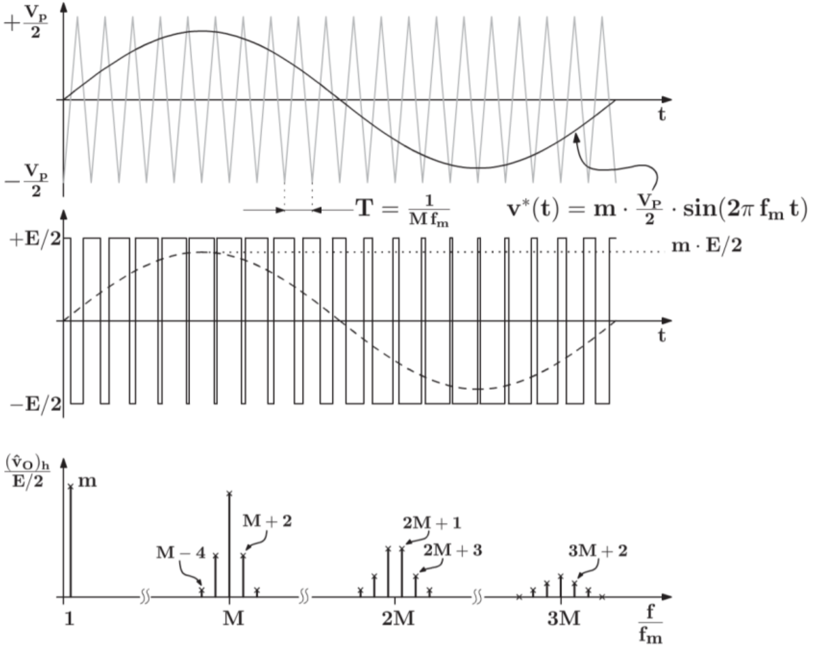


Figura 12.2: Analisi spettrale di un modulatore PWM con modulante sinusoidale a frequenza sottomultipla della frequenza di modulazione.

Analog PWM demodulation

If the carrier signal is not much larger than v^*(t) bandwidth:

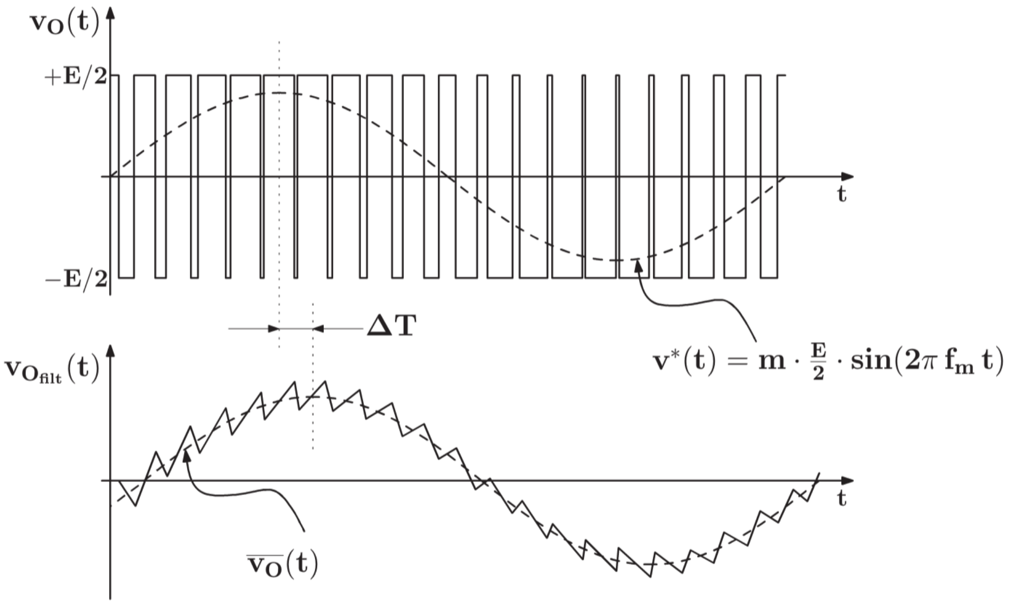


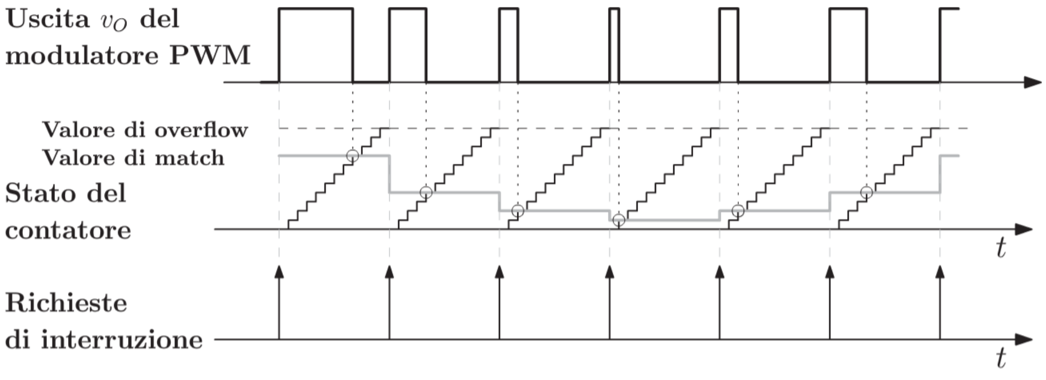
Figura 12.3: Demodulazione con *"ripple"* residuo di un segnale PWM. Si noti lo sfasamento ΔT introdotto dal filtro tra le componenti armoniche fondamentali del segnale modulato e demodulato.

Digital PWM modulation

- The PWM modulation can be implemented also using *digital circuits.*
- The role of the triangular carrier is played by a *binary counter,* the role of the analog comparator is played by a *binary comparator*.
- The binary comparator compares the value of the counter with a *match* value set by the user. The *match* value determines the duty-cycle.
- The *match* value *divided* by the counter *full-scale* value, provides the fraction of period where the output signal is high.
- The process is equivalent to an analog modulation in which the modulating signal level is acquired and quantized every carrier period.
- The counter frequency is equal to the carrier frequency times 2^n, where *n* is the number of bits of the counter. For this reason, it is difficult to have digital modulators with high resolution and high carrier frequency:

$$n = \frac{Log_{10}\left(\frac{f_{clock}}{f_{PWM}}\right)}{Log_{10}2}$$

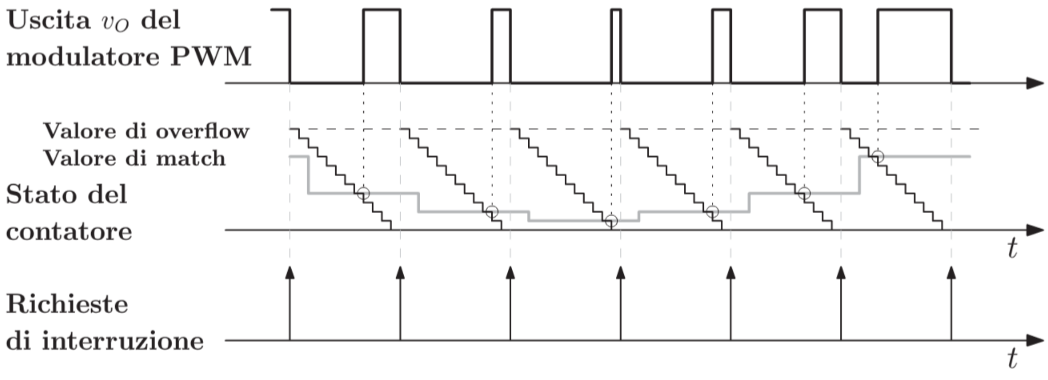
Trailing edge PWM



(a)

- There are many ways for implementing digitals PWM modulators.
- In *trailing edge* PWM, the counter starts from 0 and goes up.
- The positive edge is aligned with the counter start, the descent *trailing* edge is determined by the modulating signal.

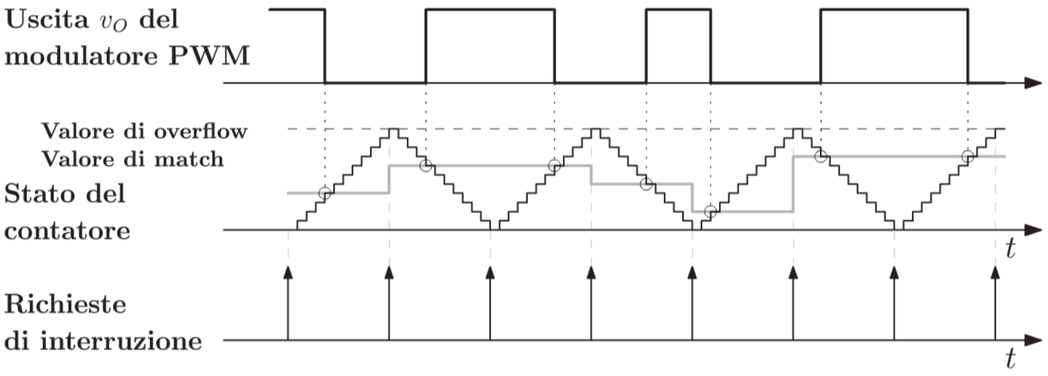
Leading edge PWM



(b)

- In *leading edge* PWM, the counter starts from maximum value and goes down.
- The descending edge is aligned with the counter restart, the positive *leading* edge is determined by the modulating signal.

Symmetric PWM



(c)

- In *symmetric* PWM, the pulse is symmetric with respect to the moments of counter restarts, with the counter going from 0 till maximum and then back to 0.
- (Pulse symmetry is useful in some applications for its better harmonic behavior).
- The symmetric mode allows also to update the signal two times per period, but in that case pulse symmetry is lost.

Response delay problem

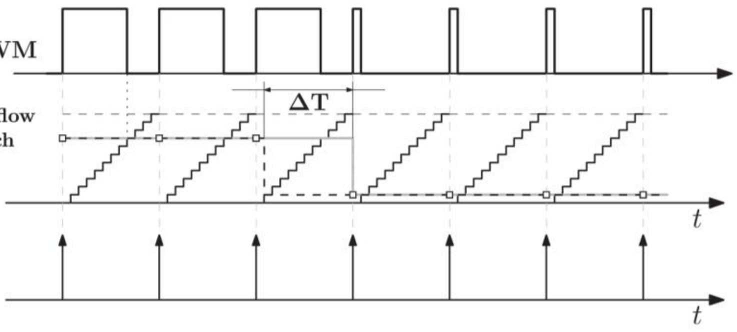


Figura 12.5: Ritardo di risposta di un modulatore PWM digitale. Il ritardo ΔT raggiunge quasi un periodo di modulazione. Esso è dovuto al fatto che il segnale modulante varia, a gradino, appena dopo che il suo valore è stato acquisito e mantenuto per l'intero periodo di modulazione successivo.

- A problem in digital PWM modulators is the delay in their response, since they sample the signal at the frequency of the carrier.
- The maximum delay is equal to the carrier period.
- Symmetric PWMs halve the delay.

PWM configuration

- The PWM modulator is configured similarly to a timer.
- The first parameter to choose is the *modulation frequency*. If not specified choose the highest to facilitate demodulation. Do not reduce resolution, which must be at least of 8 bits. Thus, the maximum f_{PWM} = $f_{clock}/256$.
- The counter frequency can be chosen by setting a division factor *P* in a *prescaler.*
- f_{clock} in µCs are in the order to tens of MHz, f_{PWM} in the order of hundred kHz, thus *P* in most cases is 1, 2, 4, or 8.
- PWM configuration is completed choosing the mode (symmetric, leading-edge, traling-edge) and the number of outputs to be activated (there can be multiple outputs). In case of complementary outputs, sometimes we can set a dead-time.
- The IRQ generated by the PWM modulator must be serviced. The ISR typically set the duty-cycle of the next PWM period.

See:

- Simone Buso, «Introduzione alle applicazioni industriali di Microcontrollori e DSP» Società editrice Esculapio, 2018
  - Chapter 12