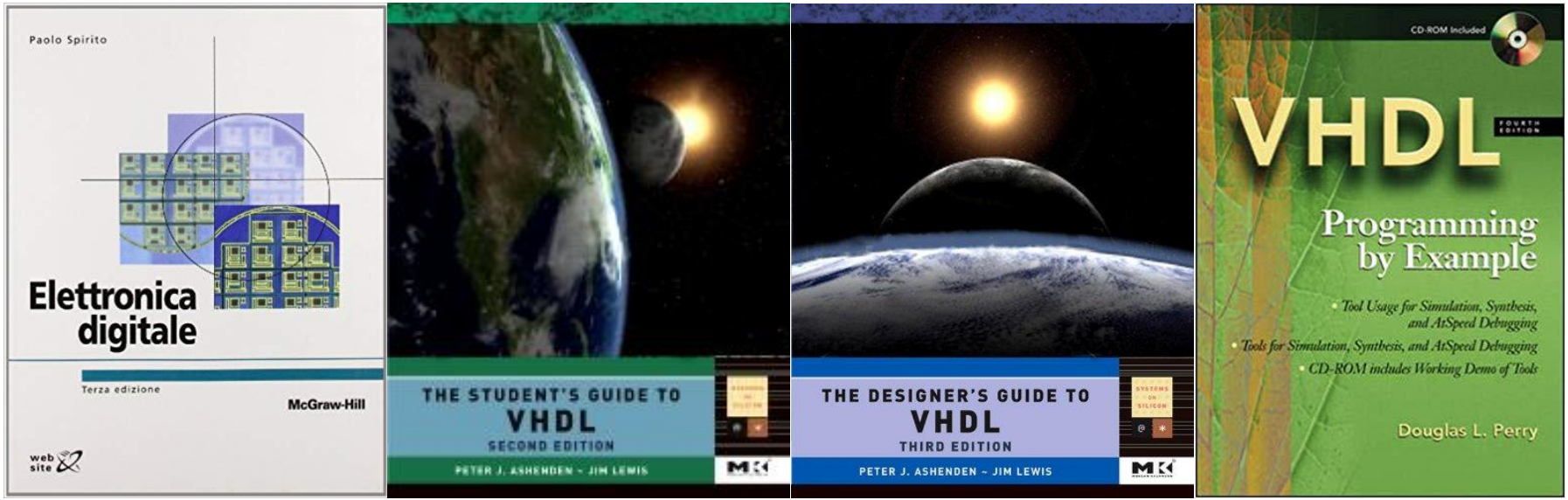
UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

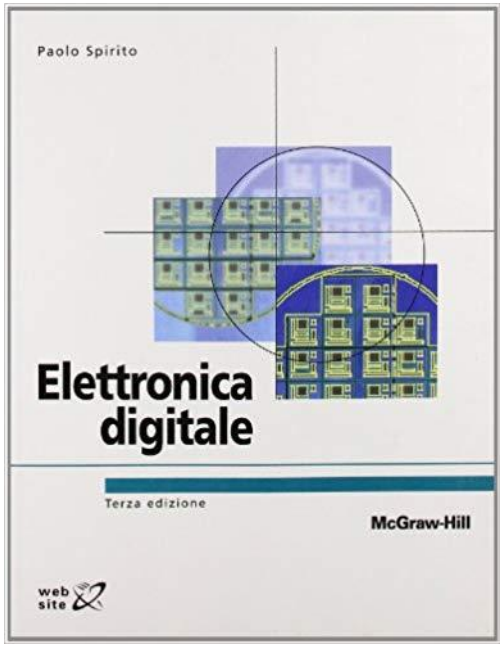
Initial information

A.Carini – Progettazione di sistemi elettronici

The books


Paolo Spirito
Elettronica digitale
Terza edizione
McGraw-Hill
web site
THE STUDENT'S GUIDE TO
VHDL
SECOND EDITION
PETER J. ASHENDEN ~ JIM LEWIS
THE DESIGNER'S GUIDE TO
VHDL
THIRD EDITION
PETER J. ASHENDEN ~ JIM LEWIS
CD-ROM Included
VHDL
FOURTH EDITION
Programming by Example
Tool Usage for Simulation, Synthesis, and AtSpeed Debugging
Tools for Simulation, Synthesis, and AtSpeed Debugging
CD-ROM includes Working Demo of Tools
Douglas L. Perry

The books

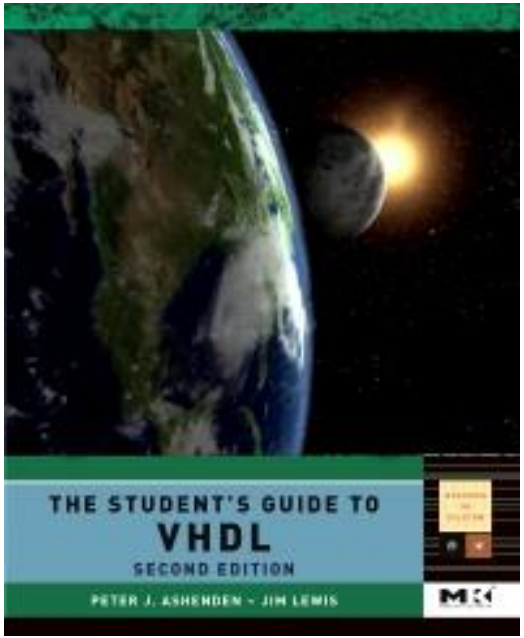


Paolo Spirito
Elettronica Digitale
McGraw-Hill, 2006

Biblioteca scientifica:

Inventario	H0A 17736
Collocazione	21b / 0045

The books

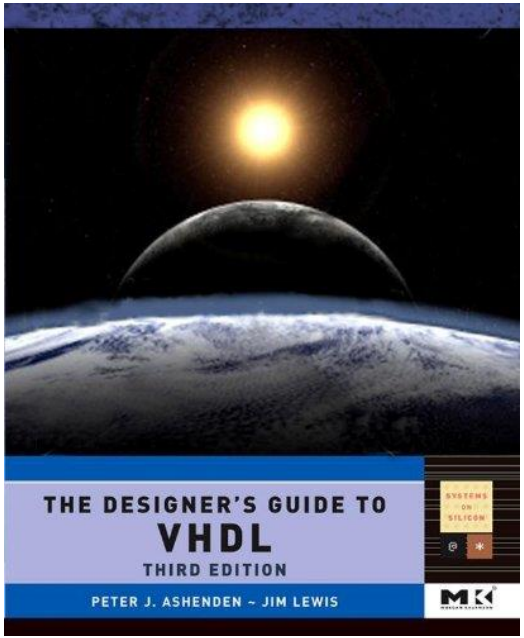


Peter Ashenden,
"The Student's Guide to VHDL",
Morgan Kaufmann, 2008

Biblioteca scientifica:

Inventario	H0A 20748
Collocazione	21a / 0272

The books

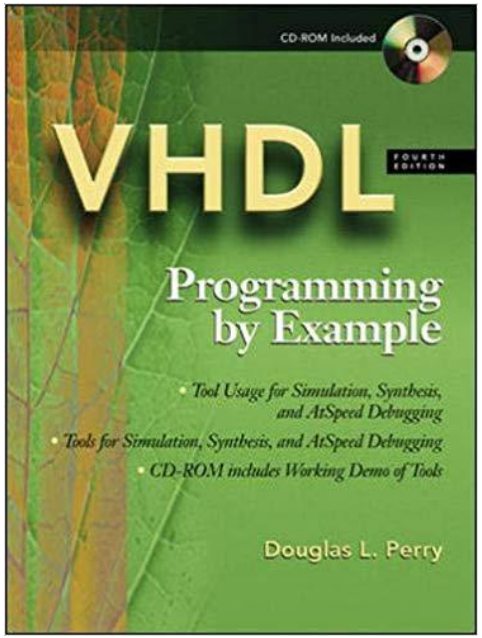


Peter Ashenden,
"The Designer's Guide to VHDL",
Morgan Kaufmann, 2006

Biblioteca scientifica:

Risorsa web da rete di ateneo:
http://search.ebscohost.com/login.aspx?direct=true&db=e000xww&AN=83627&lang=it&site=ehost-live

The books

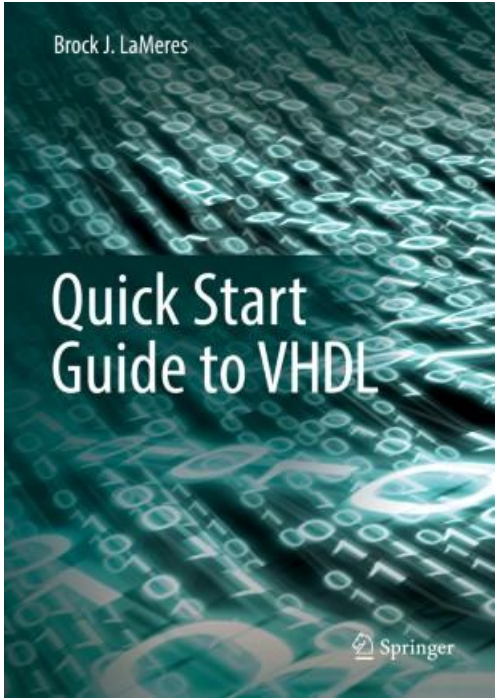


Douglas Perry,
"VHDL Programming by Example",
McGraw Hill, 2002

Biblioteca :

https://www.biblioest.it/SebinaOpac/resource/vhdl-programming-by-example/TSA3040836?tabDoc=tabloceb

The books



Brock J. LaMeres,
"Quick Start Guide to VHDL",
McGraw Hill, 2002

Biblioteca :

https://www.biblioest.it/SebinaOpac/resource/quick-start-guide-to-vhdl/TSA3227453?tabDoc=tabcata

The course program

01. Programmable logic devices and ASICs:
    01.01 Programmable logic arrays (PLA).
    01.02 Programmable array logics (PAL).
    01.03 Sequential PLDs.
    01.04 Complex PLDs (CPLD).
    01.05 Filed programmable gate arrays (FPGA).
    01.06 Application specific integrated circuits (ASIC).

02. Fundamental concepts of VHDL:
    02.01 Modeling digital systems.
    02.02 Domains and levels of modeling.
    02.03 Modeling languages.
    02.04 VHDL basic modeling concepts: behavioral and structural models, test benches, analysis, elaboration and execution.
    02.05 Lexical elements and Backus-Naur notation.

The course program

03. Scalar data types and their operations:
    03.01 Constants and variables.
    03.02 Scalar types.
    03.03 Type classification.
    03.04 Attributes of scalar types.
    03.05 Expressions and operators.

04. Sequential statements:
    04.01 If, case, null, loop, assert and report statements.

05. Composite data types and operations:
    05.01 Constrained and unconstrained arrays.
    05.02 Array operations.
    05.03 Records.

The course program

06. Basic system modeling concepts:
    06.01 The external interface description: entity declaration.
    06.02 The internal implementation description: architecture body, concurrent statements, signals.
    06.03 Behavioral description: signal assignments, wait statements, delta delays, process statements.
    06.04 Structural description: components and port maps.
    06.05 Analysis, elaboration and execution.

07. Subprograms:
    07.01 Procedures.
    07.02 Procedure parameters: signal parameters, default values, unconstrained array parameters.
    07.03 Concurrent procedure call statements.
    07.04 Functions.
    07.05 Overloading of procedures and operators.
    07.06 Visibility of declarations.

The course program

08. Packages and use clauses:
    08.01 Package declarations.
    08.02 Package bodies.

09. Resolved signals:
    09.01 Basic resolved signals.
    09.02 IEEE Std_Logic_1164 resolved subtypes.
    09.03 Resolved signals and ports.
    09.03 Resolved signals parameters.

10. Predefined and Standard Packages:
    10.01 The predefined packages
    10.02 IEEE standard packages

The course program

11. Aliases:
    11.01 Aliases for data objects.
    11.02 Aliases for non data objects.

12. Generic constants:
    12.01 Parameterizing behavior.
    12.02 Parameterizing structure.

13. Components and configurations:
    13.01 Components declarations and their use.
    13.02 Components configurations.

The course program

14. VHDL synthesis:
    - 14.01 RTL description.
    - 14.02 Constraints and attributes.
    - 14.03 Technology libraries.
    - 14.04 Synthesis.
    - 14.05 VHDL description of synthesizable combinatorial and sequential circuits.

15. High level design flow:
    - 15.01 RTL simulation.
    - 15.02 VHDL synthesis.
    - 15.03 Gate level functional verification.
    - 15.04 Place and routing.
    - 14.05 Post layout timing simulation.

Laboratories

We will use DE1-SOC boards for Intel FPGA University Program.
The boards have a Cyclone V SoC FPGA.
We will analyze, simulate, synthesize, and emulate VHLD code using Quartus Prime Lite Edition.
Quartus Prime can be downloaded from:
http://fpgasoftware.intel.com/?edition=lite