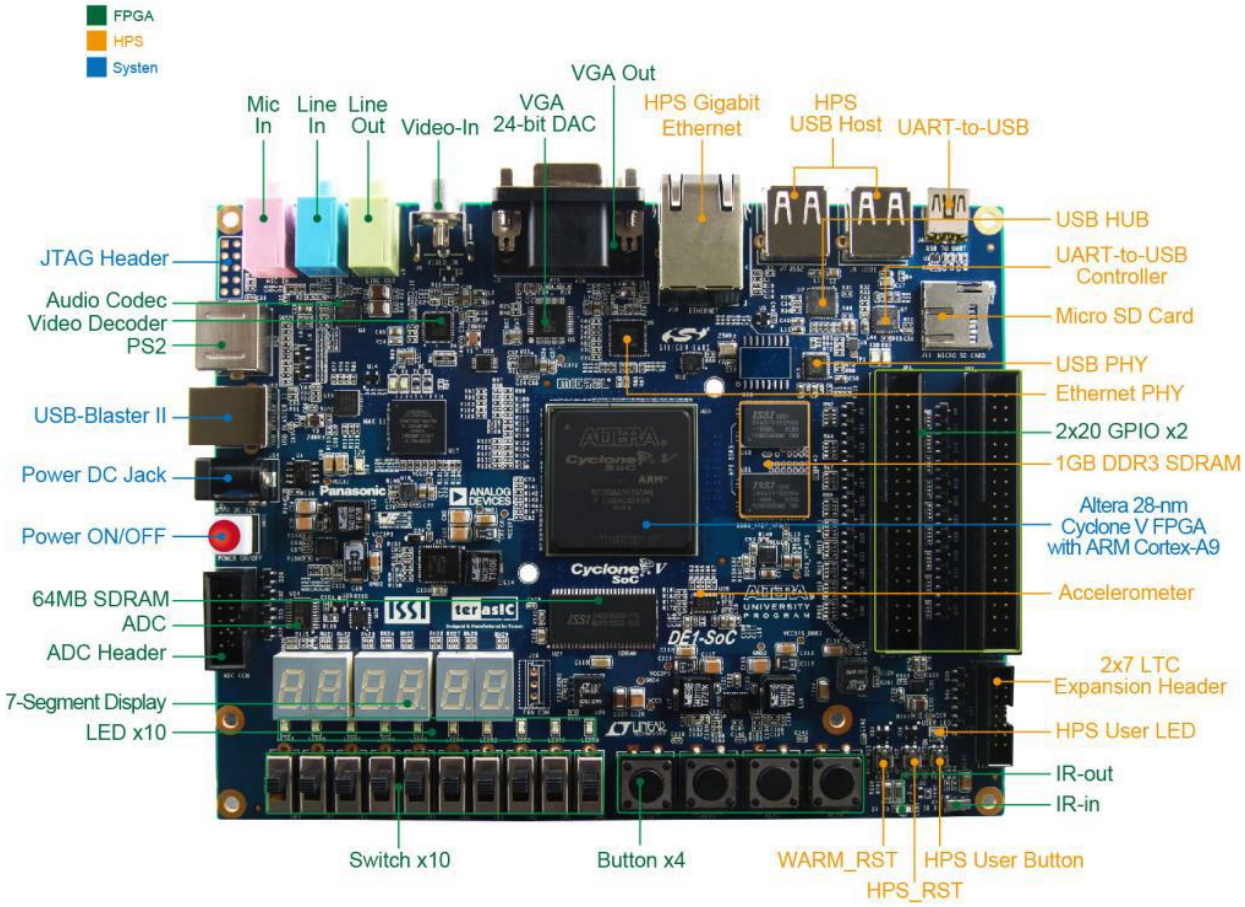
UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

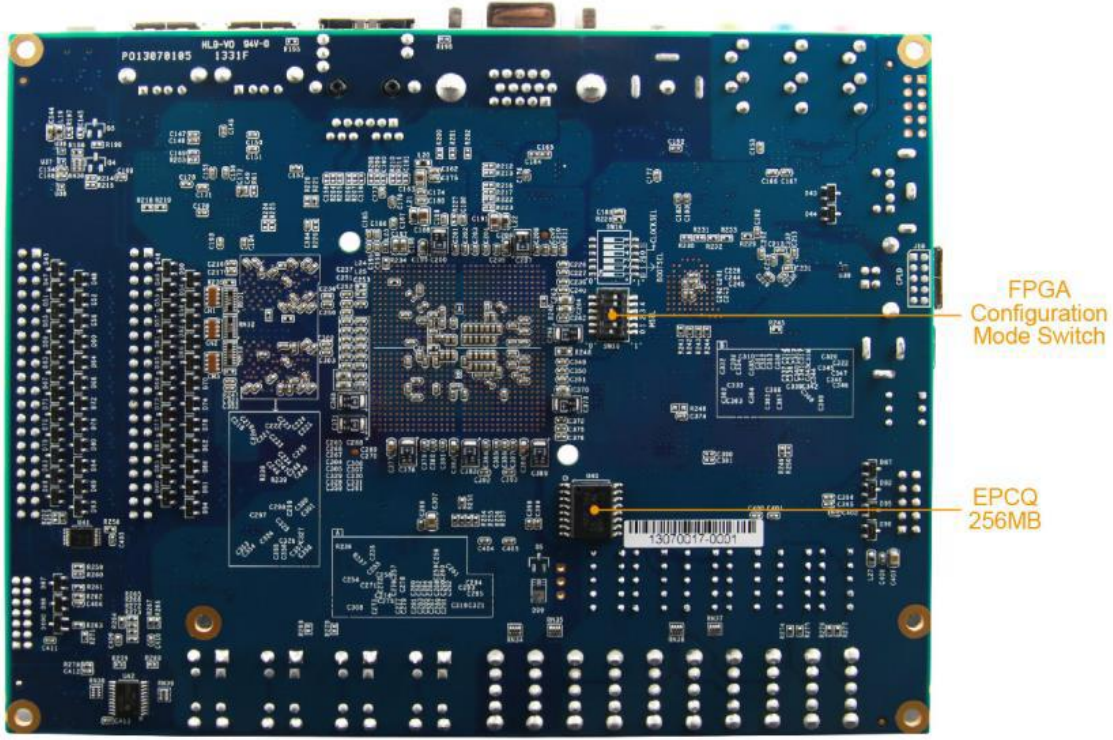
The De1-SoC development board

A.Carini – Progettazione di sistemi elettronici

Top view


FPGA
HPS
Systen
Mic In
Line In
Line Out
Video-In
VGA 24-bit DAC
VGA Out
HPS Gigabit Ethernet
HPS USB Host
UART-to-USB
USB HUB
UART-to-USB Controller
Micro SD Card
USB PHY
Ethernet PHY
2x20 GPIO x2
1GB DDR3 SDRAM
Altera 28-nm Cyclone V FPGA with ARM Cortex-A9
Accelerometer
2x7 LTC Expansion Header
HPS User LED
IR-out
IR-in
JTAG Header
Audio Codec
Video Decoder
PS2
USB-Blaster II
Power DC Jack
Power ON/OFF
64MB SDRAM
ADC
ADC Header
7-Segment Display
LED x10
Switch x10
Button x4
WARM_RST
HPS_RST
HPS User Button
DE1-SoC

Bottom view



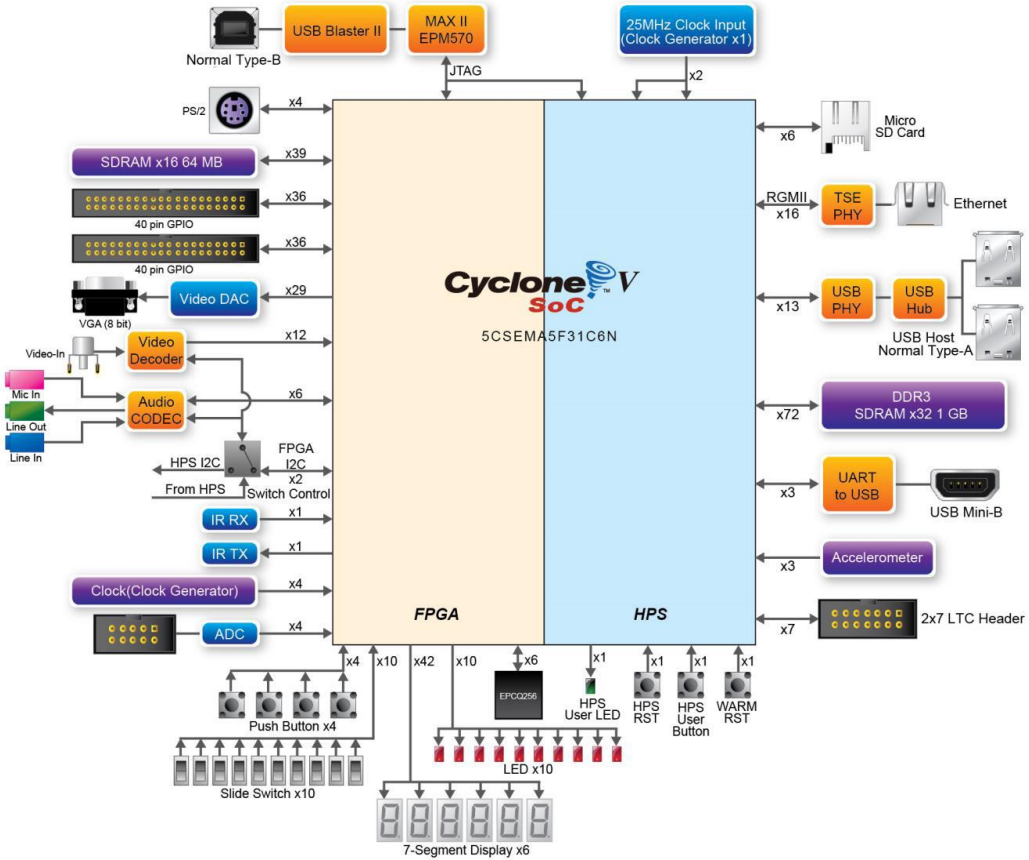
HW FPGA

- Altera Cyclone® V SE 5CSEMA5F31C6N device
- Altera serial configuration device – EPCS128
- USB-Blaster II onboard for programming; JTAG Mode
- 64MB SDRAM (16-bit data bus)
- 4 push-buttons
- 10 slide switches
- 10 red user LEDs
- Six 7-segment displays
- Four 50MHz clock sources from the clock generator
- 24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks
- VGA DAC (8-bit high-speed triple DACs) with VGA-out connector
- TV decoder (NTSC/PAL/SECAM) and TV-in connector
- PS/2 mouse/keyboard connector
- IR receiver and IR emitter
- Two 40-pin expansion header with diode protection
- A/D converter, 4-pin SPI interface with FPGA

HW HPS (Hard Processor System)

- 800MHz Dual-core ARM Cortex-A9 MPCore processor
- 1GB DDR3 SDRAM (32-bit data bus)
- 1 Gigabit Ethernet PHY with RJ45 connector
- 2-port USB Host, normal Type-A USB connector
- Micro SD card socket
- Accelerometer (I2C interface + interrupt)
- UART to USB, USB Mini-B connector
- Warm reset button and cold reset button
- One user button and one user LED
- LTC 2x7 expansion header

Block diagram

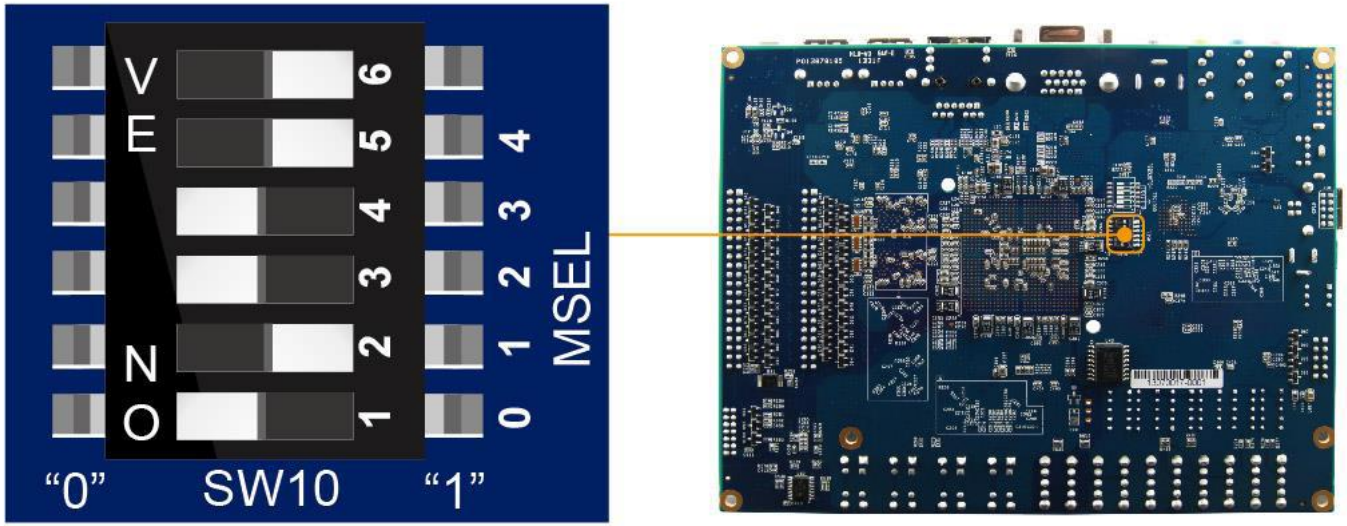


FPGA Device

- Cyclone V SoC 5CSEMA5F31 Device
- Dual-core ARM Cortex-A9 (HPS)
- 85K programmable logic elements
- 4,450 Kbits embedded memory
- 6 fractional PLLs
- 2 hard memory controllers

Settings of FPGA Configuration Mode

- These are the default settings (Active Serial mode) to be used in Labs:



HW Resources and board manual

- All HW resources (leds, buttons, switches, memories, etc.) are mapped into specific pins of the FPGA.
- The pin assignment can be found on the board User Manual.
- Keep at hand a copy of the board manual: DE1-SoC_User_manual.pdf