UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

Lab 0 – Getting acquainted with the tools

A.Carini – Progettazione di sistemi elettronici

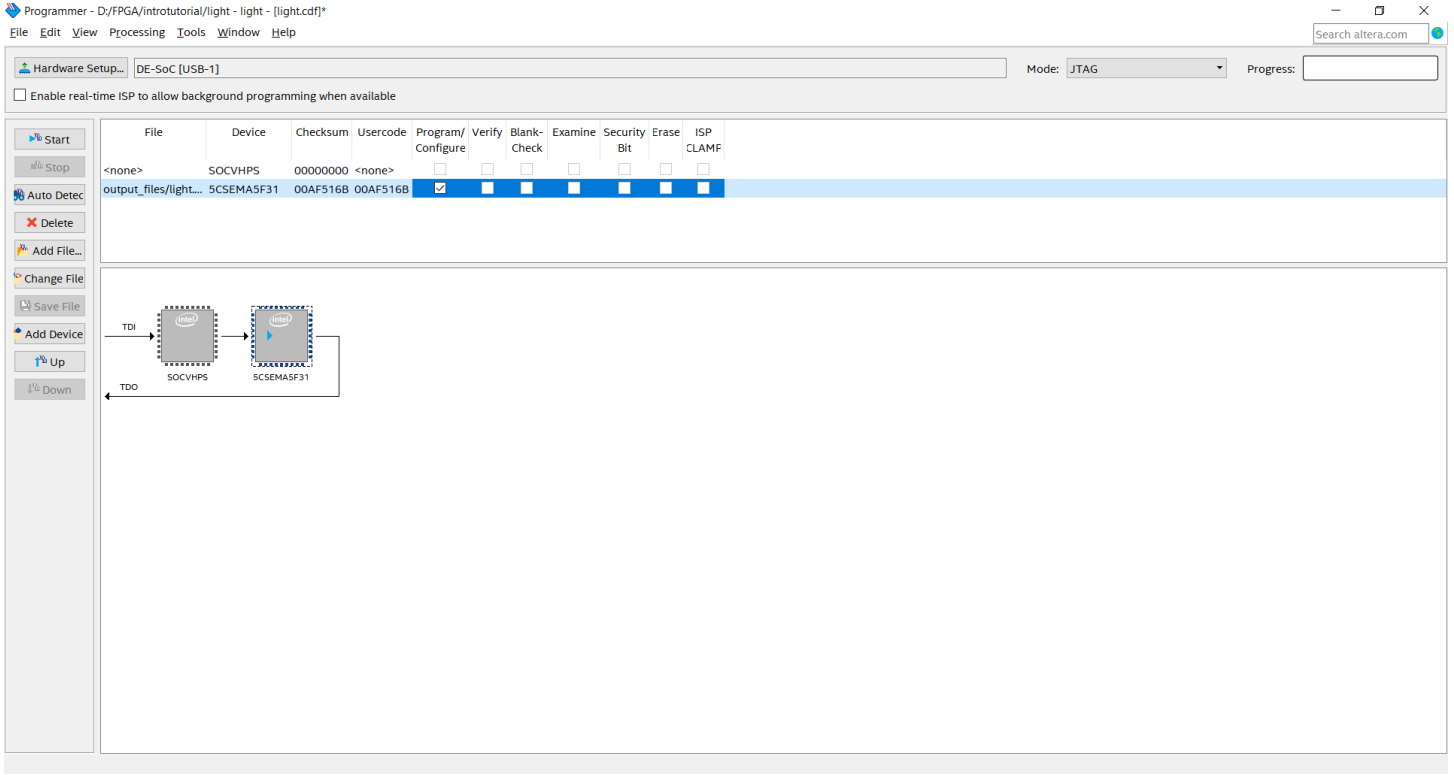
Preliminaries

- The DE-series boards require the Intel Quartus Prime CAD software. The Intel FPGA University Program recommends installation of Quartus Prime Lite Edition.
- Install this software on the computer, and ensure that the type of Intel FPGA family that is used on the board is included in the installation (Cyclone® V FPGAs).
- Plug in the power adapter that was included with the board.
- Use the provided USB cable to connect the connector on the DE-series board labeled USB Blaster to a USB port on the computer.
- Press the power button to turn on the DE-series board. The computer will recognize the new hardware connected to its USB port, but it will be unable to proceed if it does not have the required driver already installed.
- The DE-series board is programmed by using Intel's USB-Blaster, or USB-Blaster II, driver software. If the driver software is not already installed, then follow the steps of Section 4.1 of Getting_Started_with_DE-series_boards.pdf.

Assigment

- Perform the Quartus_Std_Introduction tutorial.
- When requested select the FPGA: Cyclone V SoC 5CSEMA5F31C6
- For assigning the pin use:
  - SW0: PIN_AB12
  - SW1: PIN_AC12
  - LEDR0: PIN_V16
- Be aware that Figure 31 is wrong. The right figure is in the next slide

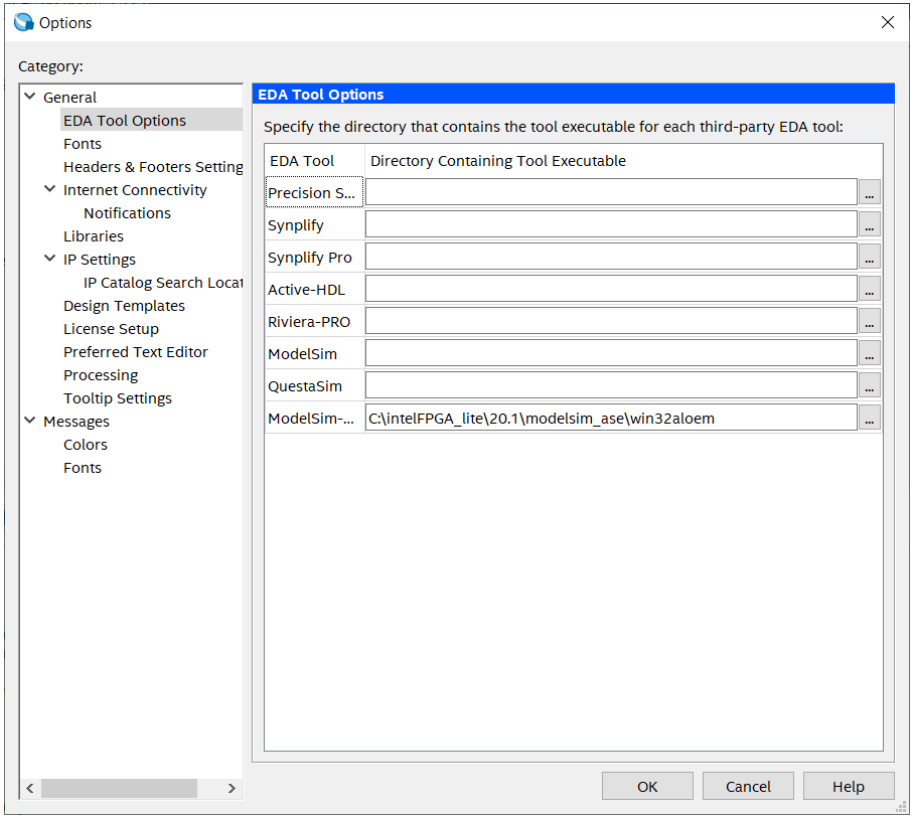
Figure 31 corrected



Assigment

- Perform the Quartus_II_Simulation tutorial.
- When requested select the FPGA: Cyclone V SoC 5CSEMA5F31C6
- In Section IV, select as simulation tool ModelSim-Altera and provide the right path (e.g., in the following figure).
- If the following error appears:
- **# ** Error (suppressible): (vsim-12110) The -novopt option has no effect on this product. -novopt option is now deprecated and will be removed in future releases.**
- *In the Simulation Waveform Editor, choose Simulation Settings|Simulation Options and delete -novopt following vsim in the Model Script (and save the changes).*
- The Timing Simulation currently does not work with Cyclone V.
- Moreover, if the following error appear:
- **# ** Error (suppressible): (vsim-SDF-3196) Failed to find SDF file "majority3_vhd.sdo".**
- Select Simulation -> Simulation settings -> Verilog and repeat the timing simulation.

Assigment


Options
Category:
General
EDA Tool Options
Fonts
Headers & Footers Setting
Internet Connectivity
Notifications
Libraries
IP Settings
IP Catalog Search Locat
Design Templates
License Setup
Preferred Text Editor
Processing
Tooltip Settings
Messages
Colors
Fonts
EDA Tool Options
Specify the directory that contains the tool executable for each third-party EDA tool:
EDA Tool
Directory Containing Tool Executable
Precision S...
Synplify
Synplify Pro
Active-HDL
Riviera-PRO
ModelSim
QuestaSim
ModelSim-...
C:\intelFPGA_lite\20.1\modelsim_ase\win32aloem
OK
Cancel
Help

Assigment

- Perform the Using_ModelSim tutorial.
- The files mentioned in the tutorial can be found in Using_ModelSim.zip
- For the timing simulation, in Quartus Prime you need the device support of Cyclone IV (at this time, timing simulation is not possible with Cyclone V).

Assigment

- Perform the «Tutorial1 Schematico» tutorial.