

**UNIVERSITÀ  
DEGLI STUDI  
DI TRIESTE**

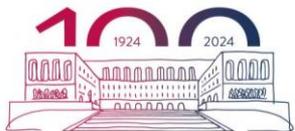


# **L'ingegneria elettronica, informatica e biomedica nella rivoluzione digitale**

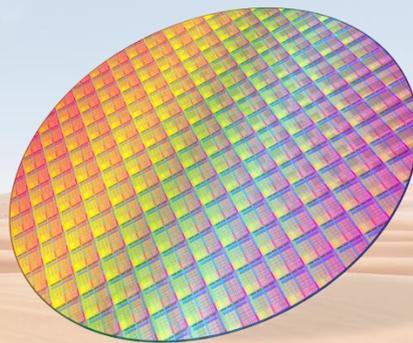
**– parte II**

**Prof. Alberto Carini**

**Docente di Elettronica**



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**Dalla Sabbia ai Circuiti Integrati**

# Indice

- Il silicio
- Diodi e Transistori
- Il processo di fabbricazione dei circuiti integrati.



# Il Silicio



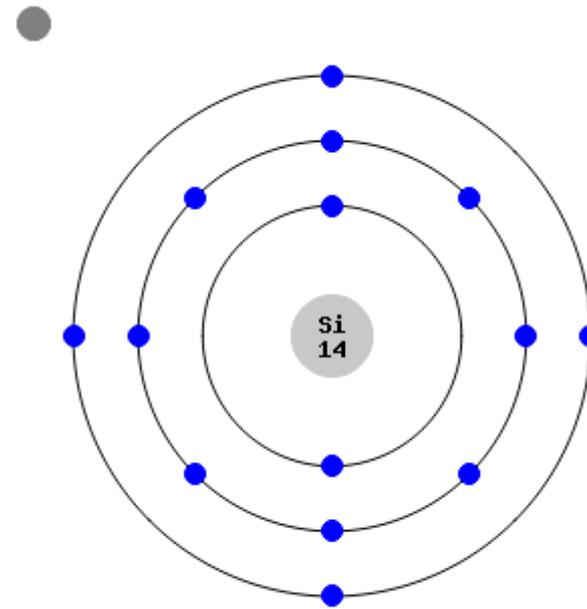
- E' il semiconduttore più usato nell'elettronica.
  - Il secondo elemento per abbondanza nella crosta terrestre, dopo l'ossigeno.
  - Usato in elettronica in forma di cristallo.
  - I *chip* (i processori, le memorie) sono costituiti da un singolo cristallo di silicio opportunamente trattato.
- 
- I materiali si dividono in **amorfi**, **policristallini**, o **cristallini** a seconda della disposizione dei loro atomi.
  - Nei materiali *amorfi* gli atomi hanno una distribuzione totalmente disordinata.
  - Nei *cristalli* abbiamo una disposizione regolare
  - I materiali *policristallini* sono formati da tanti grani di cristallo.

# Il Silicio

		IIIA	IVA	VA	VIA
		5 10.811 <b>B</b> Boron	6 12.01115 <b>C</b> Carbon	7 14.0067 <b>N</b> Nitrogen	8 15.9994 <b>O</b> Oxygen
		13 26.9815 <b>Al</b> Aluminum	14 28.086 <b>Si</b> Silicon	15 30.9738 <b>P</b> Phosphorus	16 32.064 <b>S</b> Sulfur
IIB	30 65.37 <b>Zn</b> Zinc	31 69.72 <b>Ga</b> Gallium	32 72.59 <b>Ge</b> Germanium	33 74.922 <b>As</b> Arsenic	34 78.96 <b>Se</b> Selenium
48	112.40 <b>Cd</b> Cadmium	49 114.82 <b>In</b> Indium	50 118.69 <b>Sn</b> Tin	51 121.75 <b>Sb</b> Antimony	52 127.60 <b>Te</b> Tellurium
80	200.59 <b>Hg</b> Mercury	81 204.37 <b>Tl</b> Thallium	82 207.19 <b>Pb</b> Lead	83 208.980 <b>Bi</b> Bismuth	84 (210) <b>Po</b> Polonium

Silicon

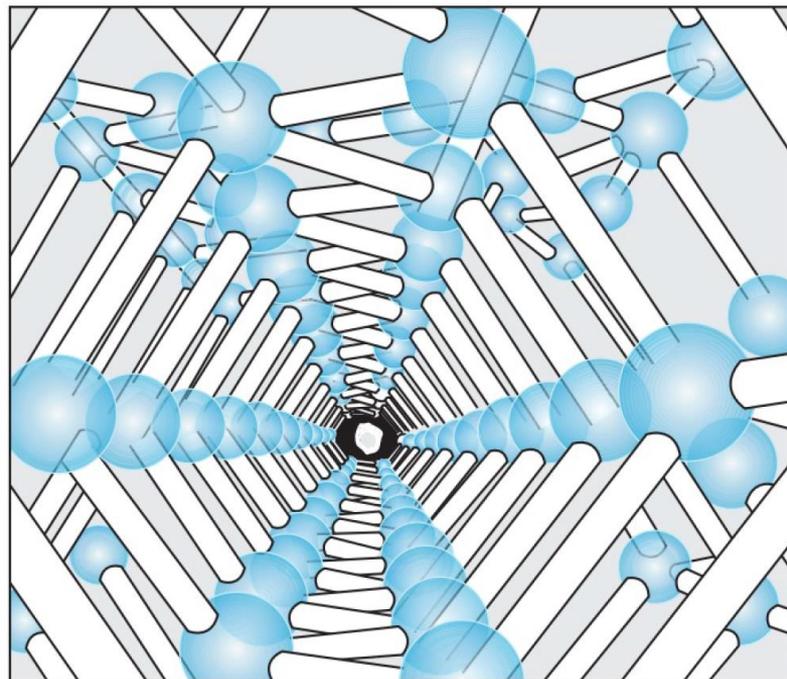
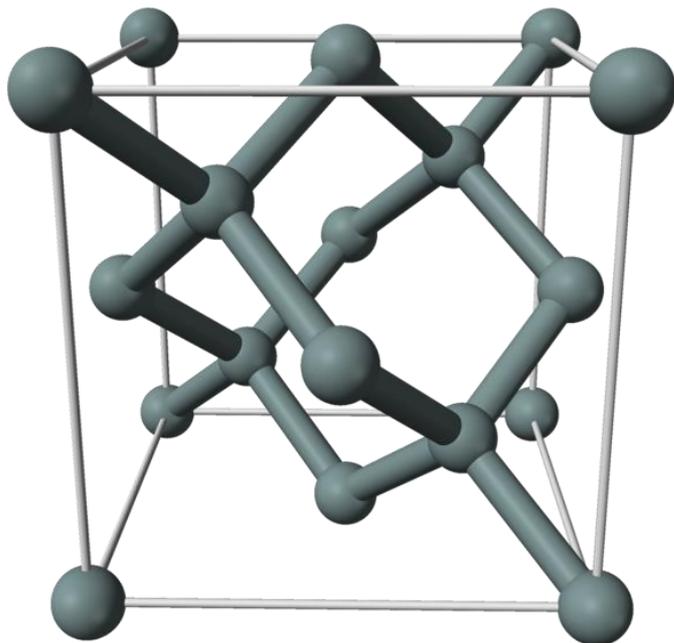
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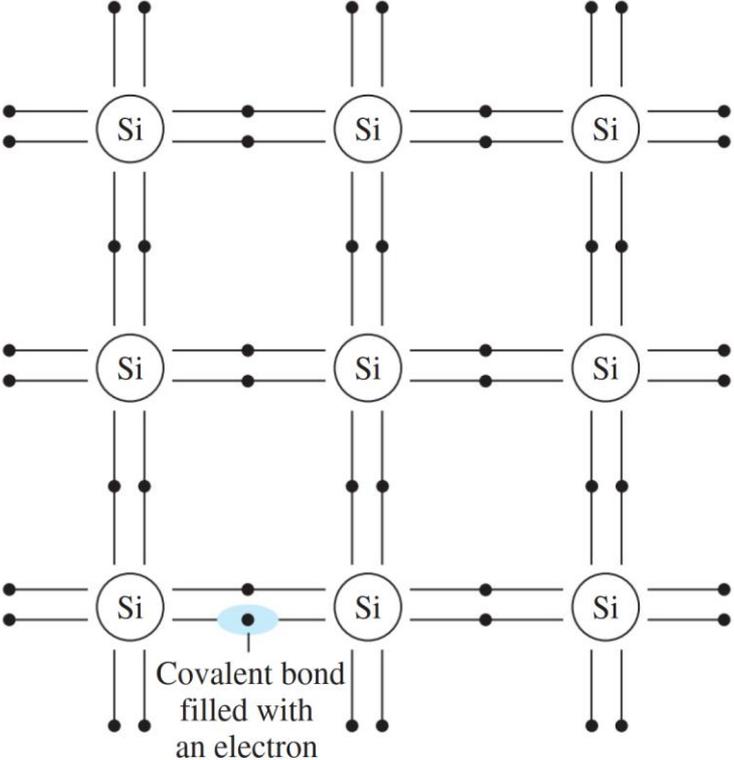
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ChemicalAid  
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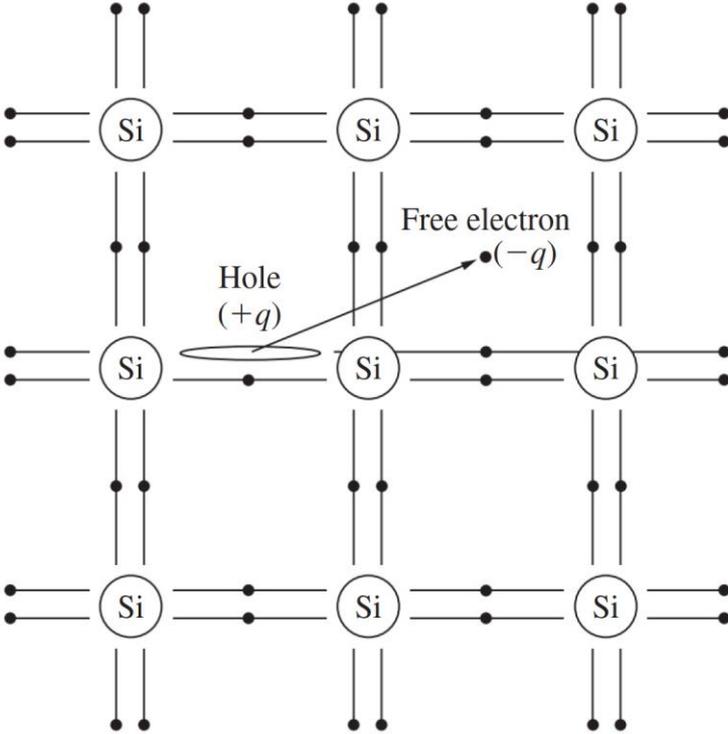
# Il Silicio



# Il Silicio



# Il Silicio



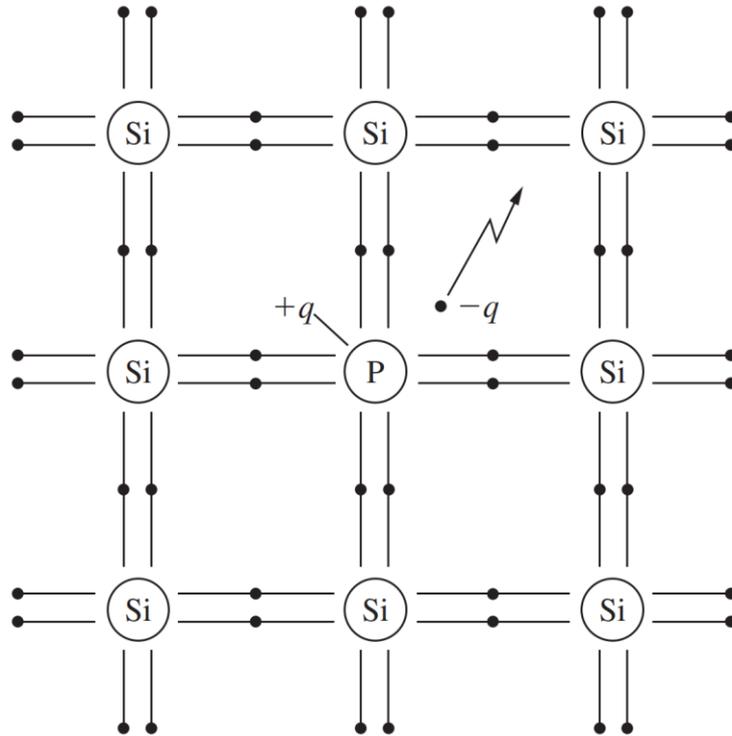
# Silicio intrinseco e drogato

- A temperatura ambiente ( $23^{\circ}\text{C} = 300\text{K}$ ):
  - concentrazione intrinseca di elettroni e lacune:  $7 \cdot 10^9 \text{ el./cm}^3 = 7,000,000,000 \text{ el./cm}^3$
  - concentrazione degli atomi di Si:  $5 \cdot 10^{22} \text{ atomi/cm}^3 = 500,000,000,000,000,000,000 \text{ atomi/cm}^3$
- Il silicio puro è quasi un **isolante** ...
- ... ma possiamo modificarne la conducibilità **drogandolo** con
  - **atomi accettori** (III colonna, e.g., Boro)
  - **atomi donatori** (V colonna, e.g. Fosforo, Arsenico, Antimonio)

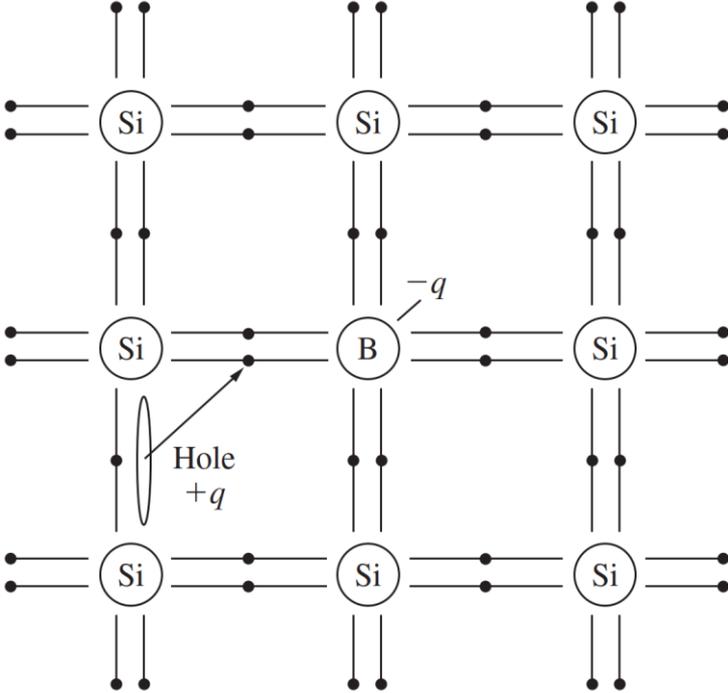
# Il Silicio

		IIIA	IVA	VA	VIA
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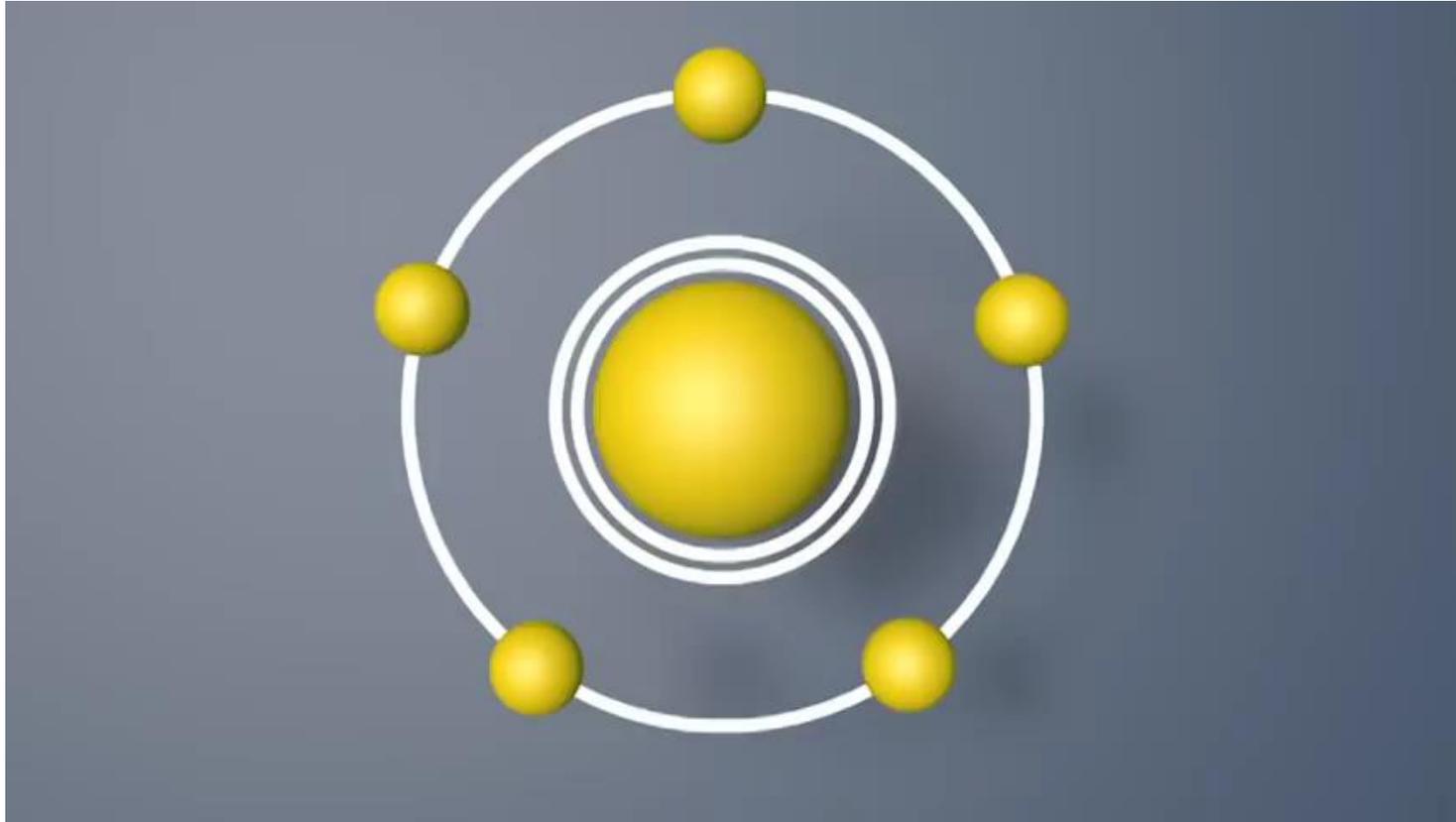
# Il Silicio drogato n



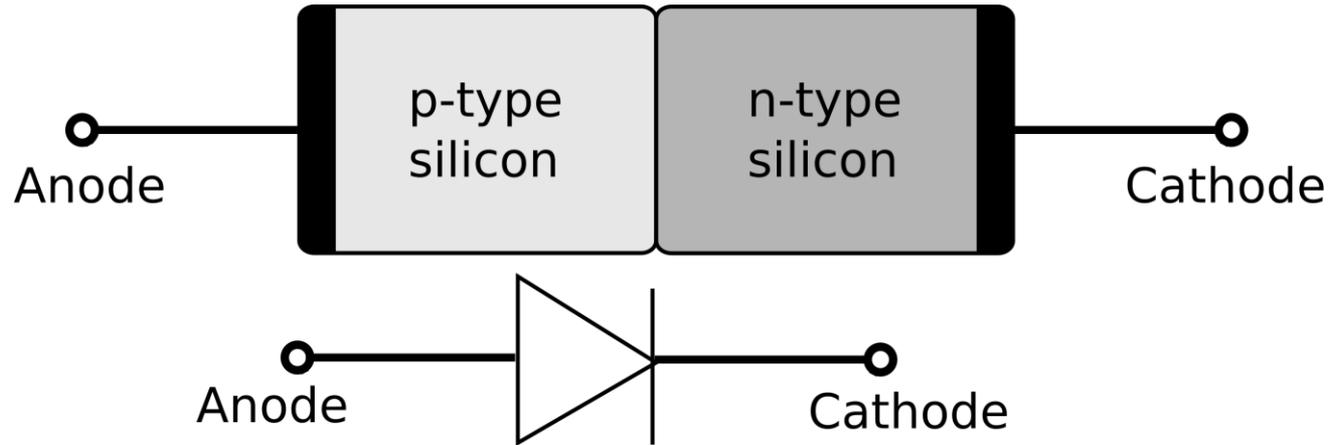
# Il Silicio drogato p



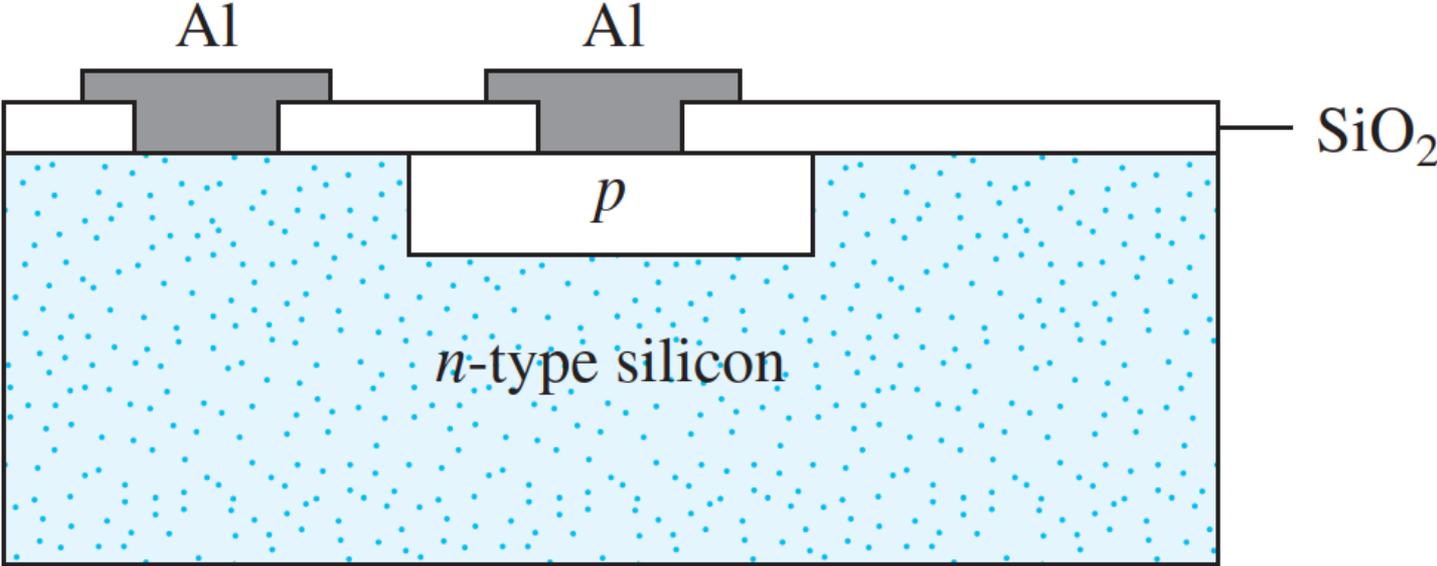
## Il Silicio drogato n e p



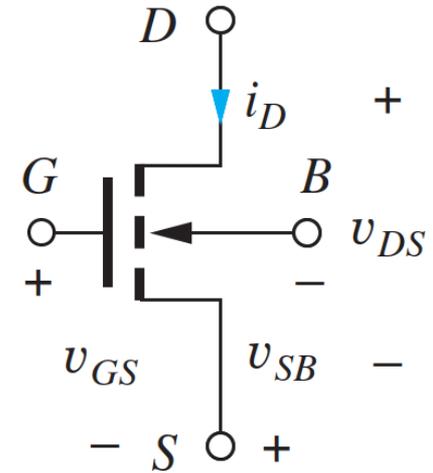
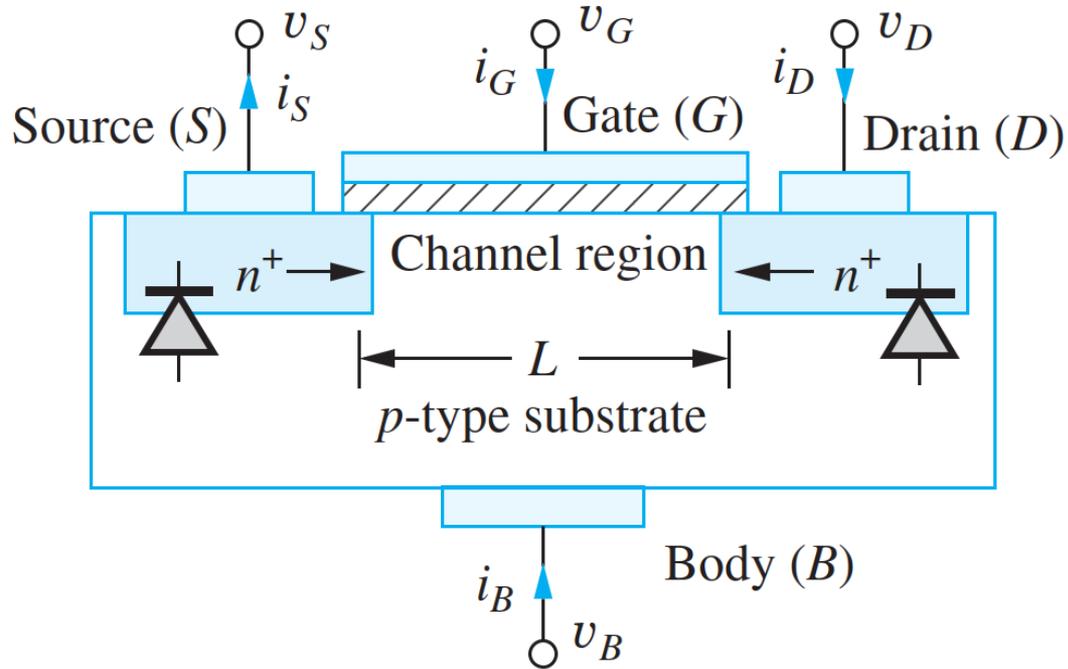
# Giunzione pn - Diodo



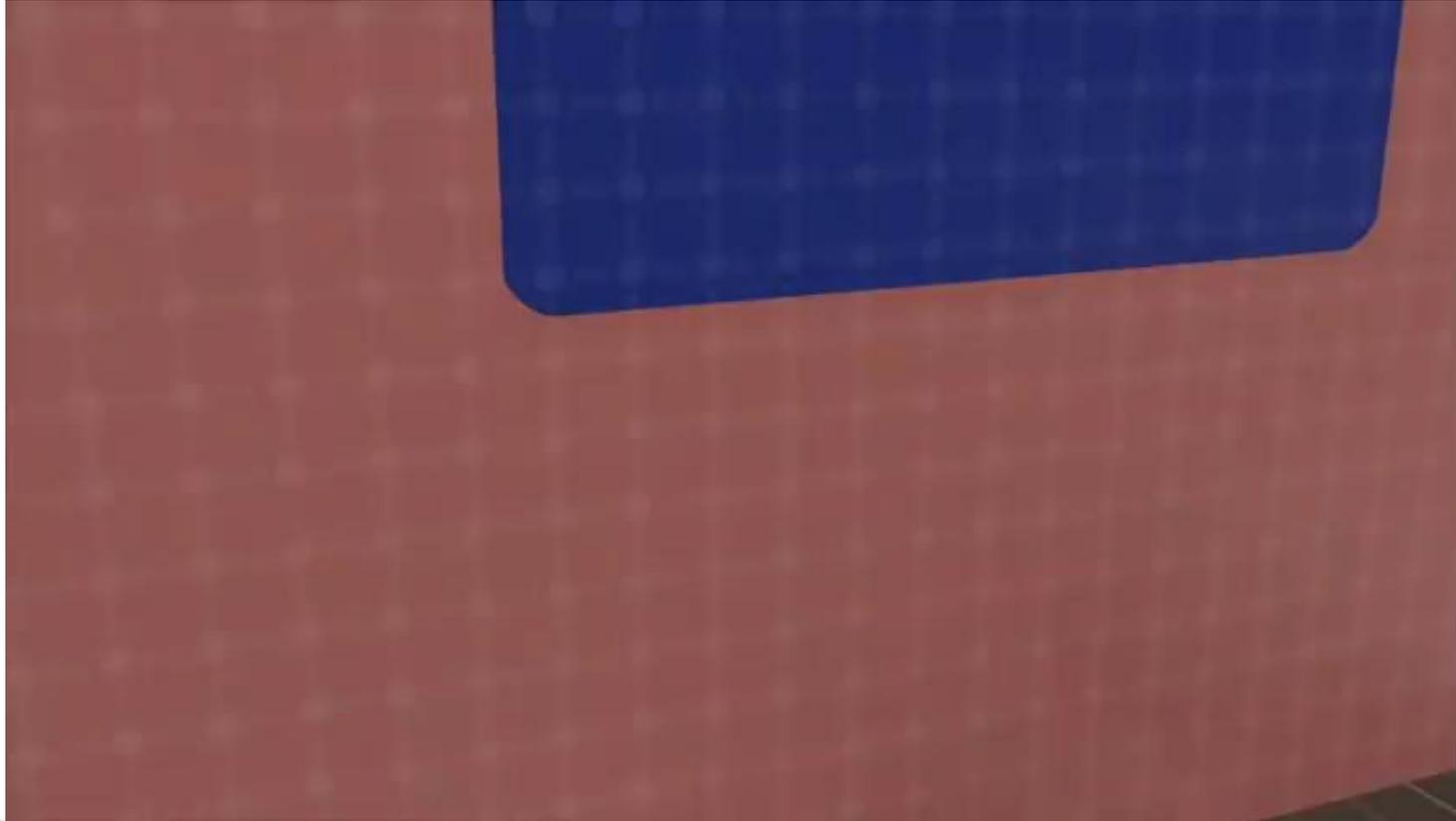
# Giunzione pn - Diodo



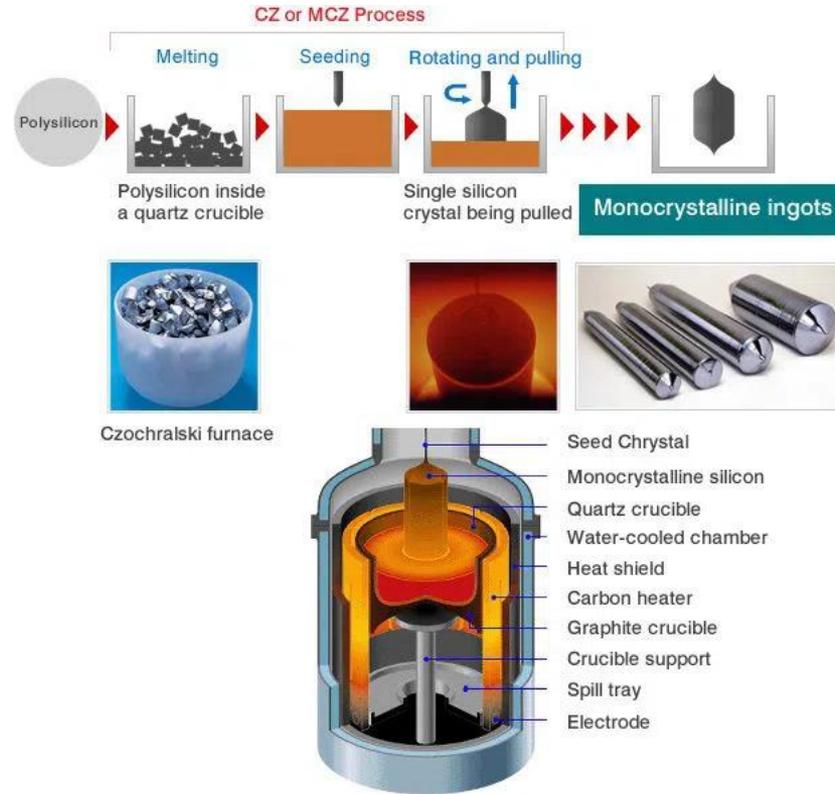
# Il transistor MOS – Metallo Ossido Semiconduttore



# Il transistor MOS – Metallo Ossido Semiconduttore



# Dal silicio a un lingotto monocristallino



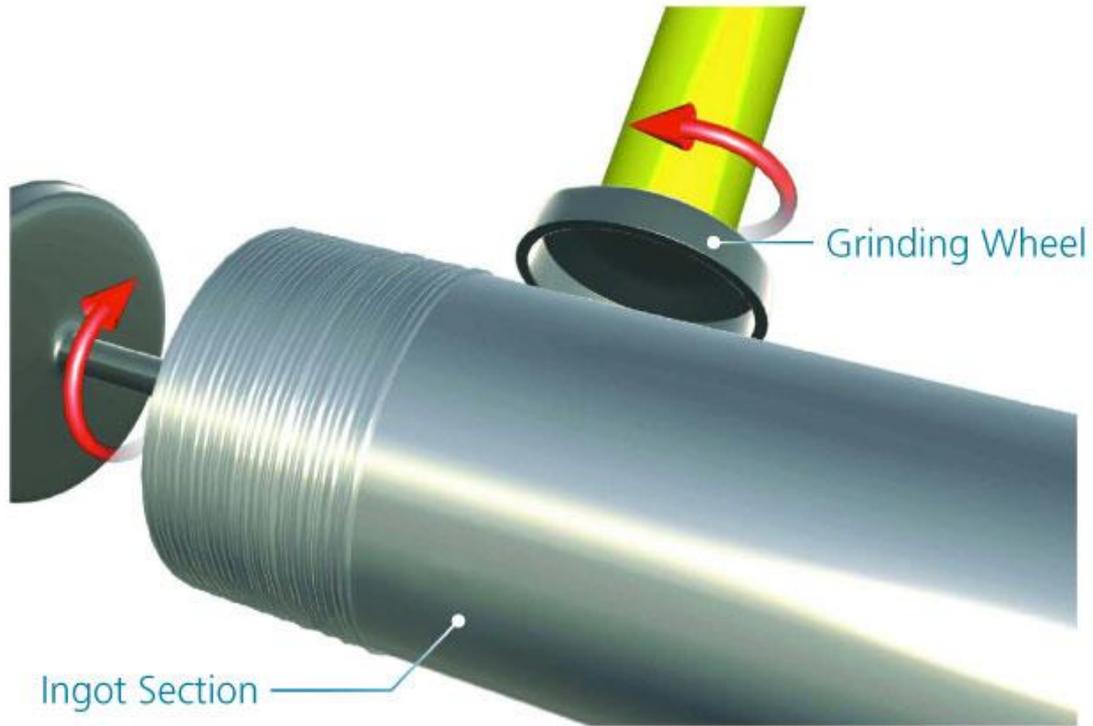
## Dal silicio a un lingotto monocristallino



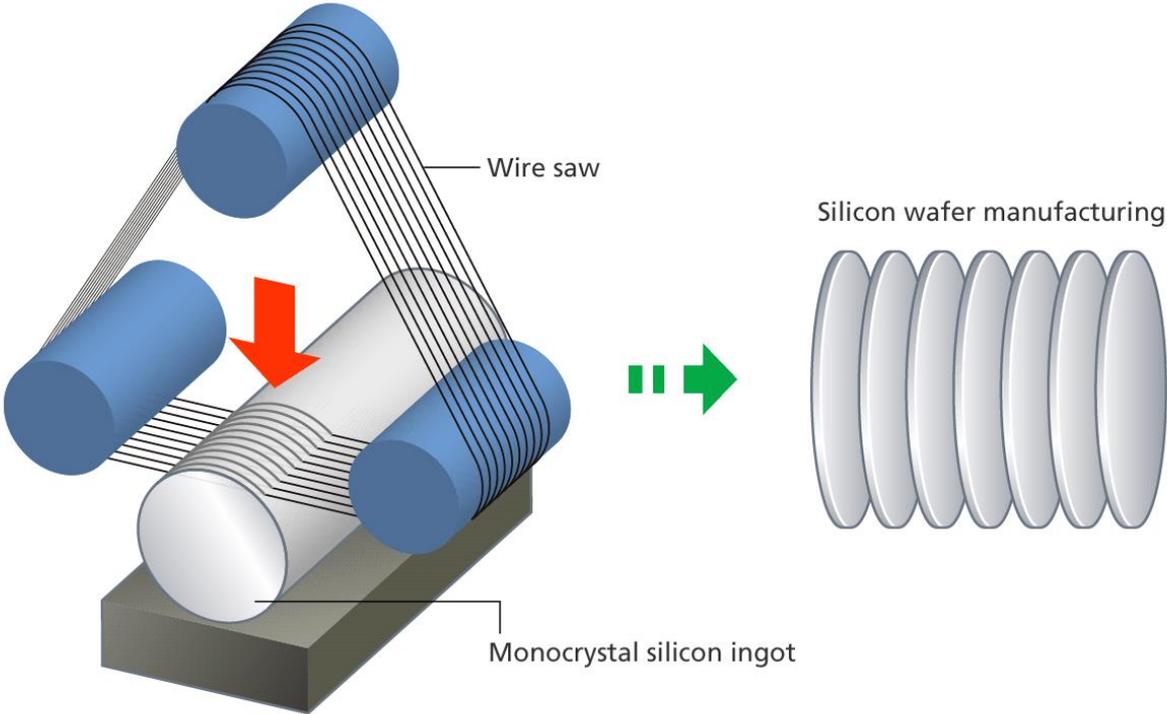
# Il lingotto di silicio



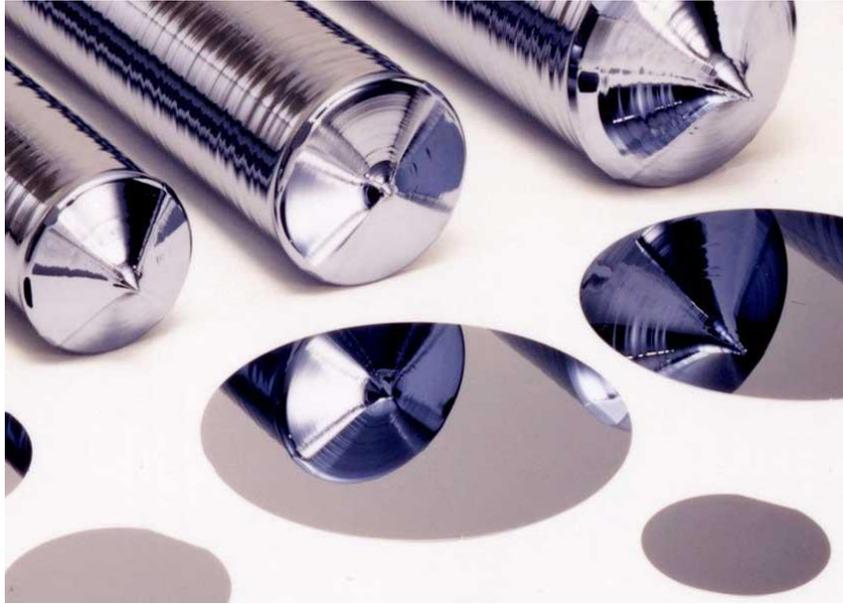
## Il lingotto viene levigato



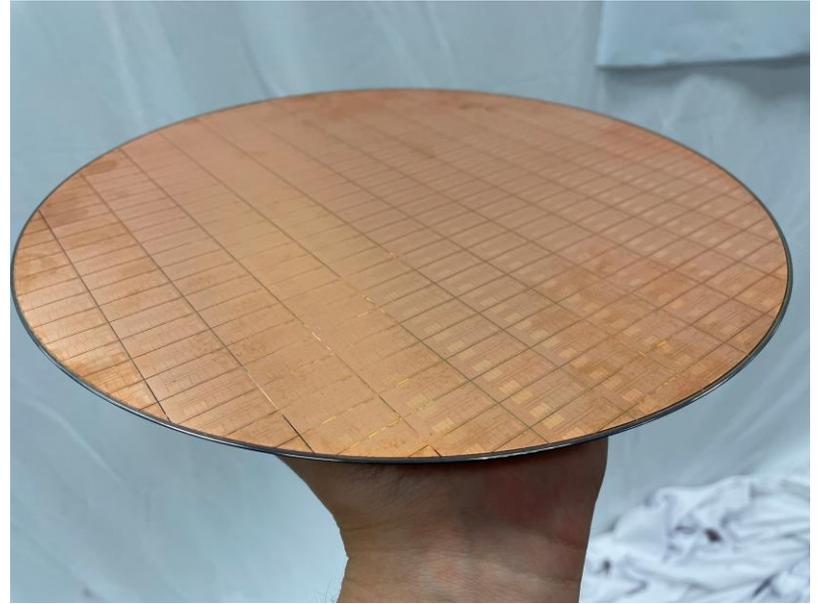
# Il lingotto viene affettato



# Produzione del wafer



Prima



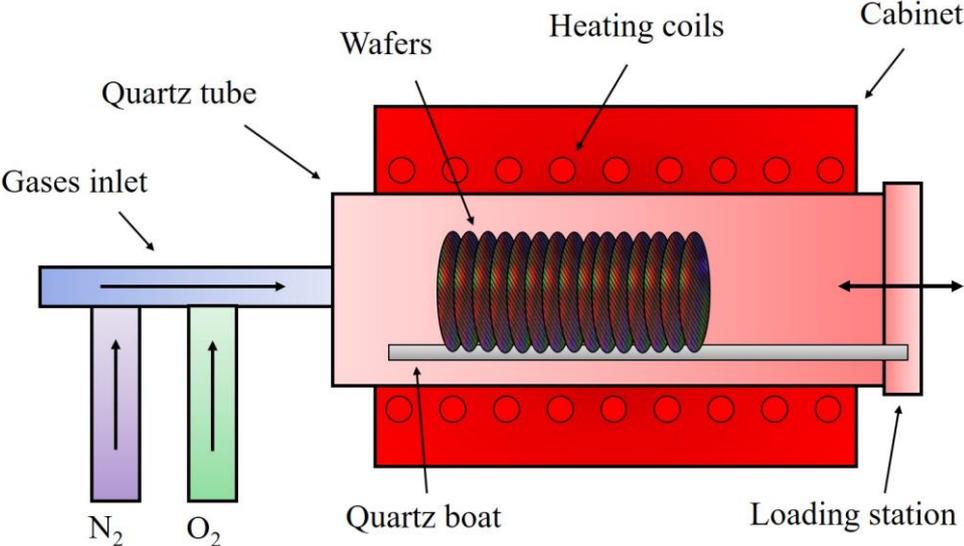
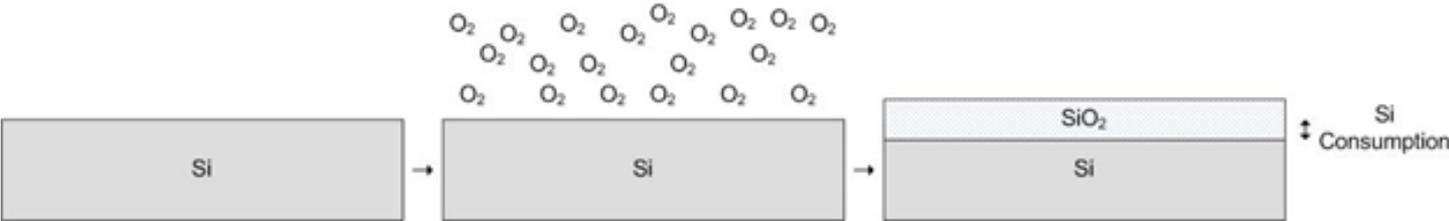
Dopo

# Principali processi

- Ossidazione
- Fotolitografia
- Incisione (Etching)
- Deposizione
- Impiantazione ionica
- Ricottura (Annealing)



# Ossidazione



# Fotolitografia

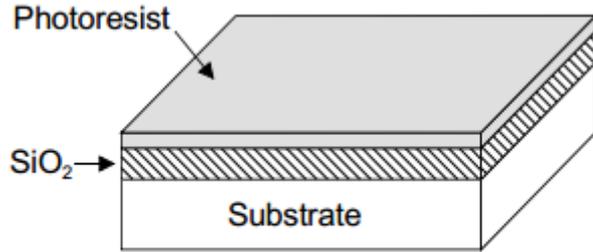
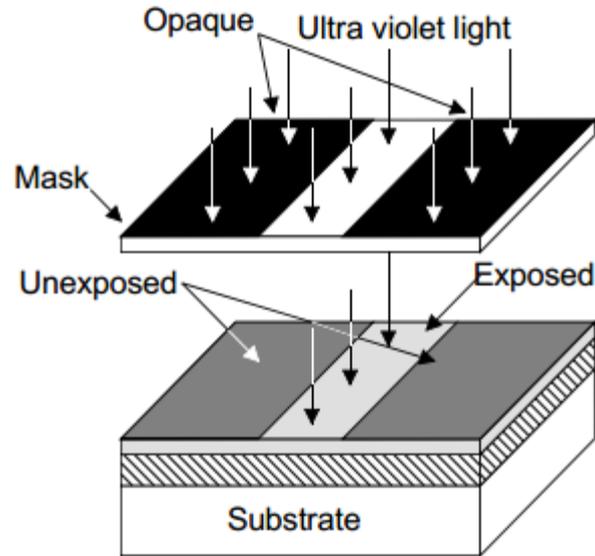
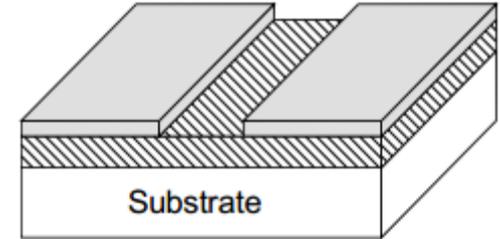


Photo Resist coating

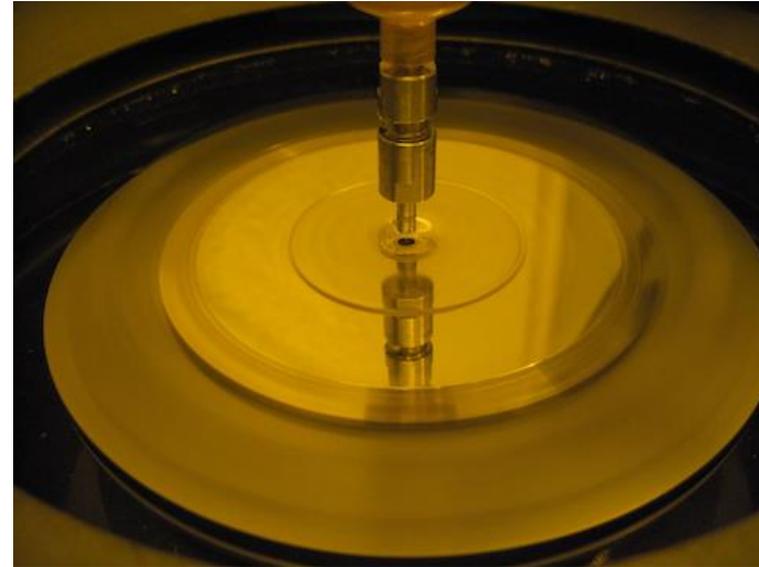
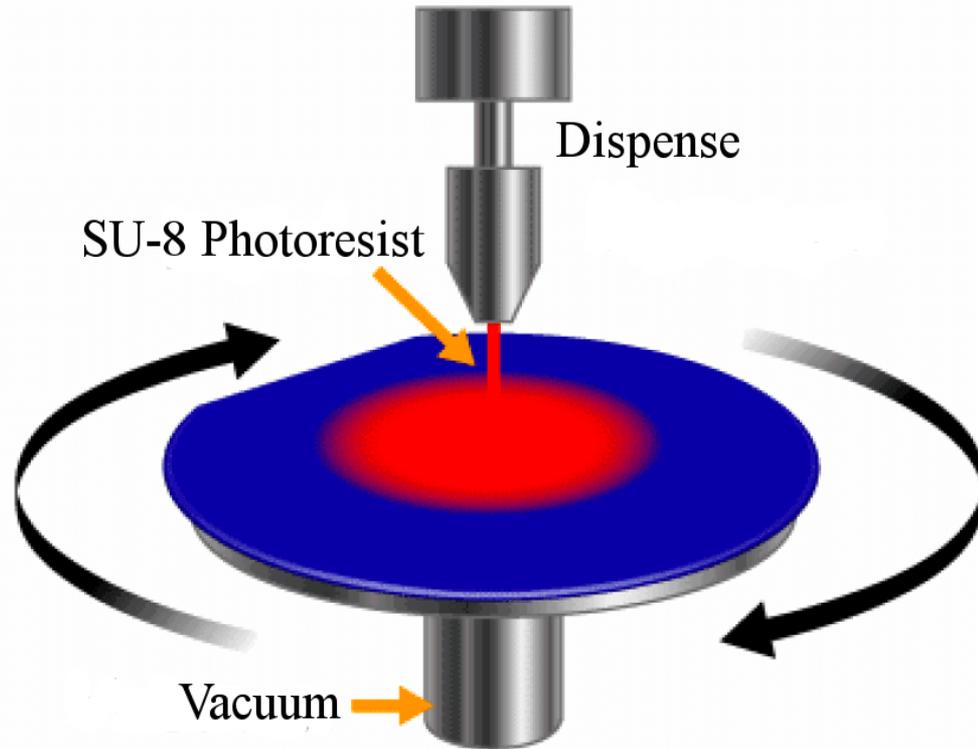


Exposure



Development

# Fotolitografia: deposizione del photoresist



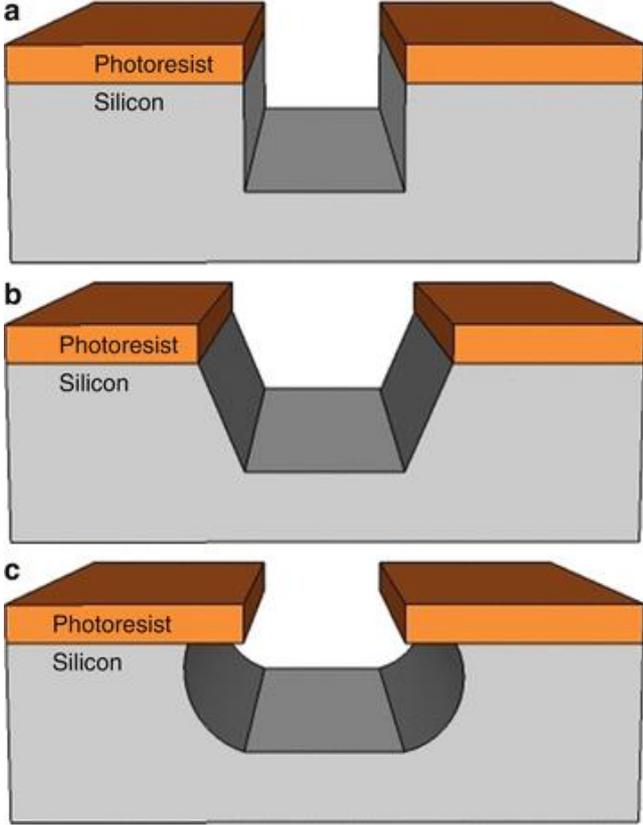
# Litografia



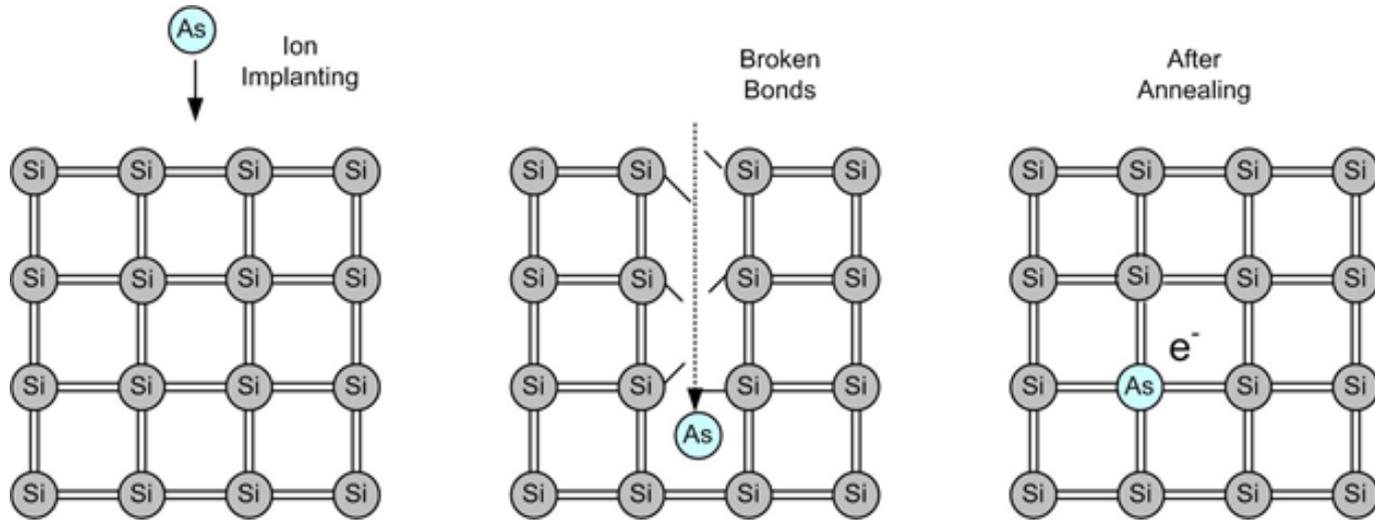
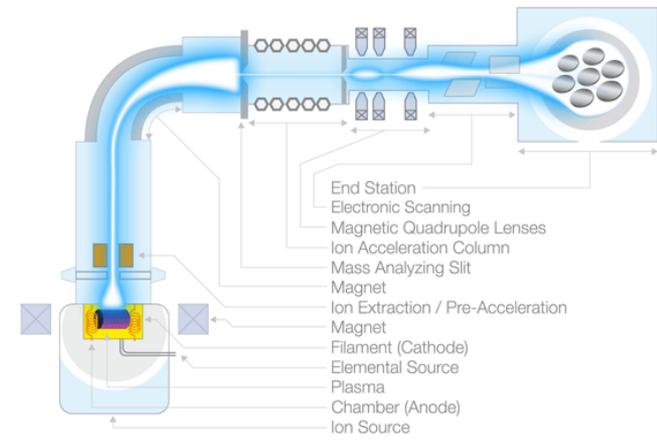
# Litografia EUV – macchina ASLM (laser UV a 13,5 nm)



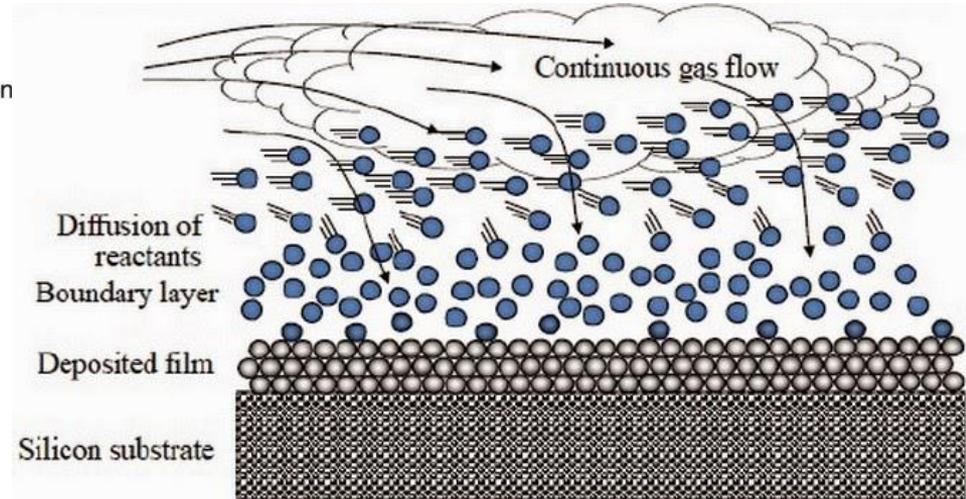
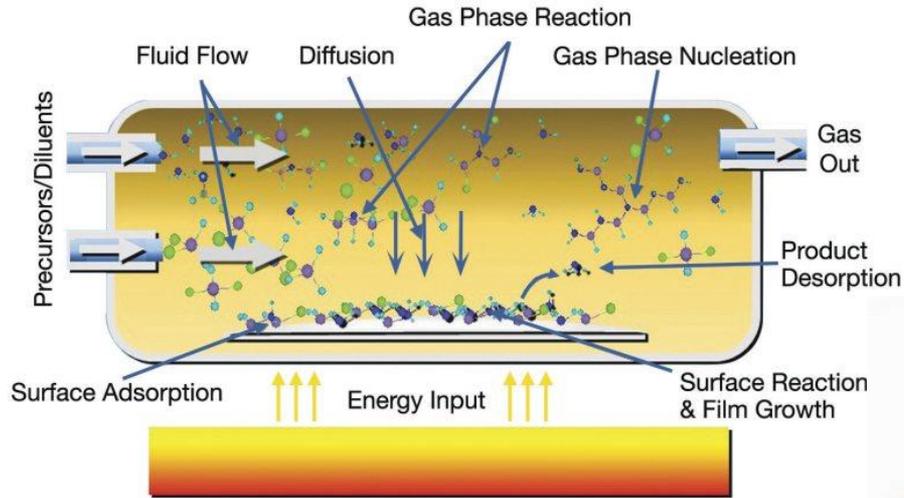
# Etching



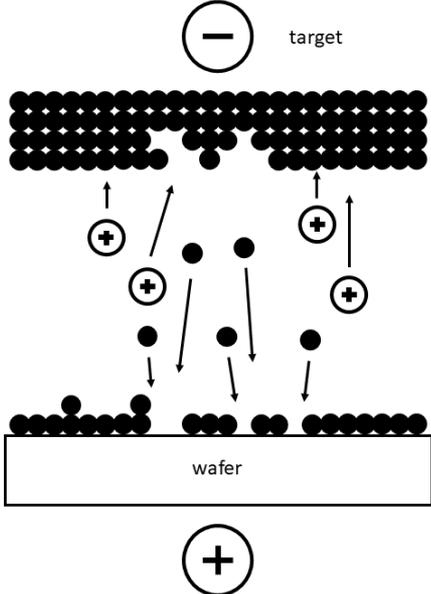
# Impiantazione ionica



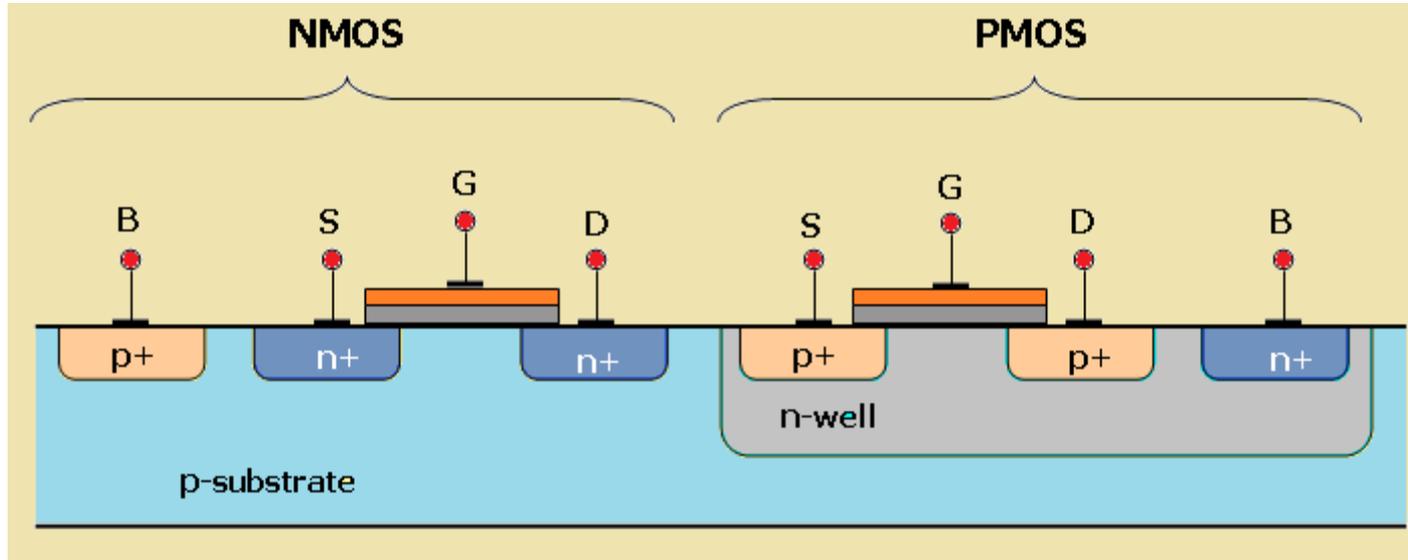
# Deposizione mediante CVD



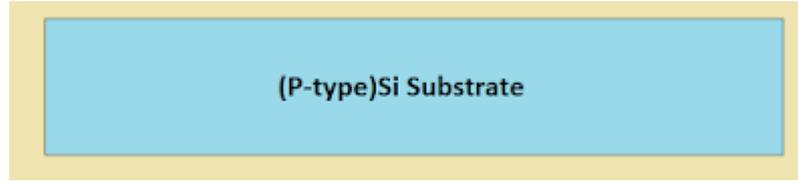
# Metalizzazione - sputtering



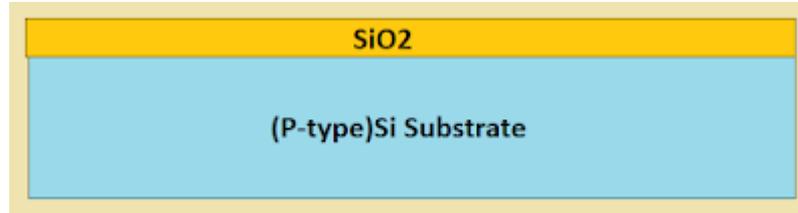
# Il processo di fabbricazione CMOS



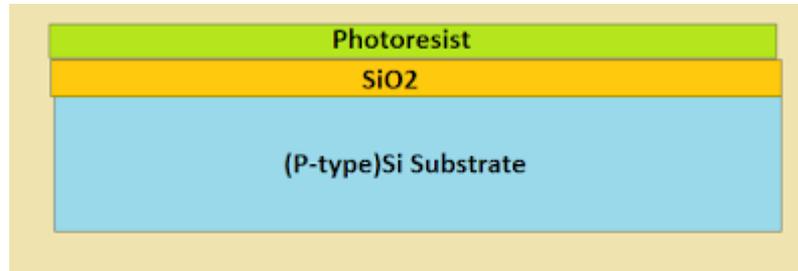
# Il processo di fabbricazione CMOS



Il substrato

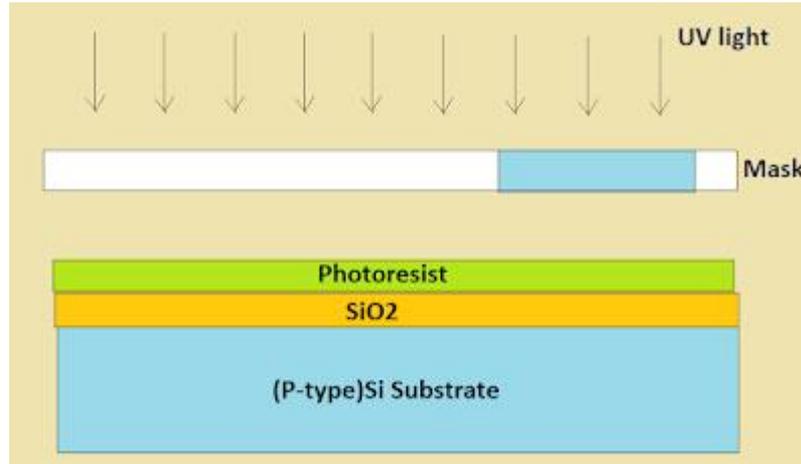


L'ossidazione

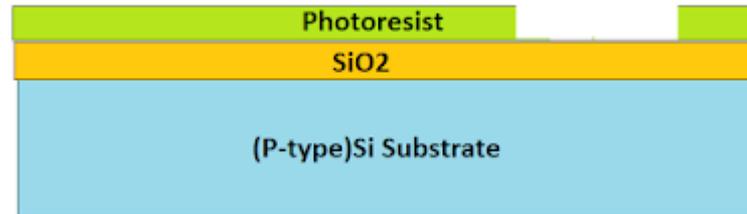


Il fotoresist

# Il processo di fabbricazione CMOS

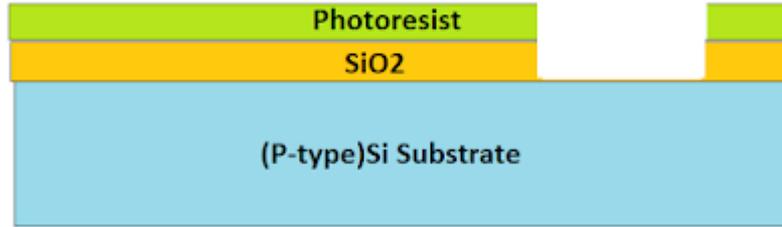


Maschera e  
Irraggiamento UV

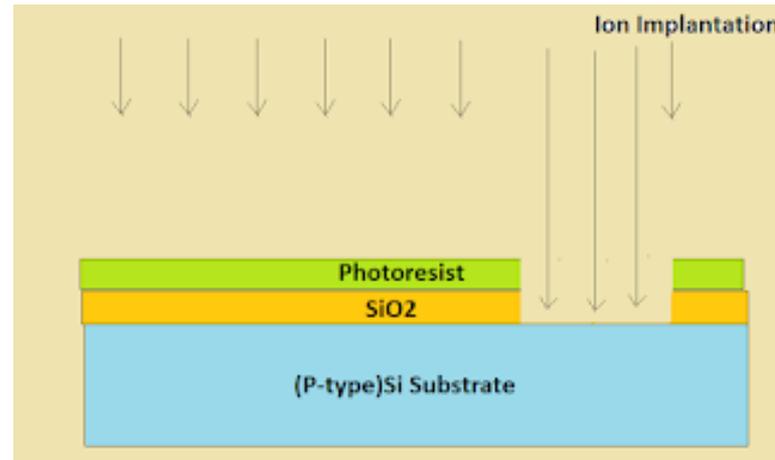


Rimozione del  
fotoresist

# Il processo di fabbricazione CMOS

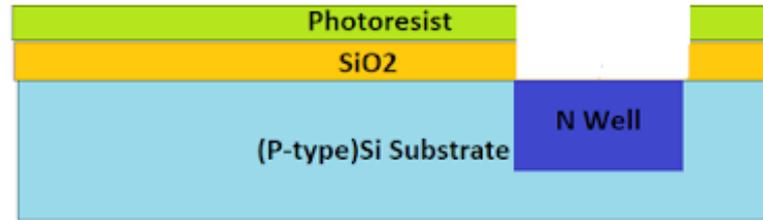


Etching SiO<sub>2</sub>

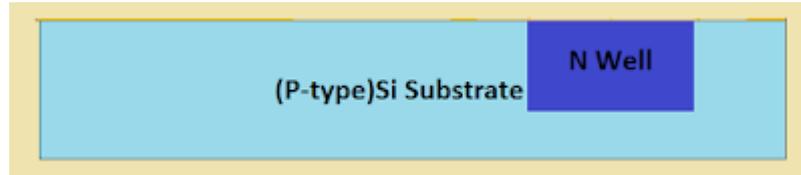


Impiantazione ionica

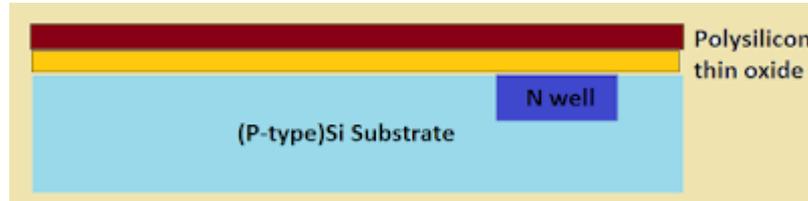
# Il processo di fabbricazione CMOS



Formazione del N well

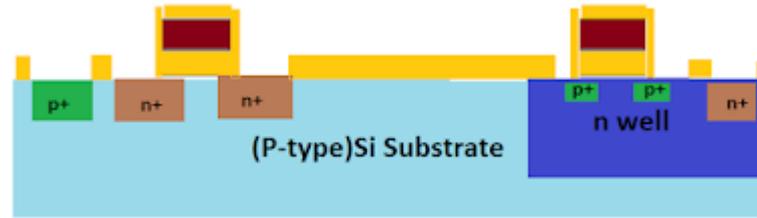


Rimozione del fotoresist  
e SiO2

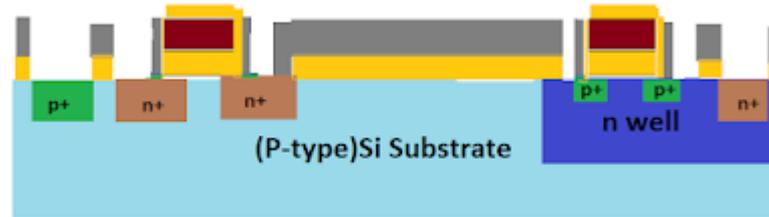


Deposizione di uno strato  
sottile di SiO2 e di uno di  
polisilicio.

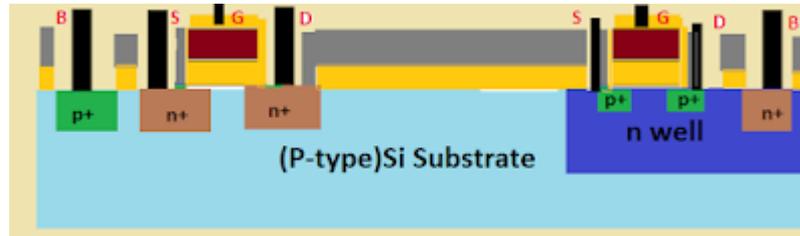
# Il processo di fabbricazione CMOS



Impiantazioni N e P



Metalizzazione



Isolamento e  
contattazione.



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Dipartimento di  
Ingegneria  
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# Grazie per l'attenzione!

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