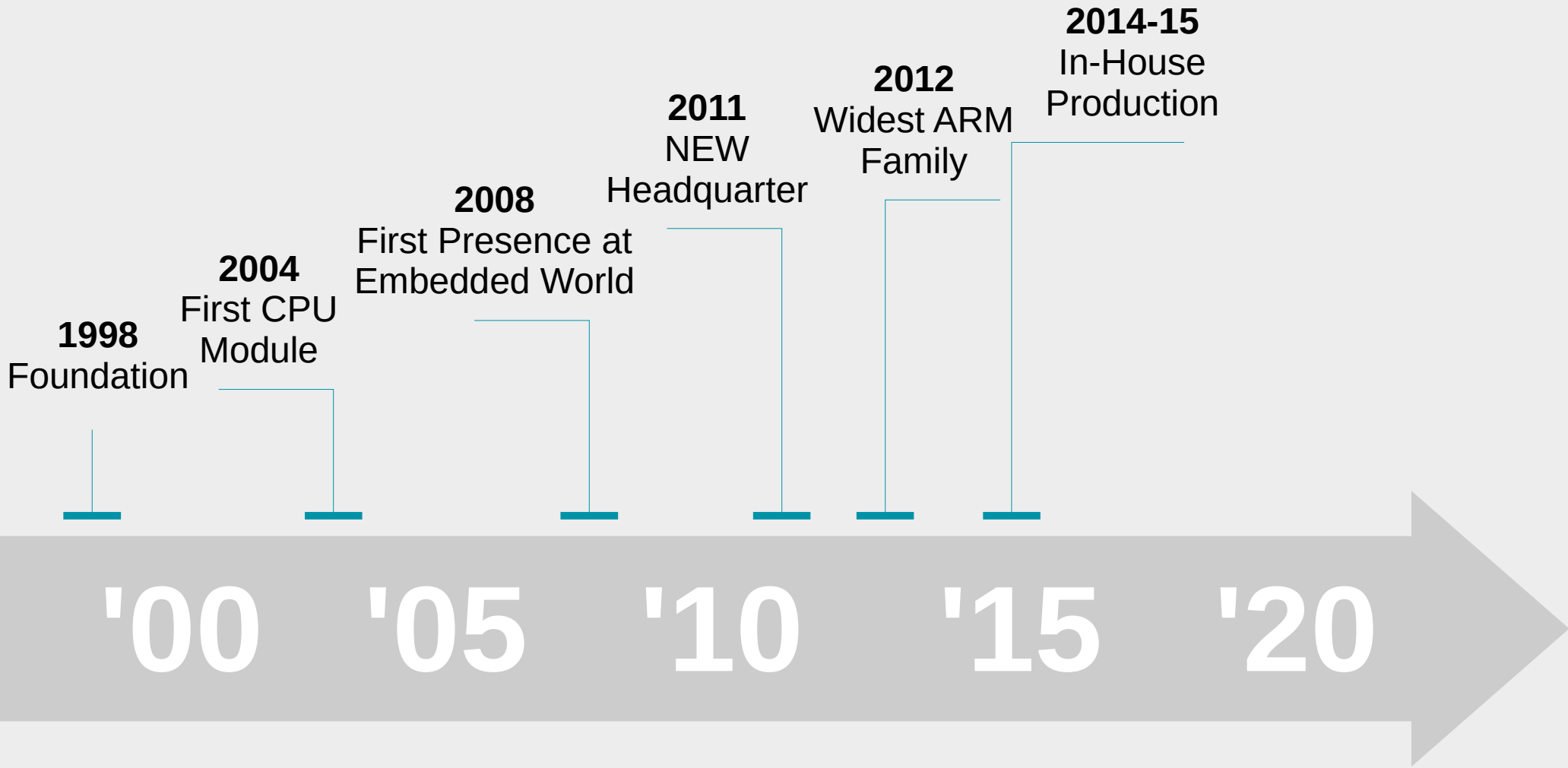


University Seminars 2016

- Andrea Marson
- R&D Manager
- 15+ years of experience on embedded systems
- <https://www.linkedin.com/in/marsonandrea>
- andrea.marson@dave.eu

- Introduction
- DAVE Embedded Systems' presentation
- Brief introduction to Xilinx Zynq architecture and state-of-the-art FPGA development techniques
- Internship/thesis proposals and real cases



DAVE Embedded Systems deals with design, manufacturing and testing of embedded systems since 1998. Our products are used by customers in different markets such as automation, telecommunication, biomedical, computer vision, image/video processing, transportation etc.

What is an embedded system?

An embedded system is a computer system with a dedicated function within a larger mechanical or electrical system, often with real-time computing constraints. It is embedded as part of a complete device often including hardware and mechanical parts. By contrast, a general-purpose computer, such as a personal computer, is designed to be flexible and to meet a wide range of end-user needs. Embedded systems control many devices in common use today.

source: Wikipedia





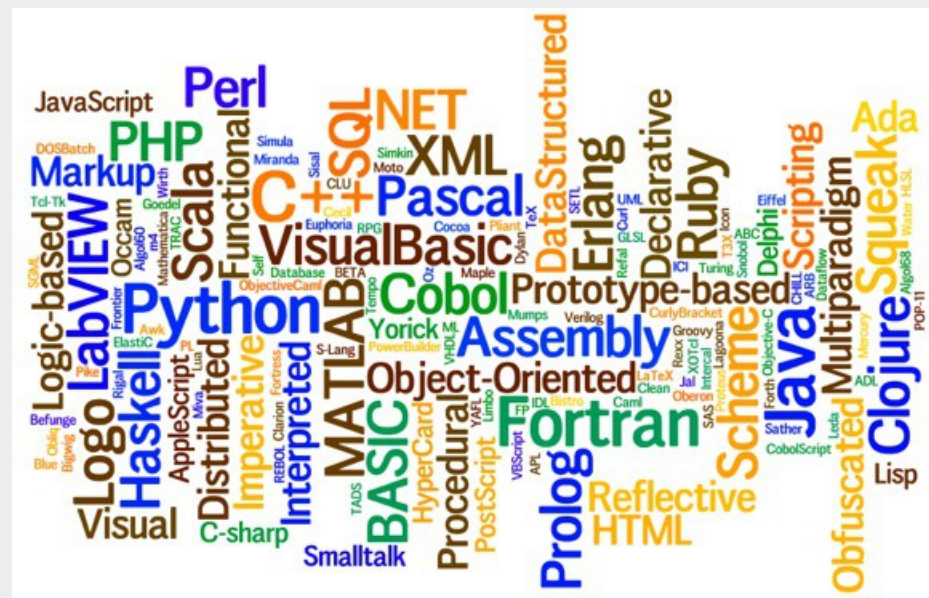
A concern expressed by many in the industry is that the “anyone can program” philosophy that is associated with the Raspberry Pi [and Arduino Ed.] tends to ignore the complexity involved in creating software for real-world systems and perhaps even devalues the engineering skills involved. For example, software for use in industrial systems must be developed in compliance with international standard IEC 61508, while developers of automotive systems must adhere to ISO 26262. Meeting these challenging and complex standards involves a wide range of different engineering skills.

It is fair to say that the Embedded Systems industry understands the motivation behind the Raspberry Pi and the need to encourage ‘programmers’ rather than ‘operators’. Certainly the Pi does expose young people to the ‘magic’ that a microprocessor is able to deliver. Looking forward, it will be interesting to see how many of the Pi generation go on to become professional embedded systems engineers.

source: <http://www.cambridgenetwork.co.uk/news/the-raspberry-pi-hero-or-zero-an-industry-perspective/>



- Most of European electronics manufacturing industry moved to Far East
- Nowadays most of added value is created in the software domain





DAVE Embedded Systems' HEADQUARTER
Via Talponedo, 29/A
33080 Porcia, Italy

DAVE Embedded Systems' BRANCH OFFICE
Maximilianstrasse, 13
80539 München, Germany



EUROPE

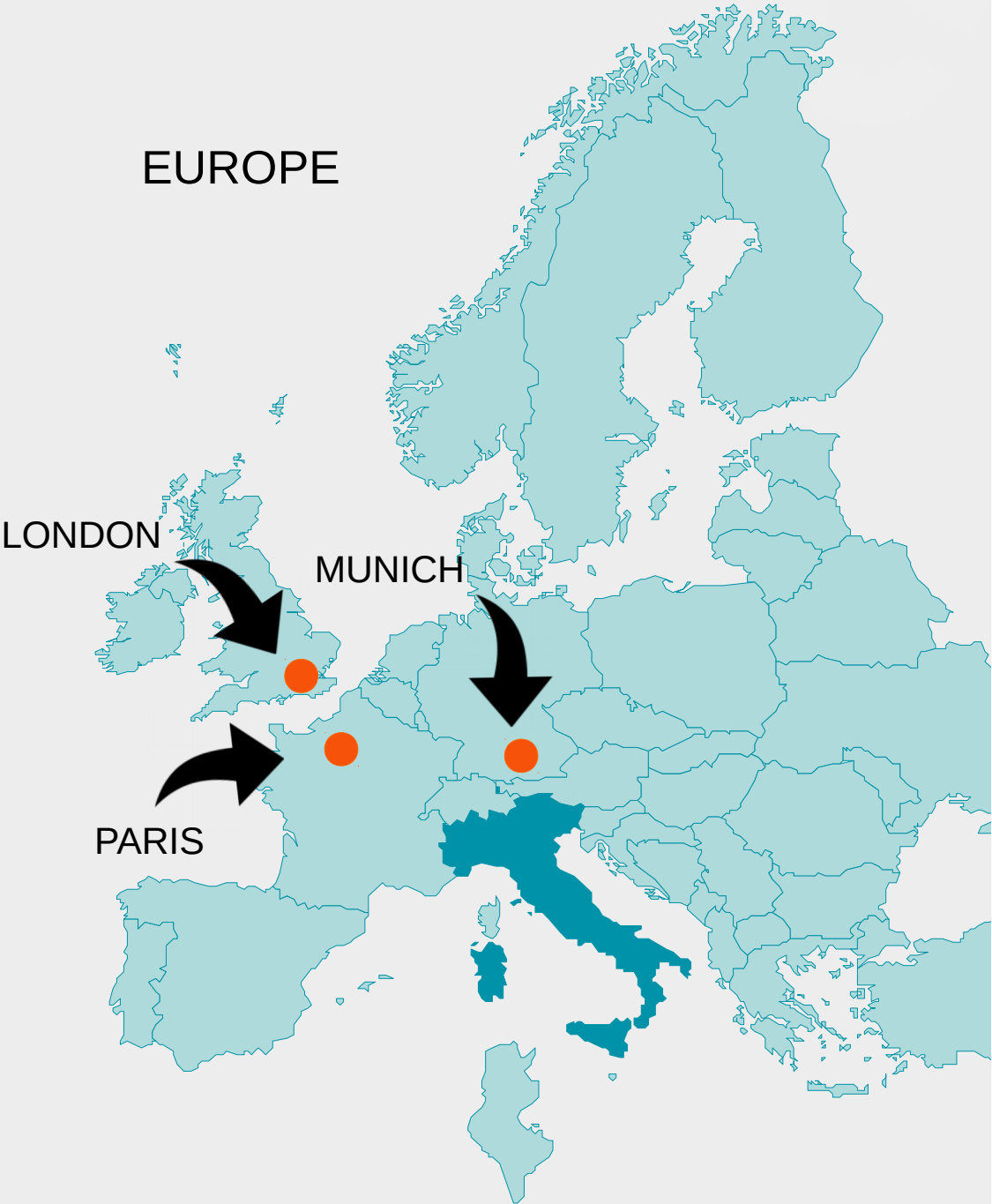
U.S.A.

LONDON

MUNICH

PARIS

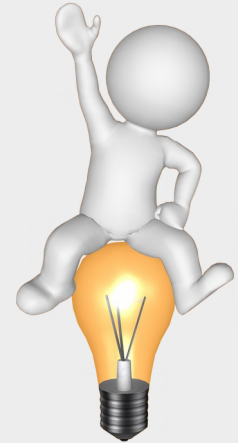
S.FRANCISCO



- Company Turnover → 3.600.000,00 €
- Company Turnover → +15% y/y
- Privately Hhelded
- Registered to “PMI innovative” list
- 20 people working



- Administration and Sales → 5
- R&D → 8
- Technical Support → 2
- Production → 6
- Interns → 2





PMI Innovative

Per prendere parte a questo progetto è necessario possedere almeno due dei tre requisiti “formativo-culturali” richiesti: investire in ricerca e sviluppo più del 3% del costo della produzione, avere un team formato per 1/3 da personale in possesso di laurea magistrale; ed essere depositari o licenziatari di brevetto o titolare di software registrato.

DAVE Embedded Systems pone un'attenzione costante nella formazione dei propri dipendenti.

Fa parte di quelle aziende in cui si è scelto di investire fortemente in Ricerca e Sviluppo, punti cardine attorno ai quali si sviluppa la nostra attività.

I soci dell'azienda e la maggior parte dei dipendenti ha scelto di approfondire il proprio percorso formativo conseguendo una laurea.

Il nostro team è composto da personale altamente qualificato e che si mantiene costantemente aggiornato.

In un'ottica di continua e costante crescita, DAVE Embedded Systems ha instaurato negli anni relazioni professionali con partner locali e internazionali.

Con l'obiettivo di investire in formazione DAVE Embedded Systems collabora attivamente con alcuni importanti poli universitari, tenendo conferenze a tema.

L'azienda svolge attività di divulgazione partecipando a congressi e meeting.



MANUFACTURERS



DISTRIBUTORS



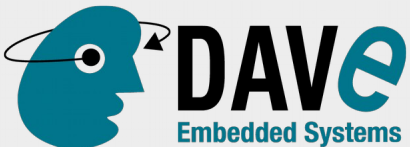
TECHNICAL PARTNERS

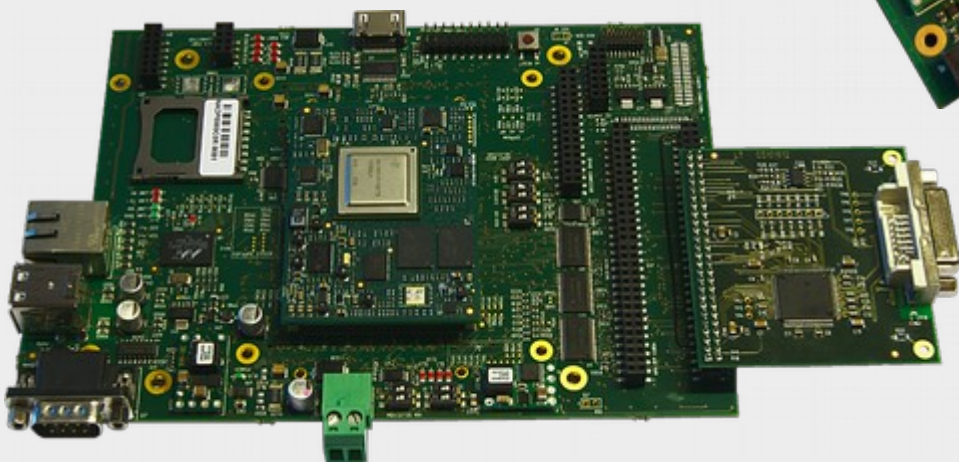
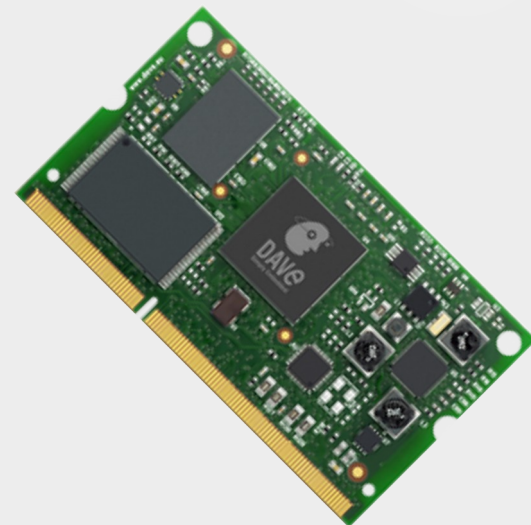
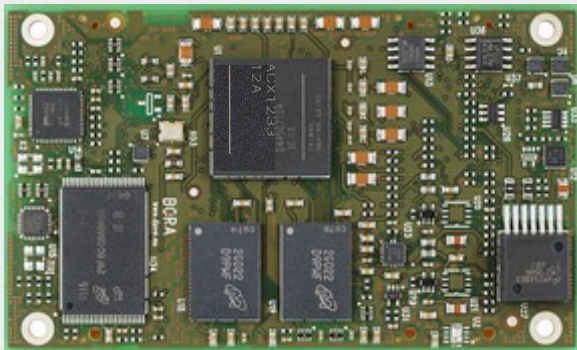


CUSTOMERS (B2B)



END CUSTOMERS (B2B / B2C)





CPU Modules (aka SoM = System on Module)

Ultra

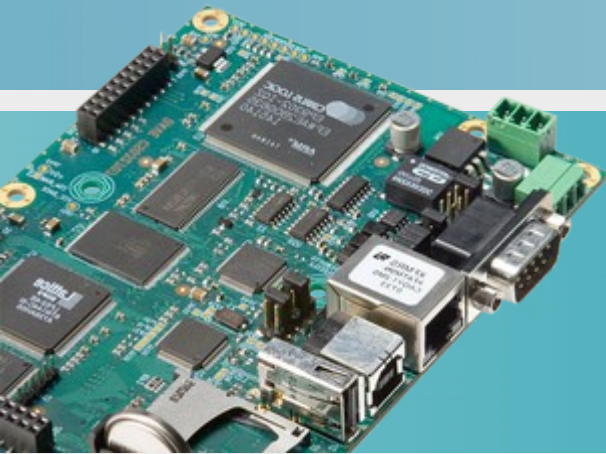
Esatta

Lite



Single Board Computers (SBC)

Custom Systems



Ultra

T.o.P
PCIe
FPGA
100G Shock

Esatta

P2P Comp.
DSP
Video

50G Shock
Computation
Connections

Lite

Temperature

Reliability

Size

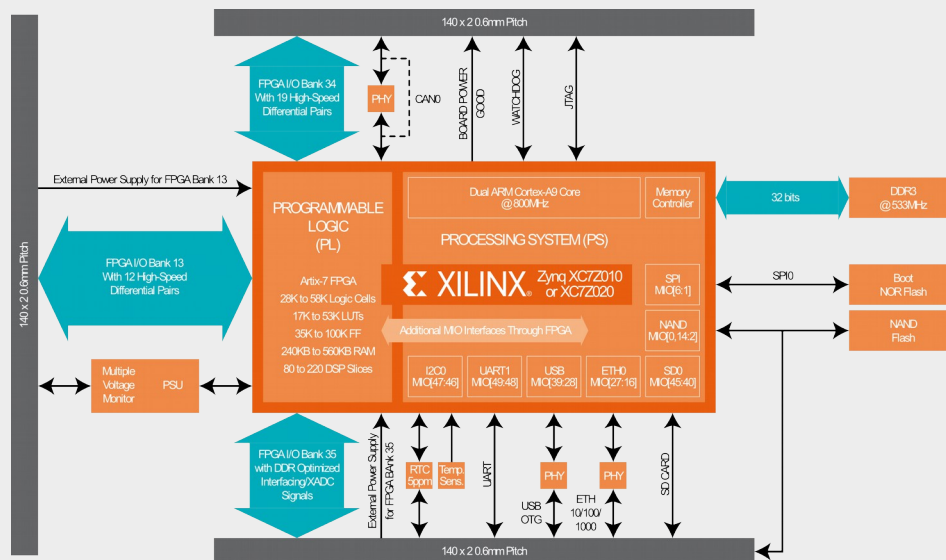
Quality

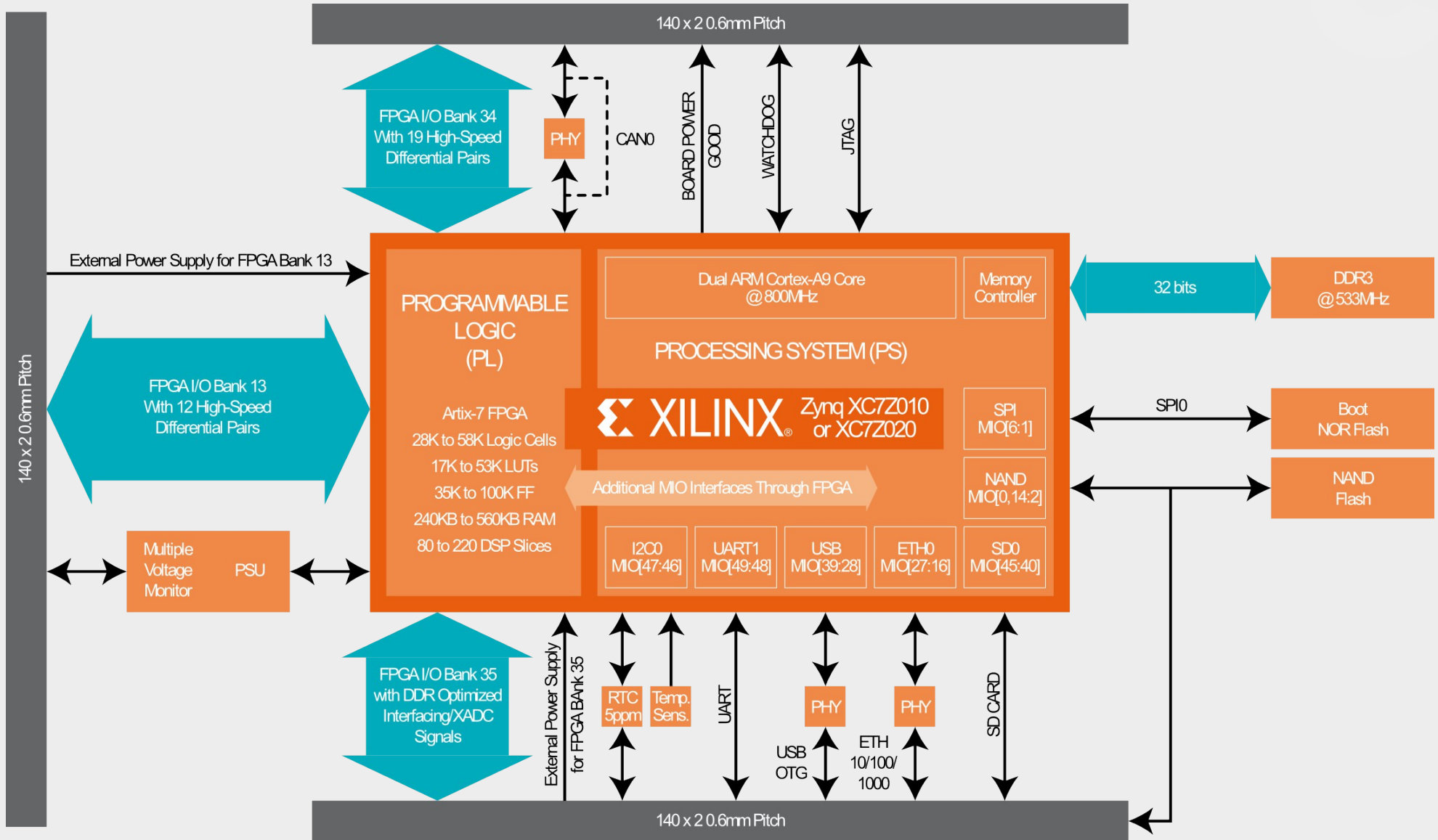
- Unmatched performance thanks to dual ARM Cortex-A9 @ 800MHz
- Enabling smarter system thanks to Artix-7 FPGA integrated on chip
- Highest security and reliability: voltage monitoring and power good enable
- Accurate timing application thanks to on-board 5ppm RTC

Top view



Bottom view





BORA Embedded Linux Kit provides all the necessary components required to set up the developing environment for:

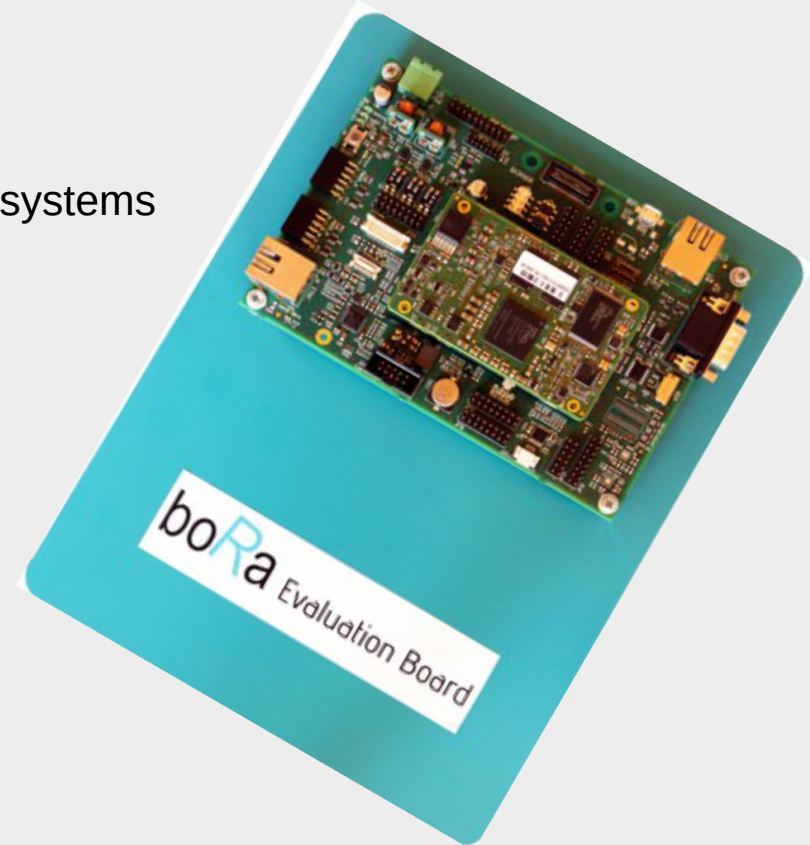
- configuring the system (PS and PL) at hardware level
- build the first-stage bootloader (FSBL)
- building the second stage bootloader (U-Boot)
- building and running Linux operating system on Bora-based systems
- building Linux applications that will run on the target

The main kit components are:

- BORA SOM
- BORA-EVB-Lite Carrier board
- AC/DC Single Output Wall Mount adapter
Output: +12V -2.0 A
- MicroSDHC card with SD adapter and USB adapter

Vivado/SDK can be viewed as a collection of programs required to deal with all of the development aspects related to Xilinx components

(software running on ARM cores, FPGA fabric verification and programming, power estimation etc.). These include strictly FPGA-related tools such as Floorplanner and pure-software development tools such as SDK.



PIN CONFIGURATION DEPEND ON WORKING MODE
SEE USER GUIDE FOR DETAILS

RS232/422/485

ETHERNET

ETHERNET

USB HOST

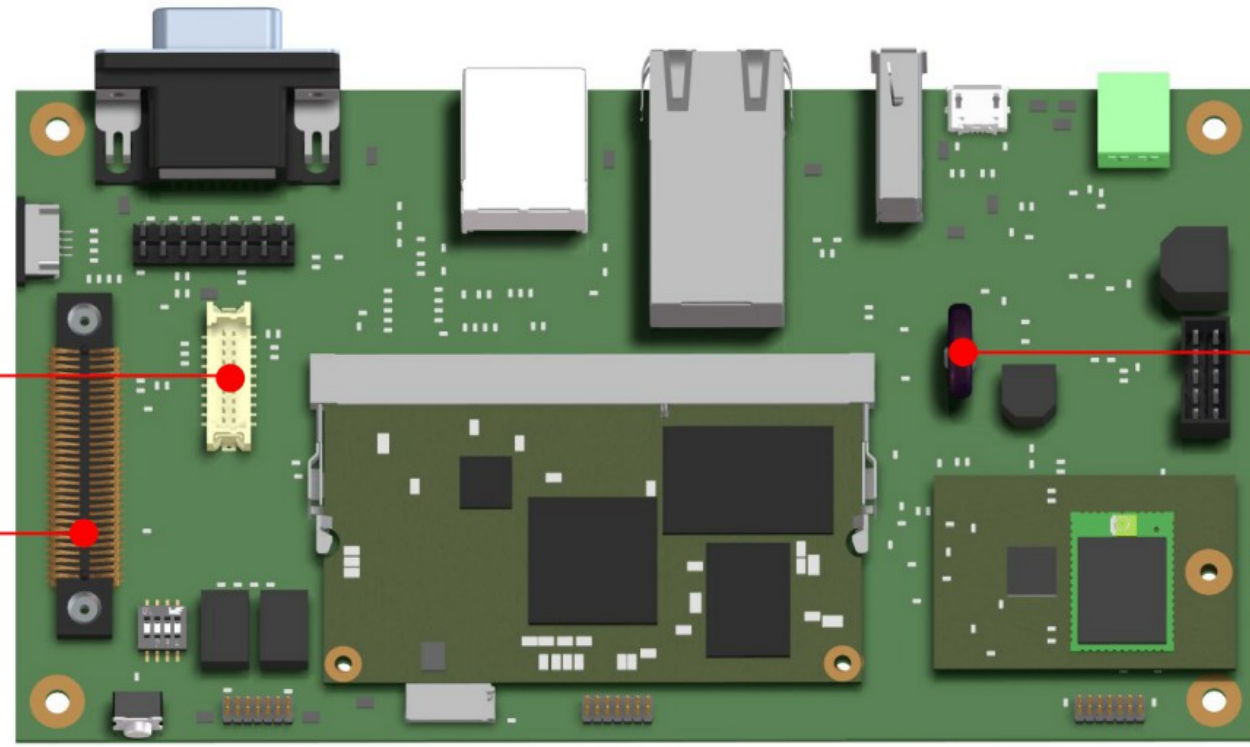
USB DEVICE

POWER SUPPLY
1: DGND
2: VIN 12-24V

RESISTIVE TOUCH SCREEN INTERFACE

2xlvds INTERFACE
SEE MANUAL FOR DETAILS

WIDE INTERFACE
SEE MANUAL FOR DETAILS



BATTERY

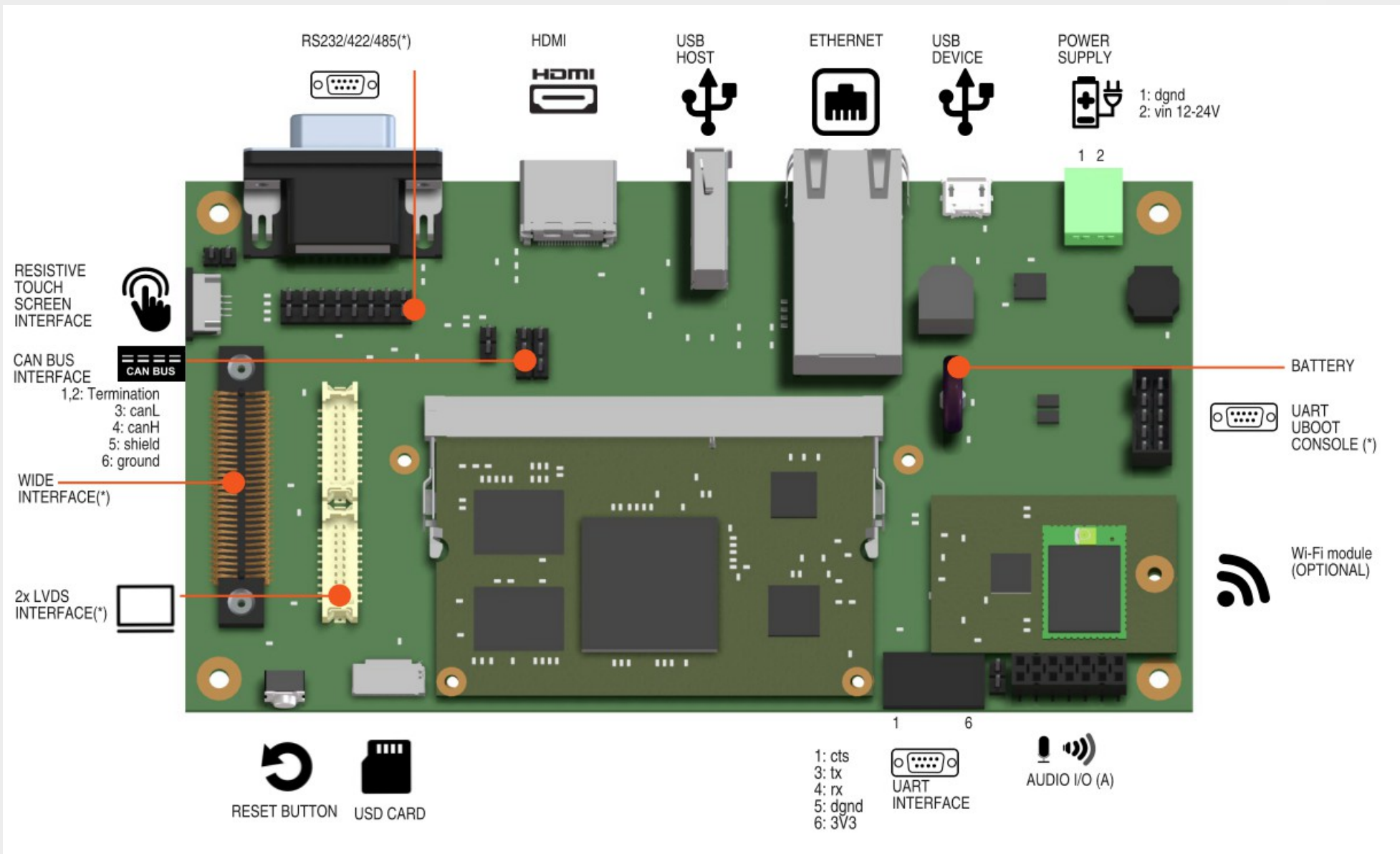
Wi-Fi module (OPTIONAL)

RESET BUTTON

CAN BUS
1.2: Termination
3: CAN L
4: CAN H
5: shield
6: gang

UART INTERFACE

AUDIO I/O
SEE MANUAL FOR DETAILS



Remote Localization Unit

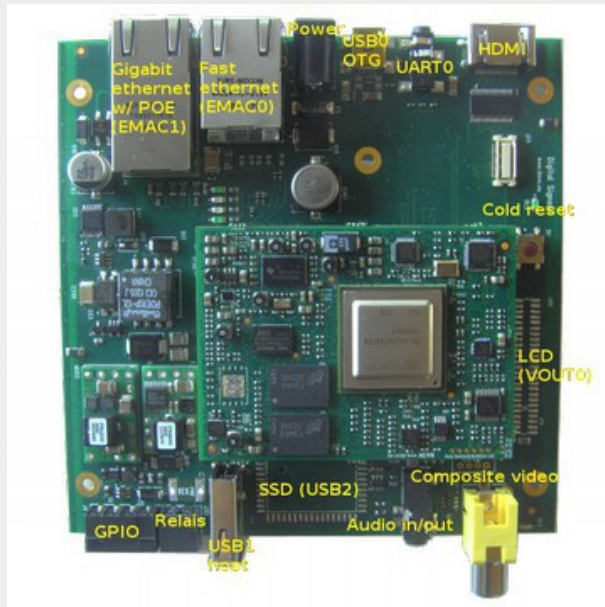
- Remote Vehicle and Safety Systems Localization & Monitoring Unit
- Neptune CPU Module
- Based on x86
- Carrier Board with Common Interfaces (USBs, Compact Flash, etc.)
- Two Boards for Monitoring Services (GPS, Accelerometer, Gyroscope) and Video Recording
- Video recording (MPEG compressed)





Passenger counting system

- Low power ARM-based CPU solution
- Fanless CPU Core for 24/7 Operation
- -40 °C to +85 °C Applications
- SoC TI DM8148 1GHz
- 750 MHz floating-point integrated DSP
- Internal Solid State Disk, Up to 16GB
- real-time operation





Application based on TI DaVinci
platform from DAVE

AViCS
Artificial Vision Counting System

Time 00:03

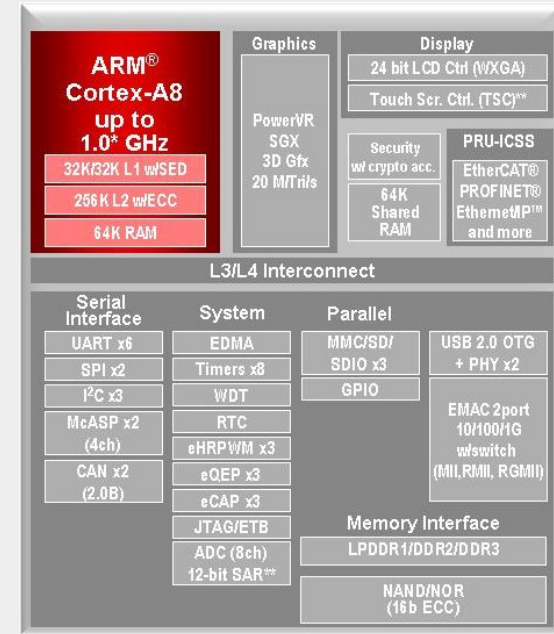
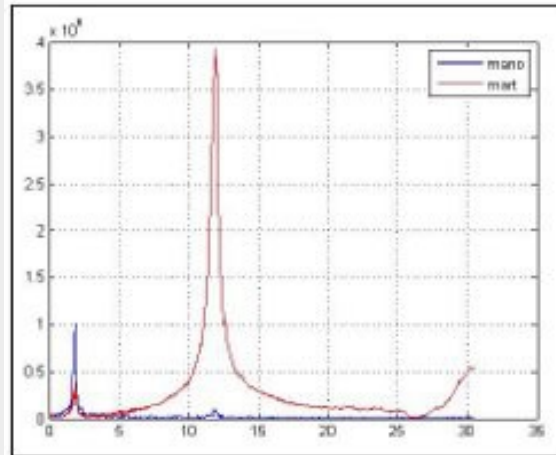
ENTRATI USCITI

00

04

Wooden poles status analyzer (X-Poles)

- battery powered
- portable
- real-time data acquisition via programmable real-time unit (PRU)
- wireless connectivity (WiFi, Bluetooth)



Directed Infrared Countermeasure system



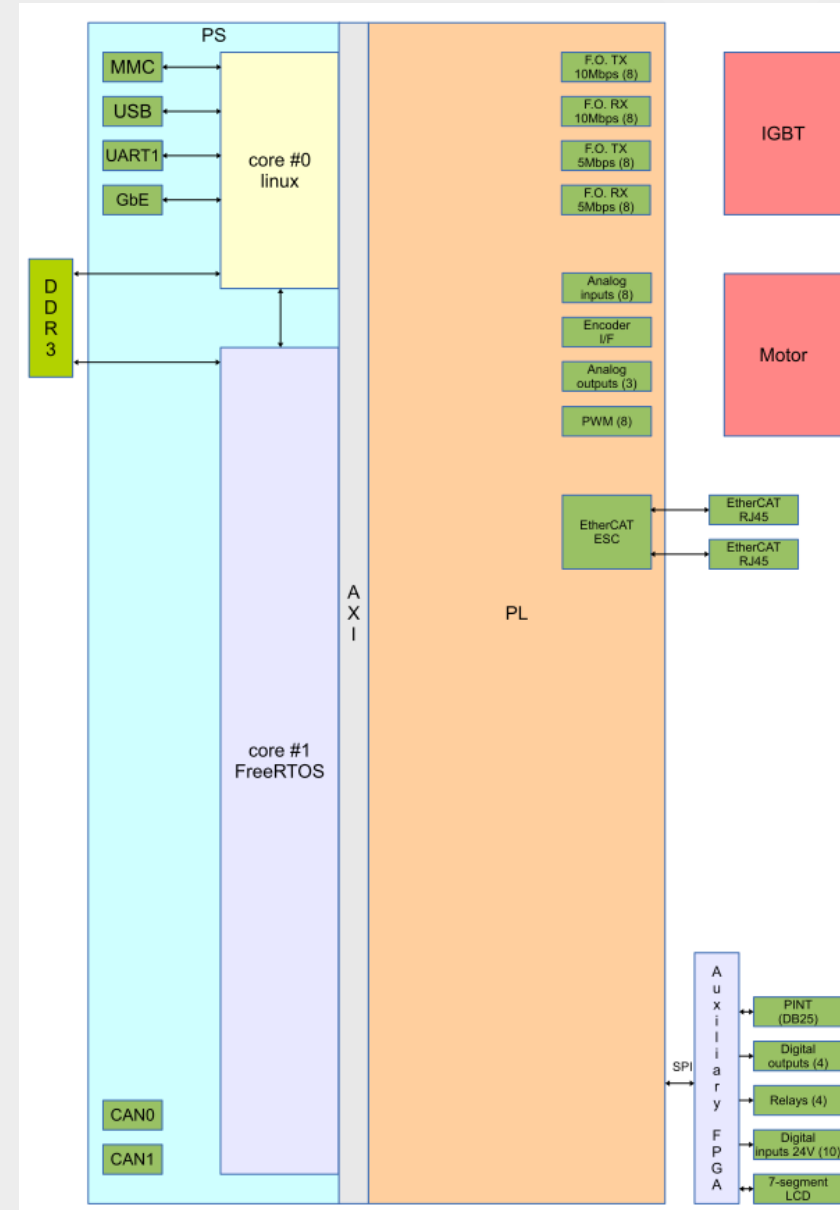
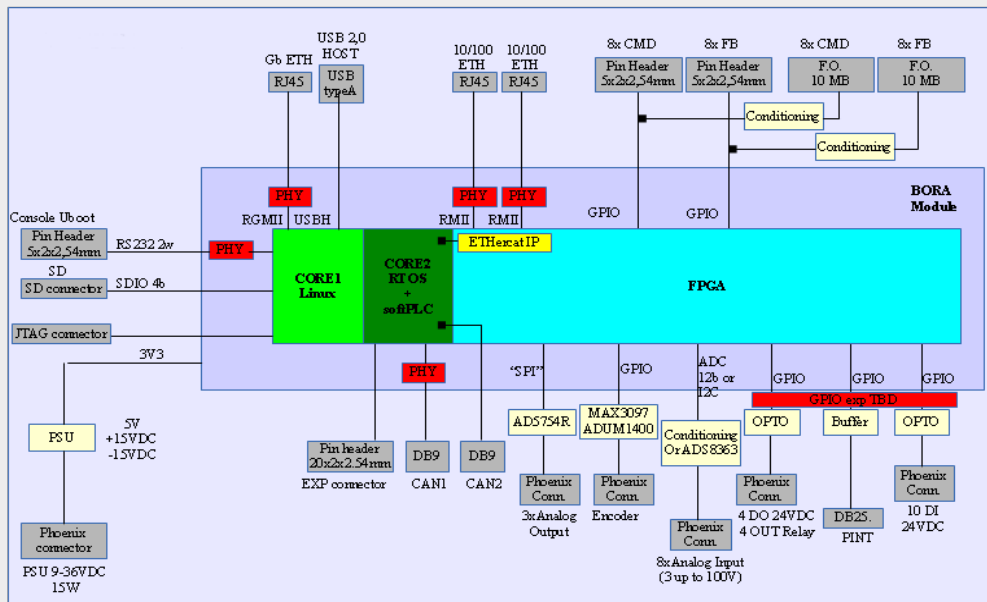
Key cutting machines

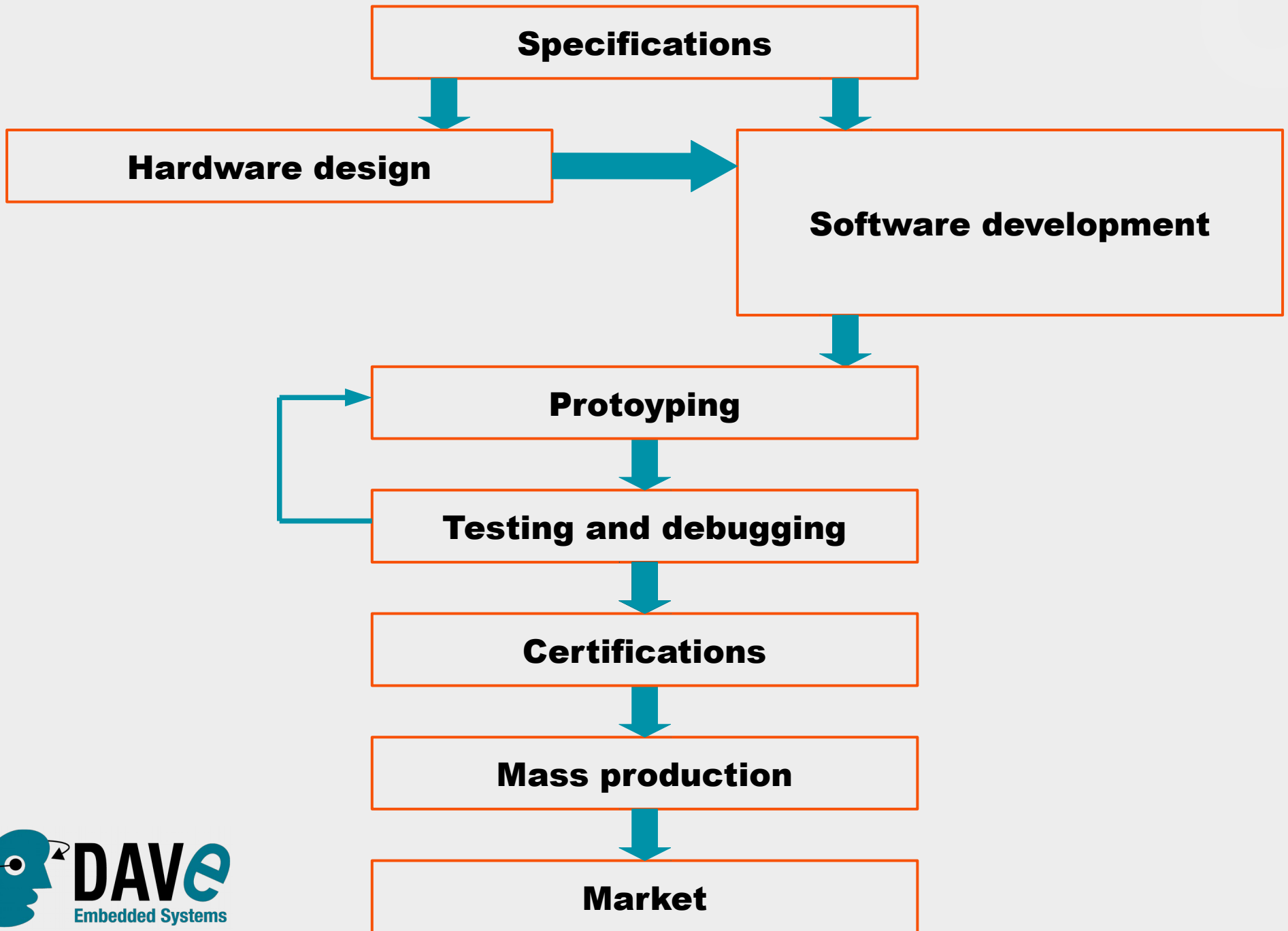
- computer vision
- integrated industrial tablet

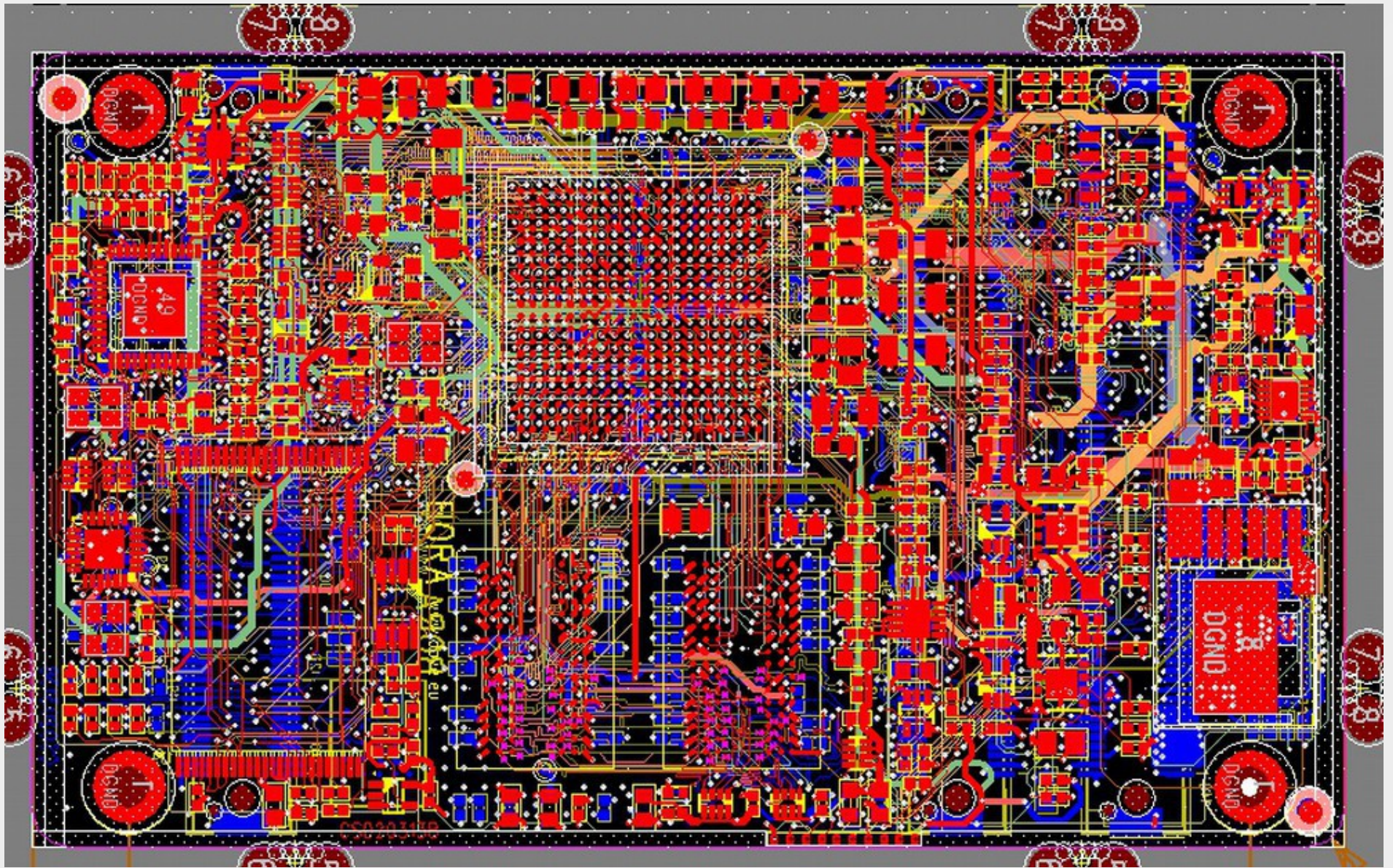


Medium voltage drives controller

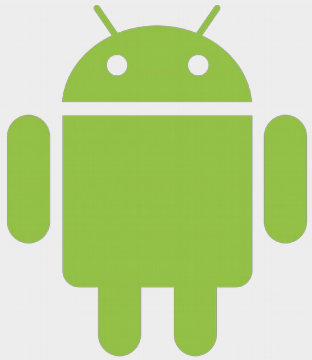
- Programmable logic Controller (PLC)
- EtherCAT slave
- hard real-time capabilities
- dual OS software architecture (Linux + FreeRTOS)



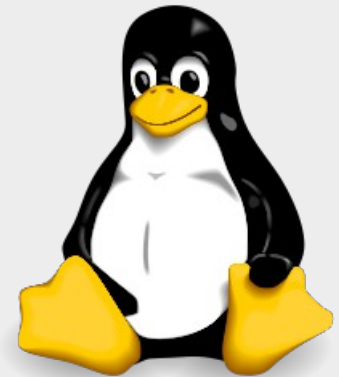
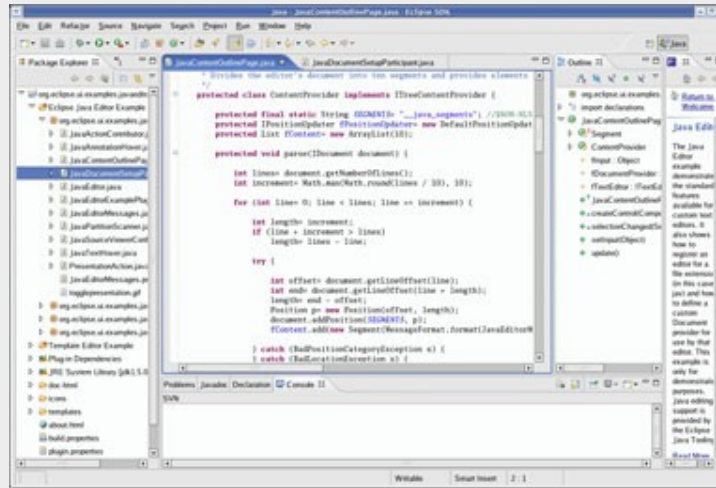








ANDROID



```
#include <stdio.h>
int main(void)
{
    printf("Hello World!\n");
    return 0;
}
```

C/C++



Code less.
Create more.
Deploy everywhere.



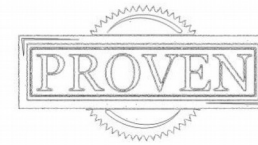
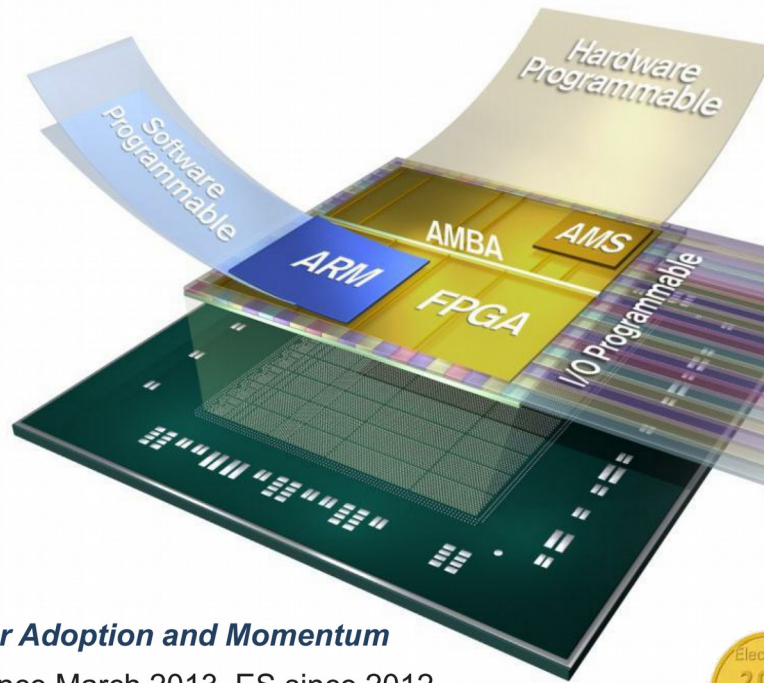


- Università degli Studi di Udine
- Università degli Studi di Padova
- Università degli Studi di Trieste
- Università degli Studi di Ferrara
- Istituto IMAMOTER CNR di Ferrara
- Istituto Tecnico. S. T. "J.F. Kennedy" di Pordenone
- Associazione Cultura Informatica (AsCI) – Udine
- Texas Instruments
- NXP/Freescale
- Xilinx



The First All Programmable SoC

ZYNQ

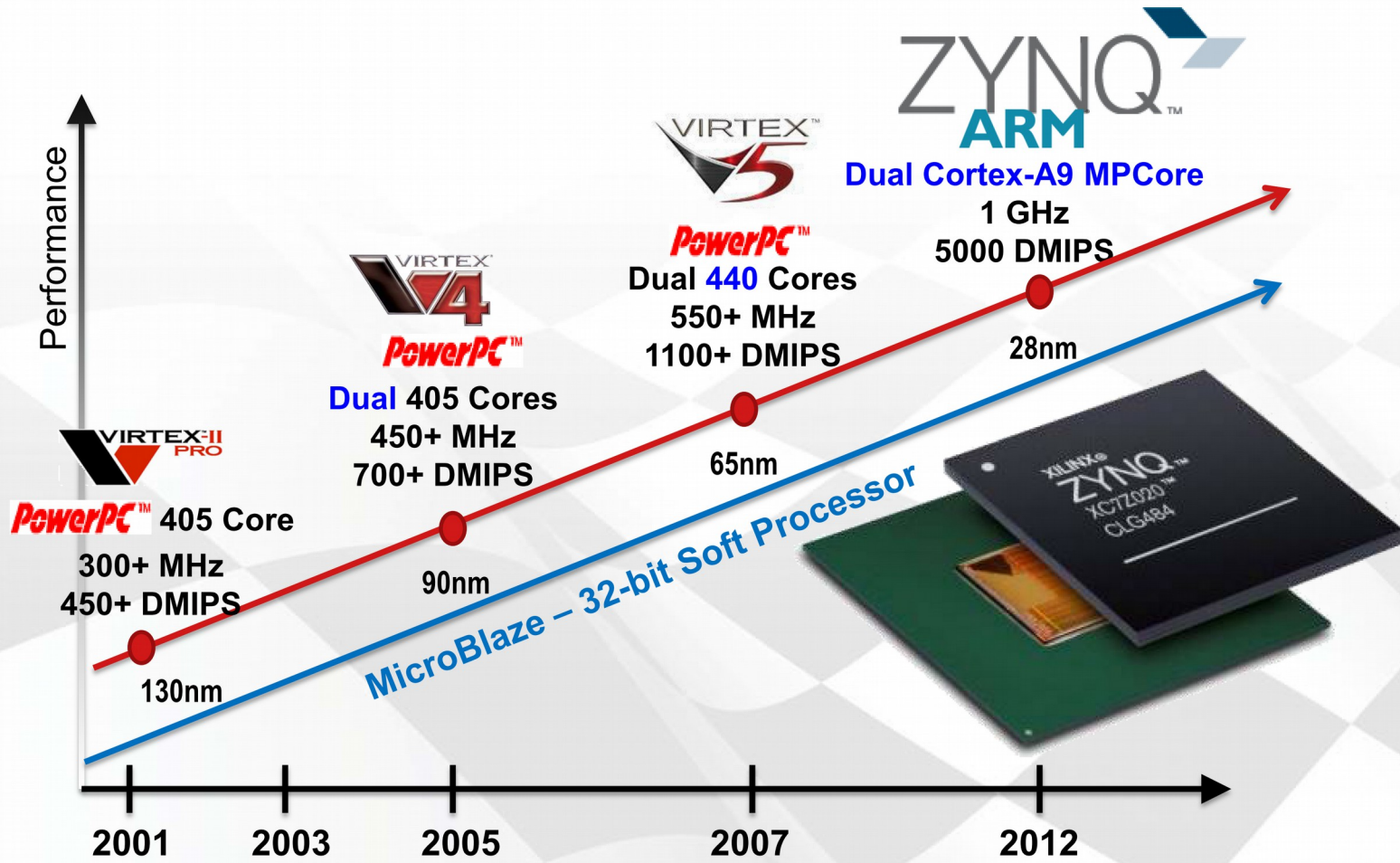


Significant Customer Adoption and Momentum

- ✓ In full production since March 2013, ES since 2012
- ✓ 500+ unique customers actively designing
- ✓ 100+ Zynq specific partners
- ✓ All major OSs supported and in use
- ✓ 20+ different development boards and SOMs

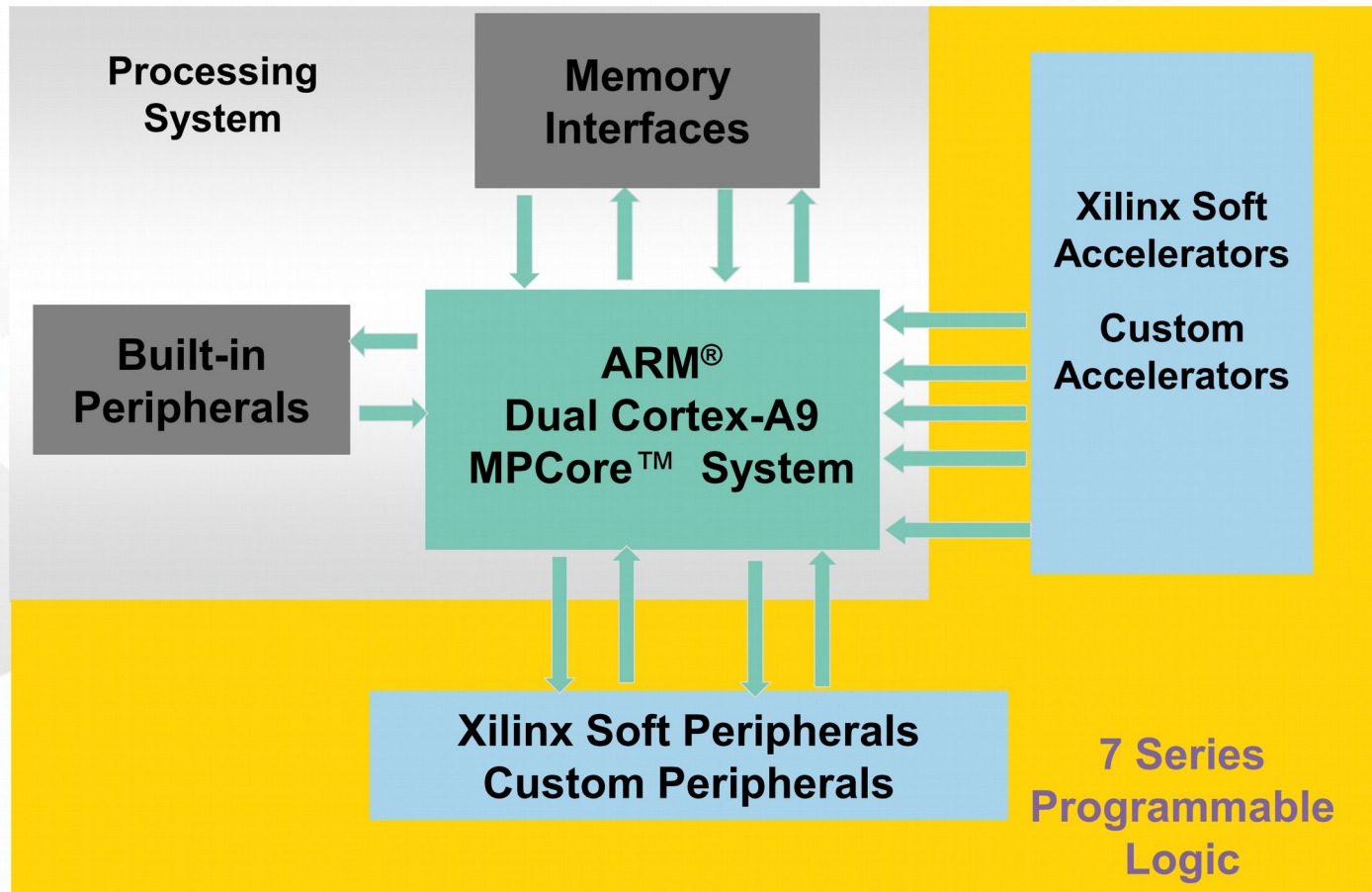


Xilinx Processing Heritage

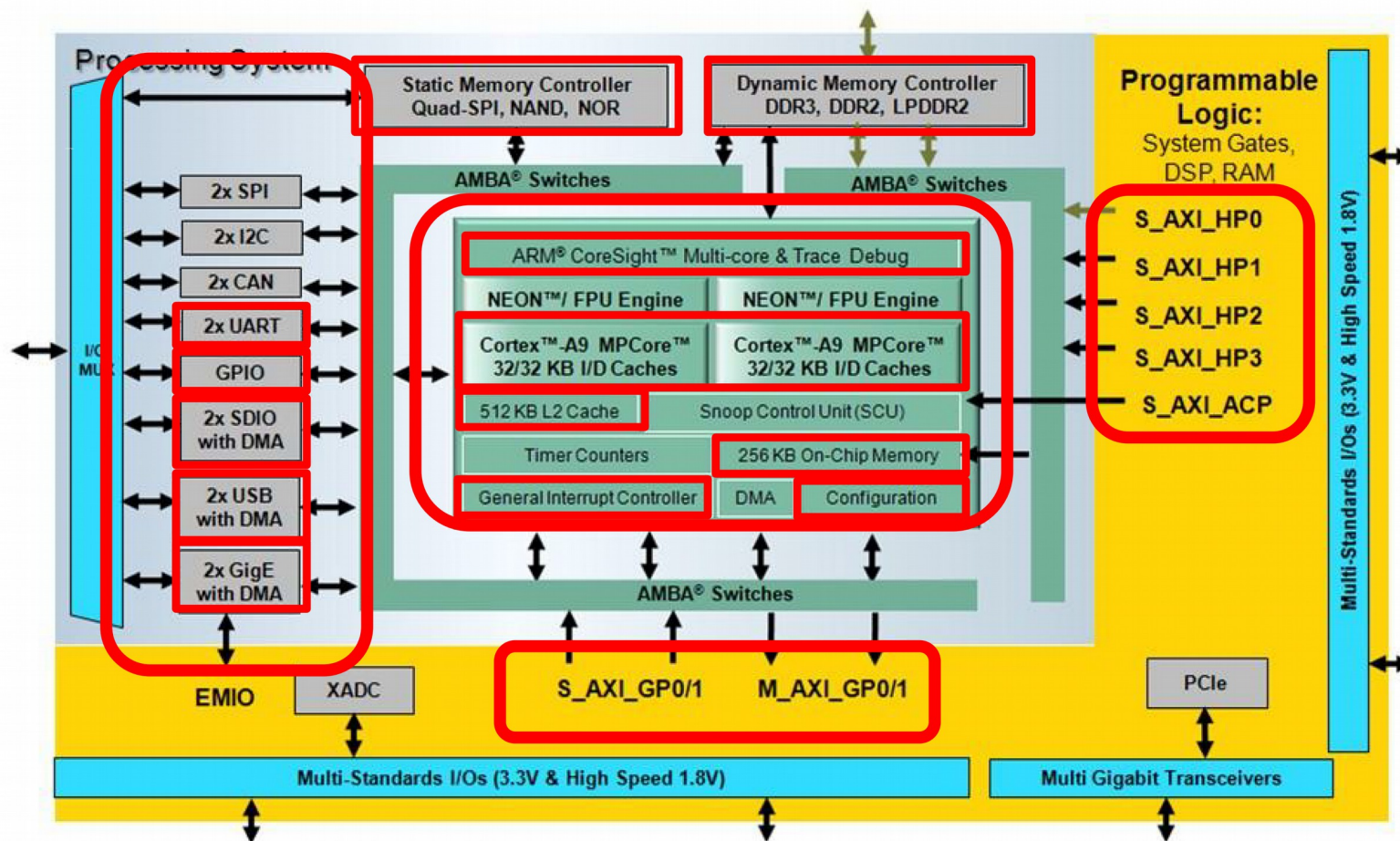


10+ years, 4 Generations

Zynq-7000 AP SoC Basic Architecture



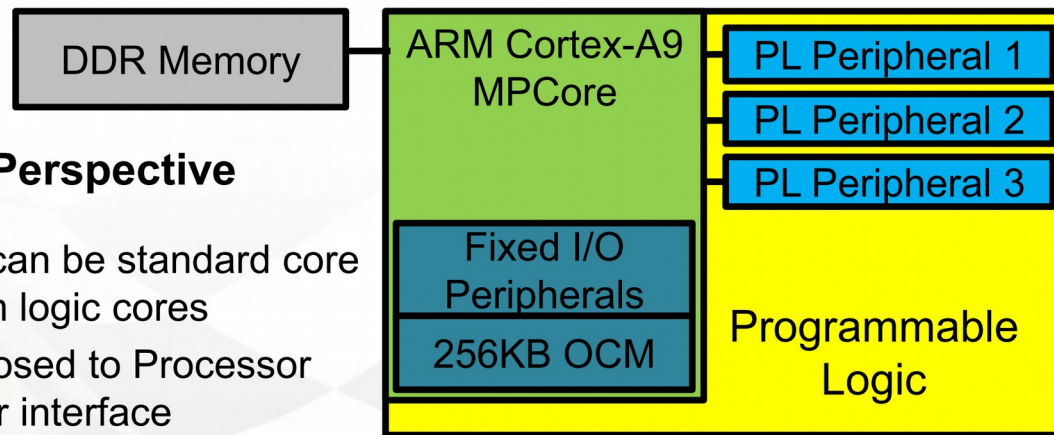
Zynq-7000 AP SoC Block Diagram



Connecting HW and SW

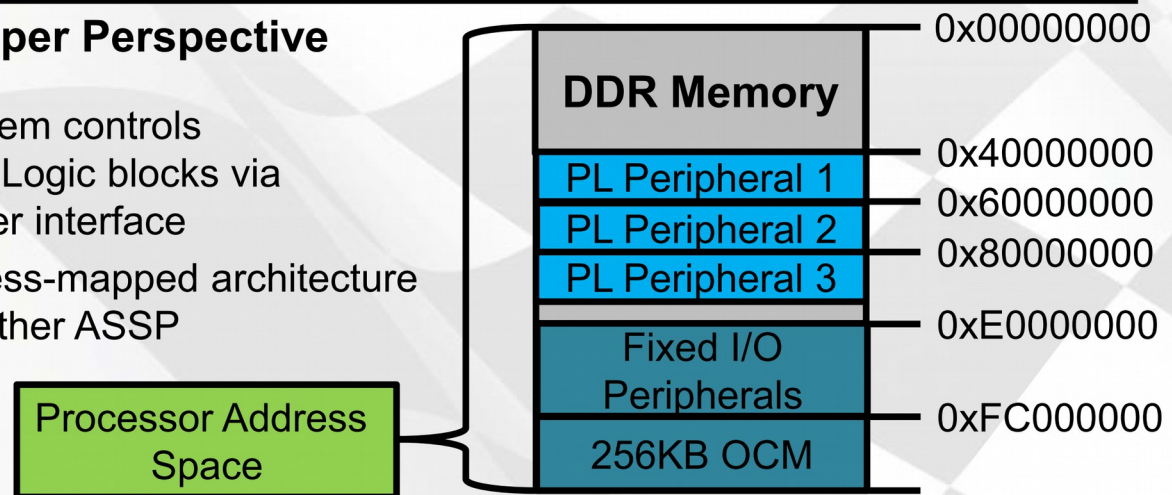
Hardware Designer Perspective

- Peripheral blocks can be standard core offerings or custom logic cores
- Logic controls exposed to Processor System via register interface

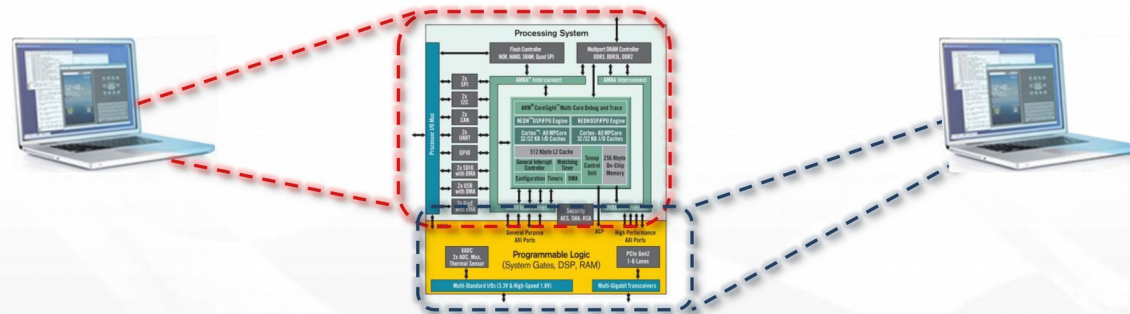


Software Developer Perspective

- Processor System controls Programmable Logic blocks via exposed register interface
- Standard address-mapped architecture similar to any other ASSP



Parallel Developments of your AP SoC Based Application



Software Development

- Processor boots first like any ARM based SoC.
- SW developers can use their favorite SW tool to load / debug SW code over JTAG
- Programmable Logic can be left unconfigured while developing on real hardware

Hardware Development

- Reference SW boots processor first leaving PL up and ready to be programmed through JTAG
- Vivado Probe connects to Programmable Logic like to any other FPGA
- FPGA developer can start loading / debug like for any FPGA

➤ SW developments like any other ARM based SoC

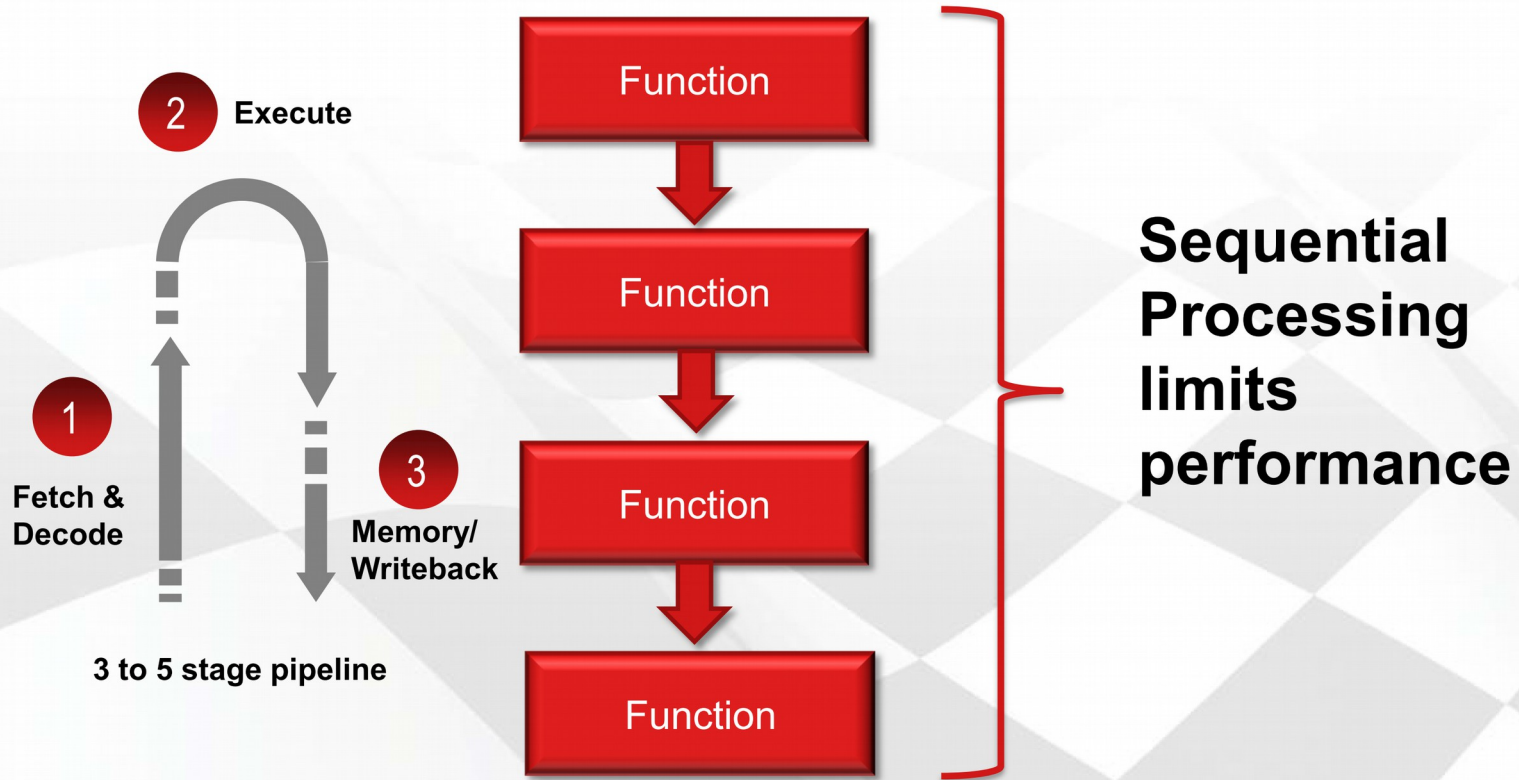
➤ HW developments like any other Xilinx FPGA

System Bottlenecked?

- **Profiling indicates processor activity**
 - Is processor utilization exceeding 90%?
 - Processor Queue Length > 2?
 - If multiprocessor system, processor time > 50%?
 - Intensive reoccurring tasks?
- **Effects of overburdened Processors include:**
 - Increased Data Latency
 - Delayed Interrupt Handling
 - Lowered Data Throughput

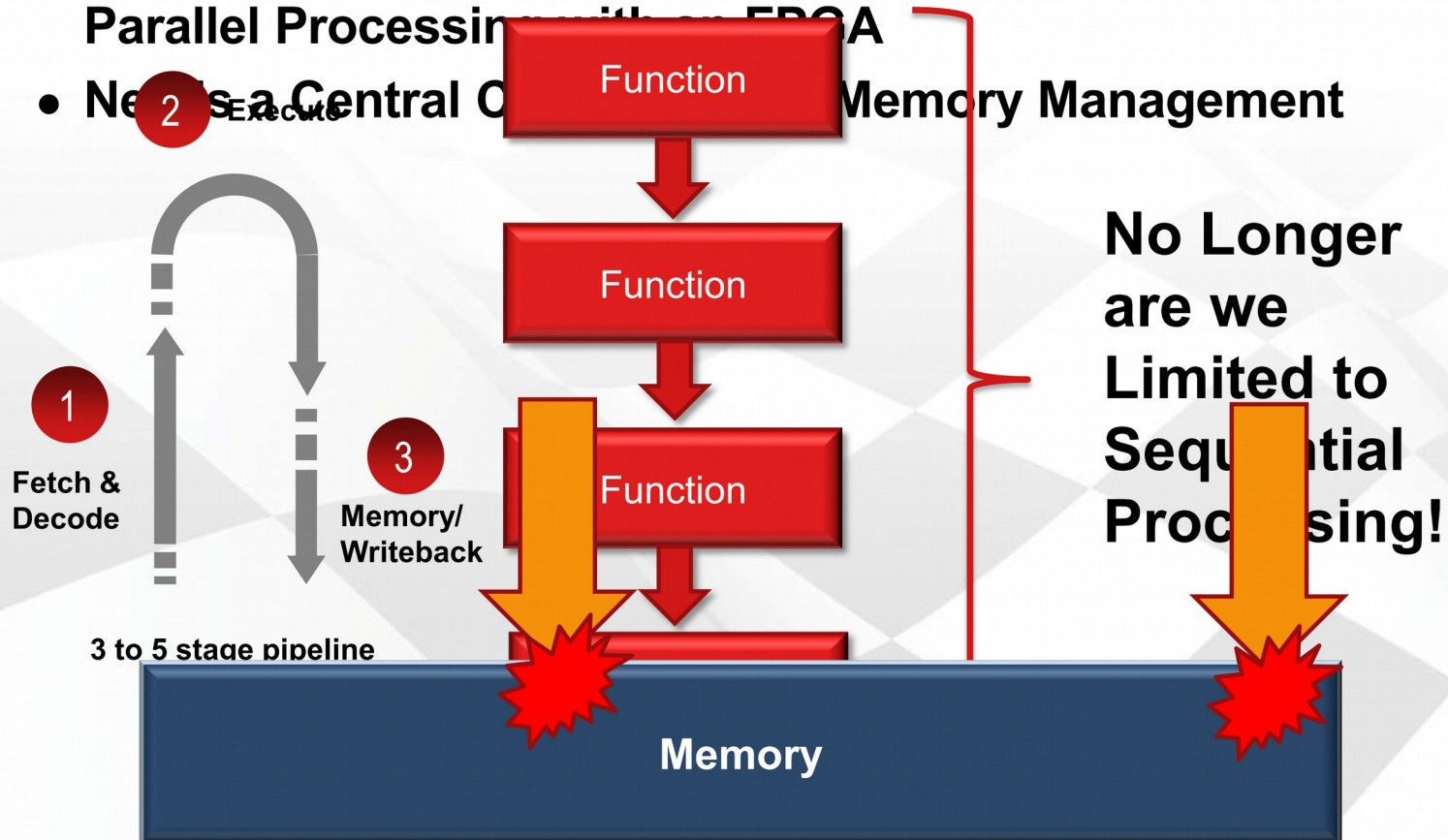


Software Engineers: Stuck in a Sequential World



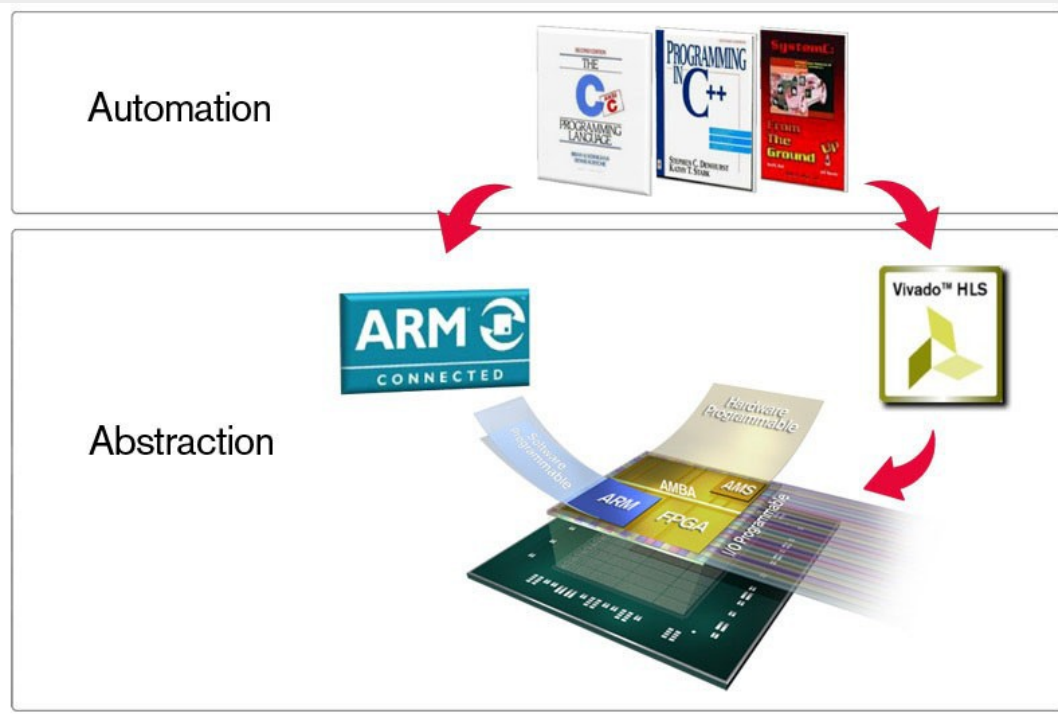
Parallel Processing is Efficient...

- For critical systems and performance, Engineers utilize Parallel Processing with an FPGA
- No longer a Central Controller Memory Management

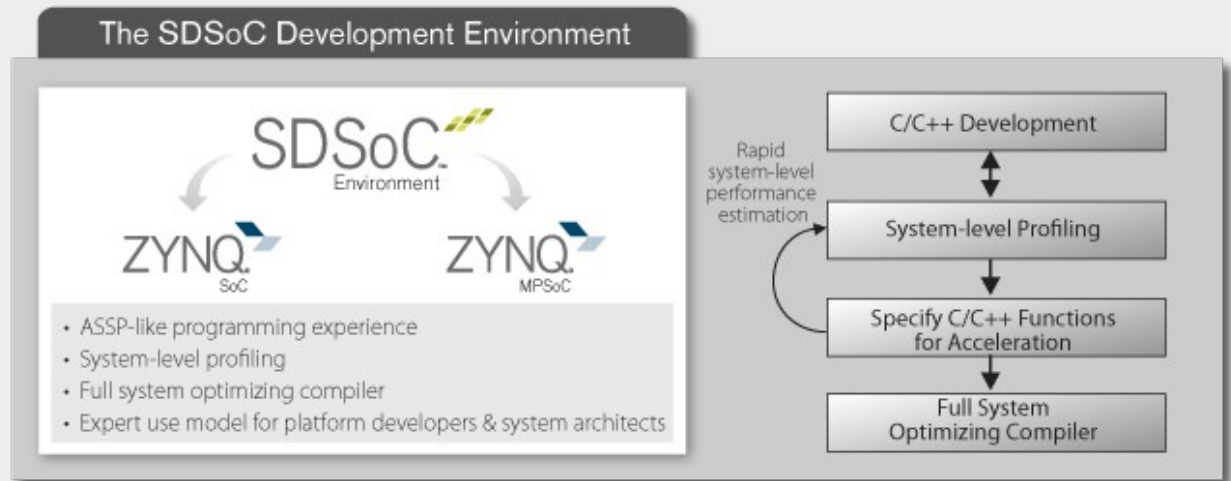


HLS

<http://www.xilinx.com/products/design-tools/vivado/integration/esl-design.html>



SDSoC



<http://www.xilinx.com/products/design-tools/sdx/sdsoc.html>

- 5G Wireless
- ADAS
- Cloud Computing
- Industrial IoT
- SDN (Software Defined Network)/NFV (Network Function Virtualization)
- Video/Vision

source: <http://www.xilinx.com/alliance/featured-solution-partners/solutions-by-megatrend.html>



sources:

- <http://bcove.me/ruyd02ca>
- blogs.intel.com





ALL PROGRAMMABLE™



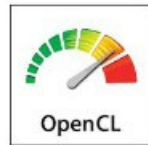
High frequency trading



E-commerce



Cloud computing



"Xilinx needs a new generation of design environments that abstract away the complexity of the hardware.

ICHEC really helps us with the proliferation of the design expertise as they can develop the education material that is required to train up the next generation of programmers."

Michaela Blott Principal Engineer - Xilinx Research



Microsoft Catapult

Doug Burger From Microsoft Research Talks About Project Catapult Which Will Make Bing Twice As Fast (Jun 17, 2014)



<http://microsoft-news.com/doug-burger-from-microsoft-research-talks-about-project-catapult-which-will-make-bing-twice-as-fast-video/>

Microsoft is planning to replace traditional CPUs in data centers with field-programmable arrays, or FPGAs, processors that Microsoft could modify specifically for use with its own software. These FPGAs are already available in the market and Microsoft is sourcing it from a company called Altera. The FPGAs are 40 times faster than a CPU at processing Bing's custom algorithms.



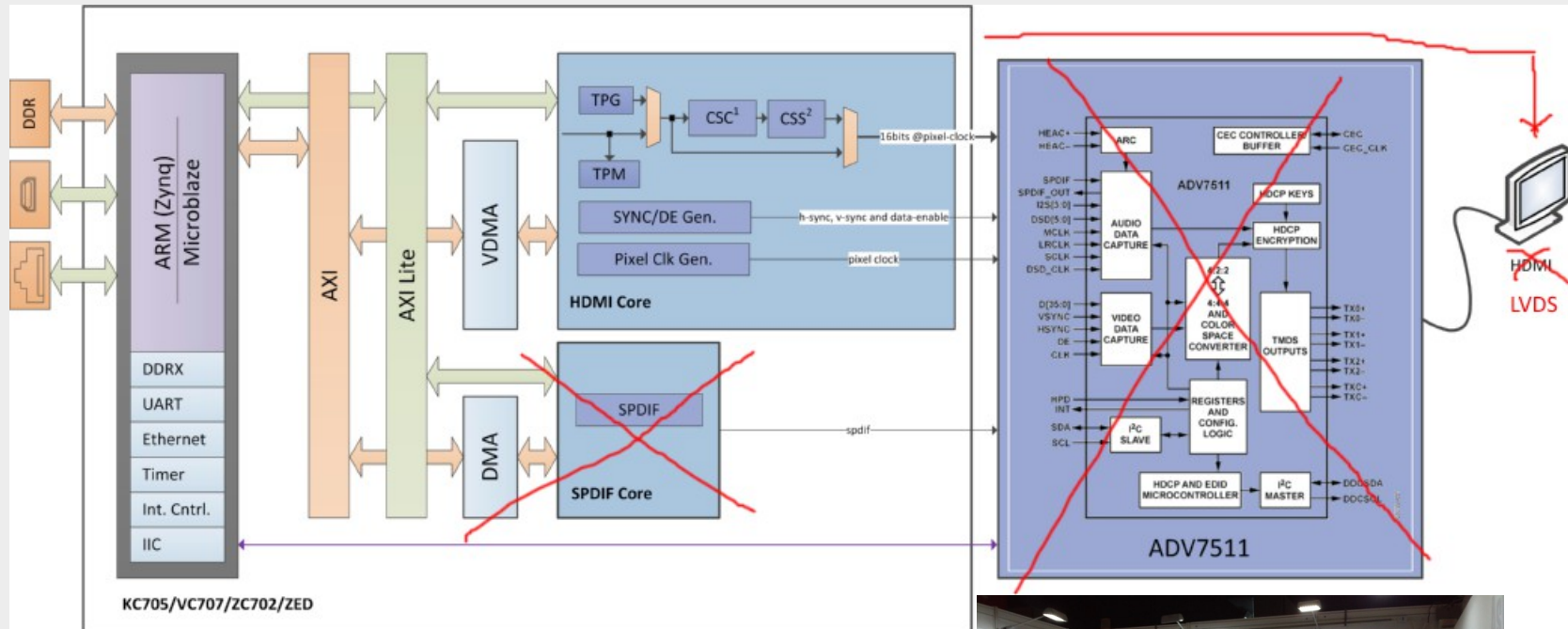
- <http://www.xilinx.com/products/design-tools/software-zone/sdaccel/supervessel.html>
- <http://www.xilinx.com/about/customer-innovation/data-centers-storage-hpc/cloud-computing.html>



- applicabili sia ai corsi triennali (tirocini) sia alle lauree magistrali
- l'argomento trattato viene modulato in maniera opportuna, in accordo con lo studente, affinché il contenuto sia congruo con il percorso accademico del laureando
- possibilità da parte del laureando e del relatore di proporre delle variazioni
- previsto un periodo di presenza fisica presso i laboratori dell'azienda ma possibilità di svolgere parte del lavoro in remoto (vedi <http://www.xilinx.com/support/university.html>)
- premio di laurea o rimborso spese per studenti non residenti nelle vicinanze della nostra sede
- efficace anche come strumento di **preselezione del personale** (ad Aprile 2015 oltre il 60% delle risorse del reparto di ricerca e sviluppo di DAVE Embedded Systems è composto da personale che è stato inserito nell'organico immediatamente dopo aver svolto la tesi sperimentale)

- l'ingegneria dei sistemi embedded abbraccia numerose discipline e di conseguenza le tesi proposte hanno un carattere fortemente interdisciplinare
 - progettazione hardware (prevalentemente digitale ma anche analogica)
 - signal integrity
 - compatibilità elettromagnetica
 - sviluppo firmware e device drivers
 - sviluppo software di alto livello
 - sviluppo su FPGA
 - sviluppo su DSP
 - sistemi operativi e RTOS (real-time operating system)

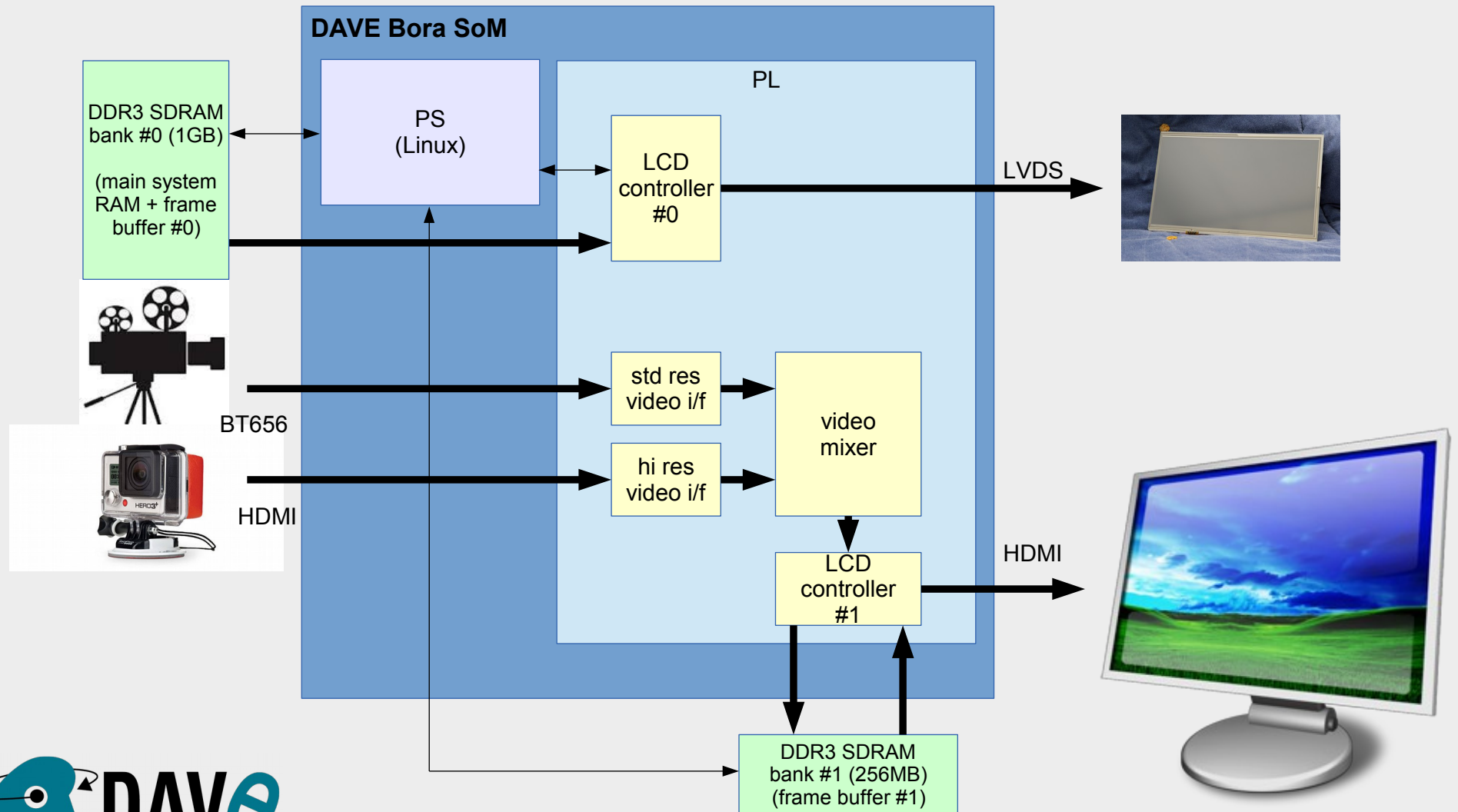
Integrazione in Zynq di un controller grafico con uscita LVDS

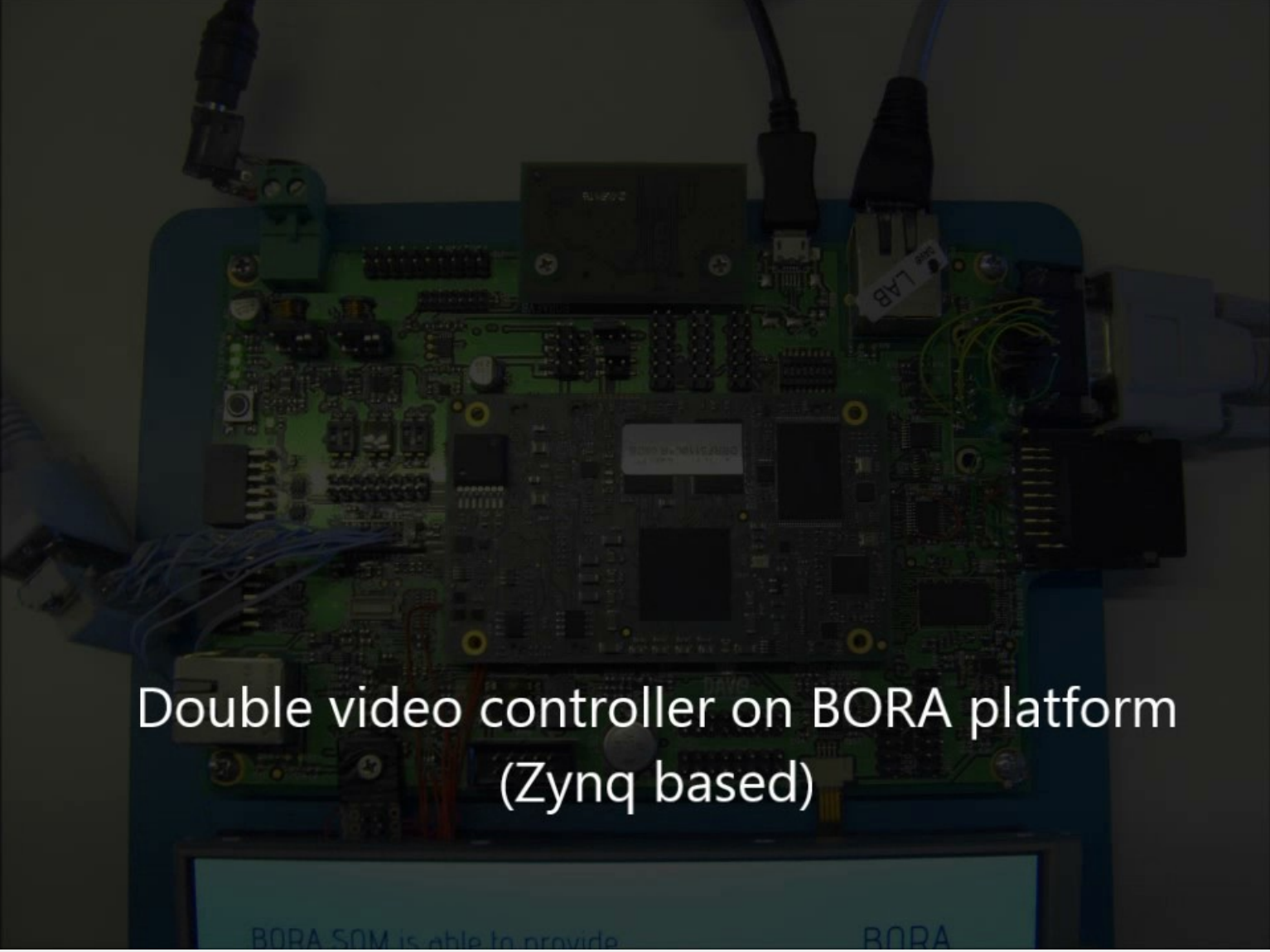


1. RGB to YCbCr Color space conversion (not applicable to VC707).
2. 444 to 422 Subsampling (not applicable to VC707).



Sviluppo di un controller video con doppia uscita indipendente (LVDS + HDMI)

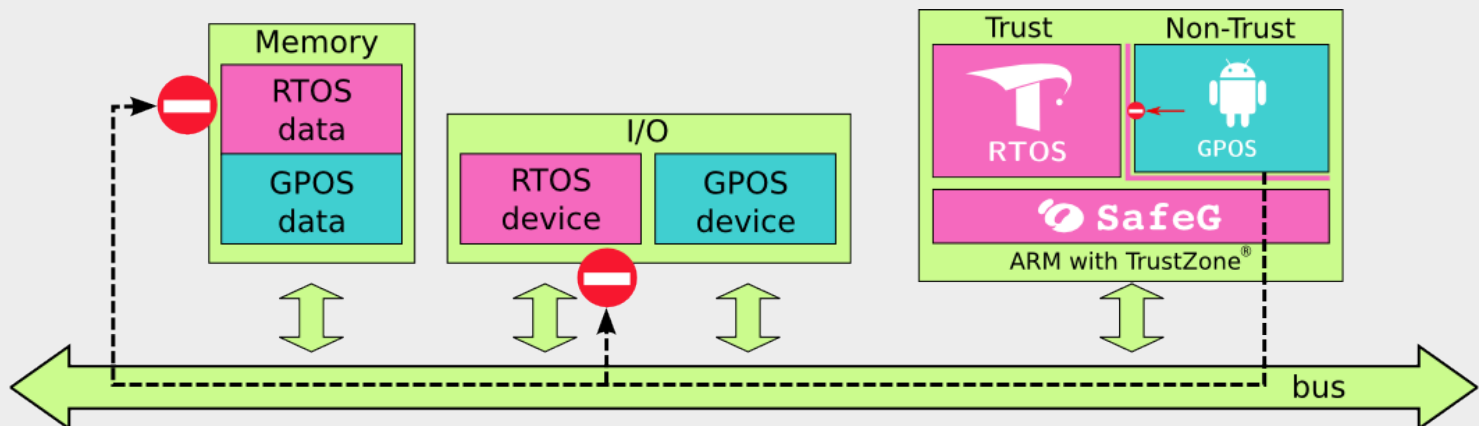
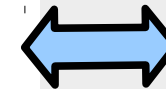
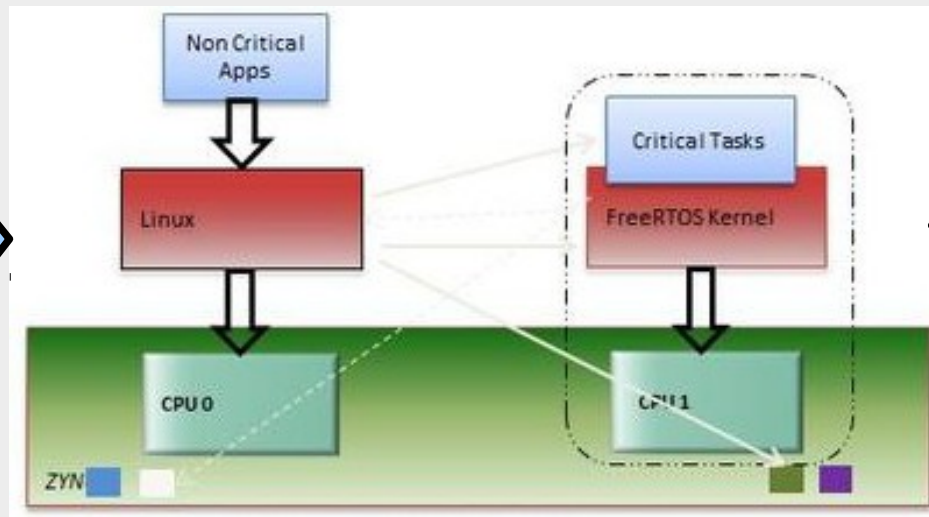
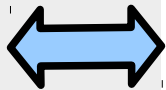




Double video controller on BORA platform
(Zynq based)

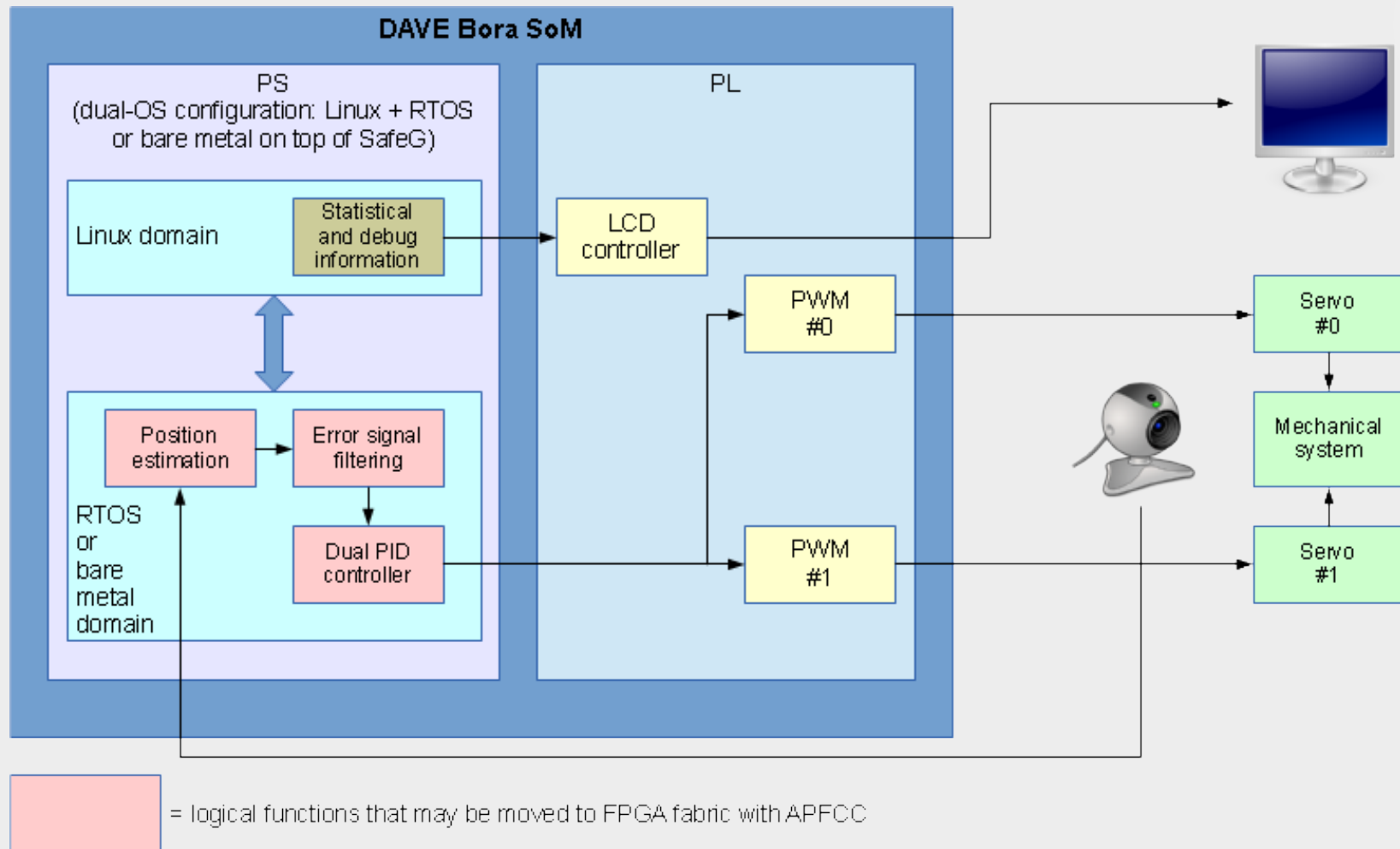
Porting del monitor SafeG su processore multicore NXP/Freescale iMX6 (1/2)

- www.toppers.jp/en/safeg.html
- Asymmetric multi-processing (Linux + RTOS)
- TrustZone





Renesas R-Car E1 Cortex-A9 533Mhz

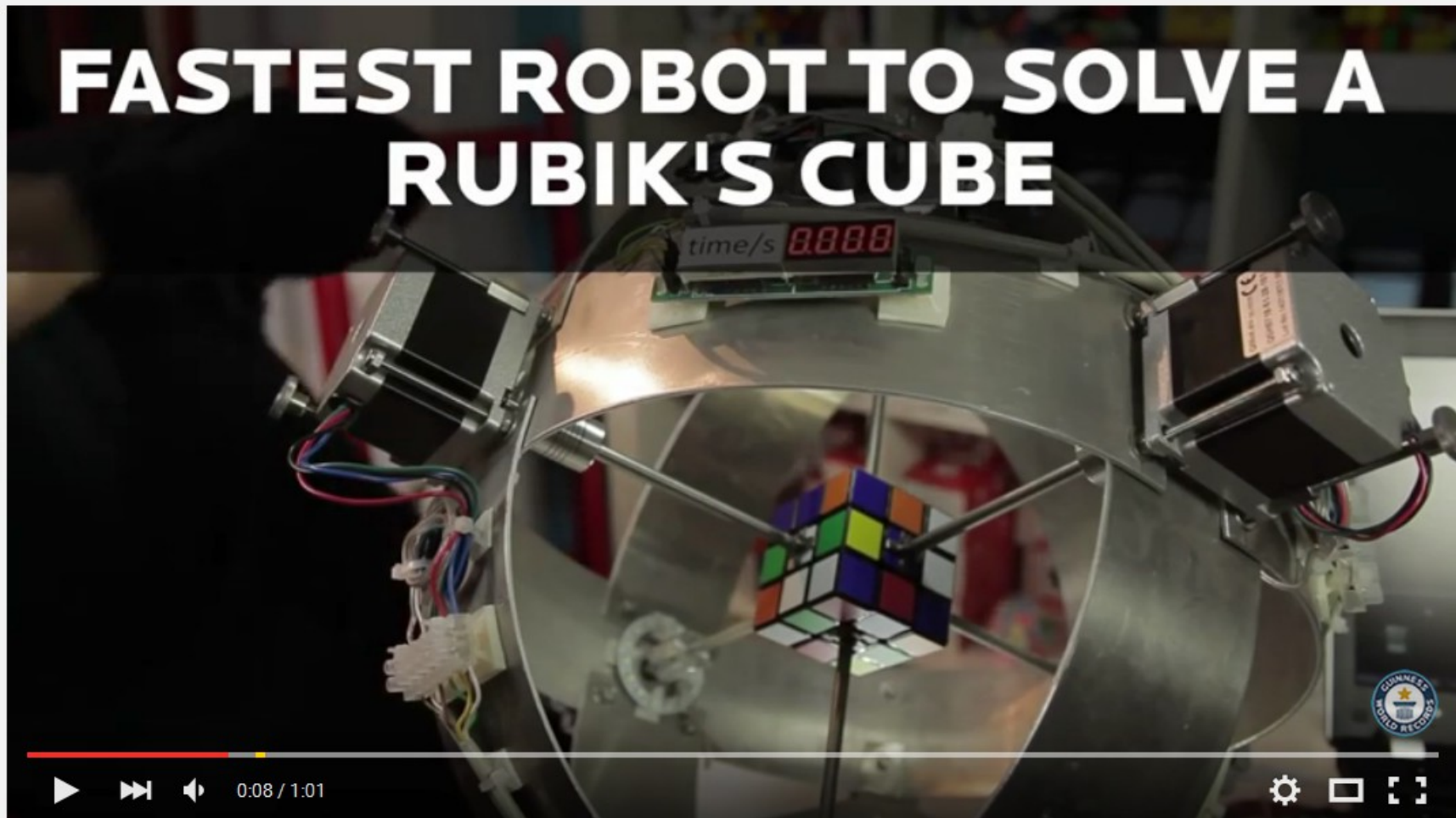


The internship aims at implementing on BORA platform (Zynq based) a real-time detection and control system. This system is used to keep the balance of a mechanical system by acting on two servo motors. Servos are driven by independent PID controllers via PWM IPs implemented in FPGA. PID controller are fed by a signal error generated by image processing algorithms applied to a video stream. Video stream is generated by a camera shooting the mechanical system itself.

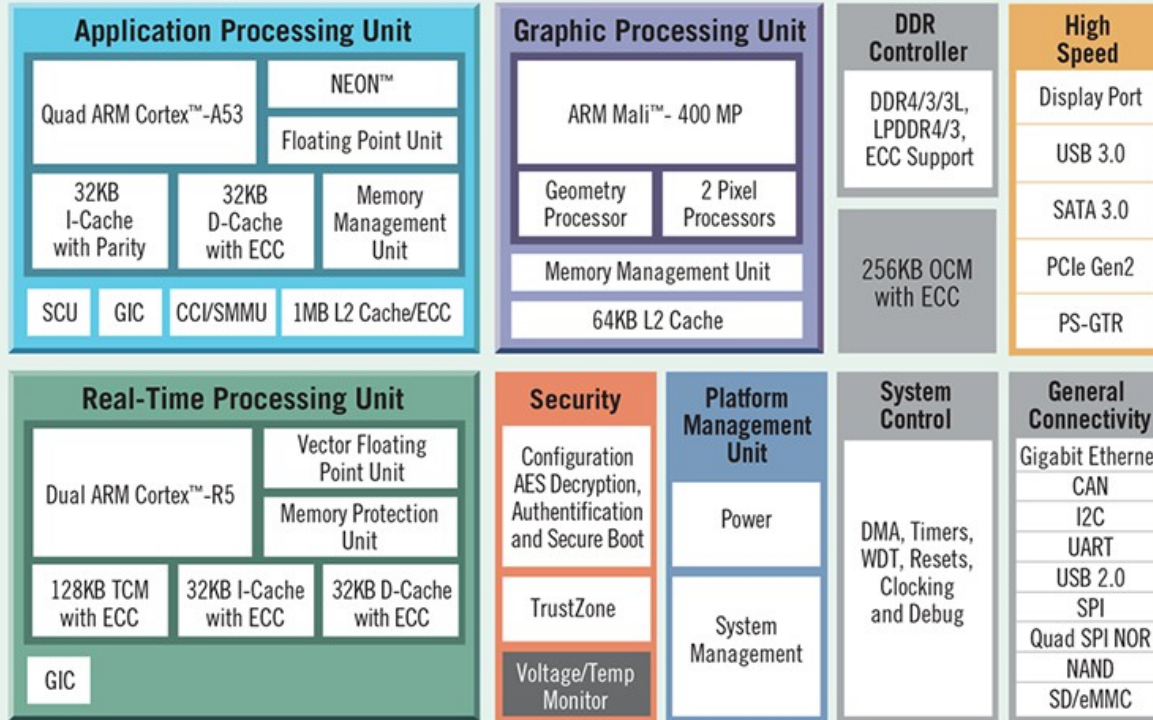
Time consuming portions of software are hardware accelerated, meaning that they are implemented in FPGA via high level languages such as C and C++.

Ball and Plate Control System

Costruire un robot basato su Zynq in grado di battere il record mondiale della risoluzione del cubo di Rubik



Processing System



Programmable Logic

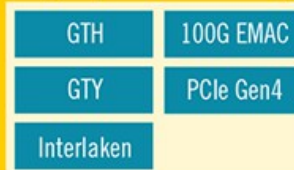
Storage and Signal Processing



General Purpose IO



High Speed Connectivity



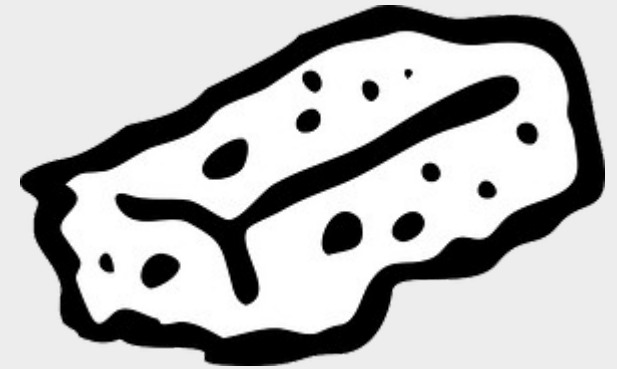
Video Codec



Note: Illustration not drawn to scale.

Detto in maniera meno altisonante:

- avere 20 anni capita una volta nella vita
- siate curiosi e assorbite più che potete!
- non aspettatevi nulla per diritto acquisito!



**Trieste Mini
Maker Faire®**



FABLAB
UDINE



CV di un vostro “concorrente” indiano:

- 26 anni
- Bachelor of Engineering Electronics and Communication Engineering
- C, C++, Assembly, Java, RCP, Android, Shell, Batch scripting
- German (basic), English (fluent), French (intermediate)
- Master of Science: Control and Embedded Instrumentation, ESIGELEC, Rouen (France)
- Master of Science: Embedded System and Instrumentation, Manipal University, Manipal (India)
- Internship at Texas Instruments GmbH, Munich (Germany)
- Internship at Texas Instruments GmbH, Nice (France)





stages@dave.eu



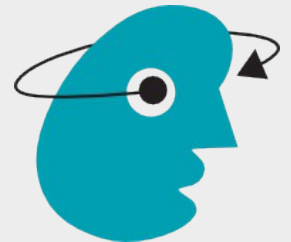
DAVE Embedded Systems



@DAVE_Embedded

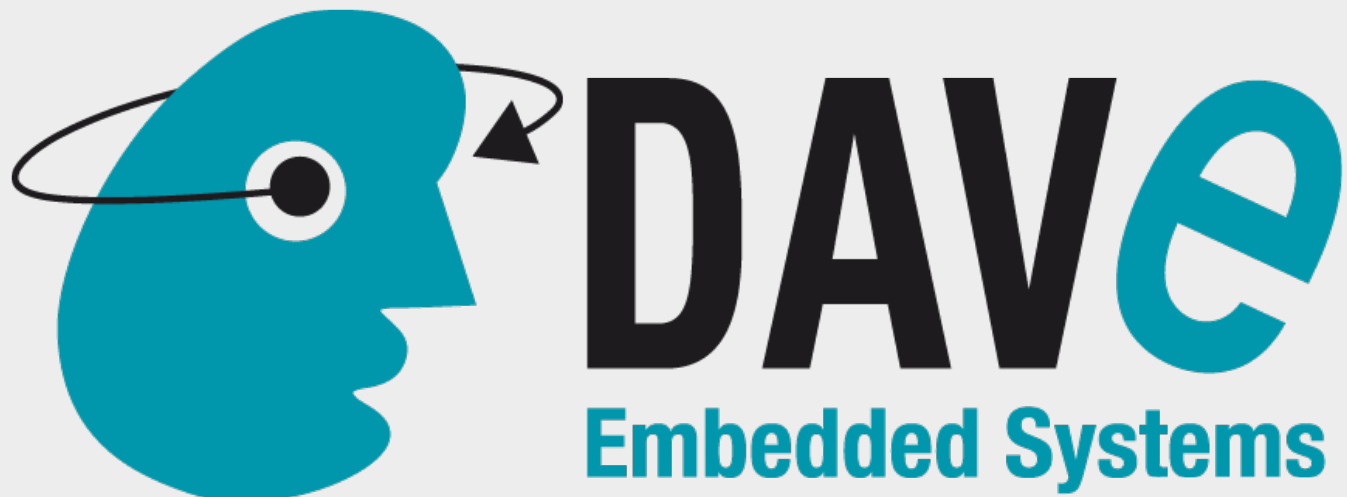


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