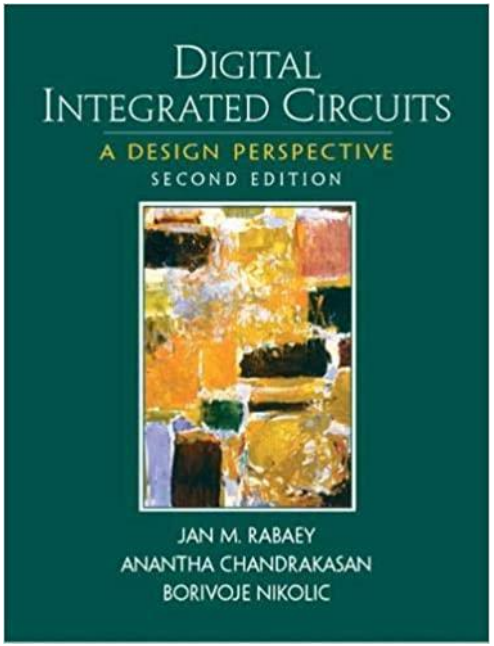
UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

Course Presentation

A.Carini – Digital Integrated Circuits

Books

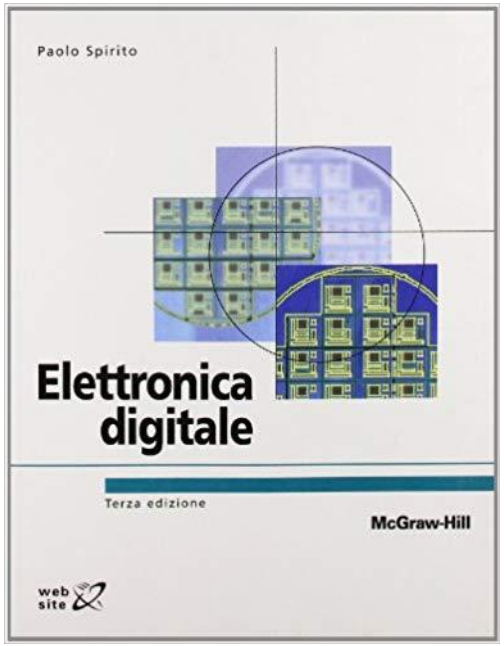


J. M. Rabaey, A. Chandrakasan, B. Nikolic
Digital Integrated Circuits: A Design Perspective
Pearson, 2003

Biblioteca scientifica:

Inventario	H0A 9614
Collocazione	21b / 0028

Books



Paolo Spirito
Elettronica Digitale
McGraw-Hill, 2006

Biblioteca scientifica:

Inventario	H0A 17736
Collocazione	21b / 0045

The course program

1. Introduction

Digital electronics field; Cost of an integrated circuit; Functionality and Robustness; The Voltage Transfer Characteristic; Nominal voltage levels; Low and high limit voltages; Noise Margins; Regenerative Property; Directivity; Fan In and Fan Out; Ideal digital gate; Propagation delay; Rise and fall times; Power and Energy Consumption

2. The MOS(FET) Transistor

The MOS Transistor under Static Conditions; Resistive Operation; The Saturation Region; Velocity Saturation; Drain Current versus Voltage Charts; Subthreshold Conduction; A unified MOS model for manual analysis; An even more simplified model; Equivalent resistance when (dis)charging a capacitor; Dynamic Behavior; MOS Structure Capacitances; Channel Capacitance; Junction Capacitances

3. The Wire

A first glance; Electrical Wire Models; The Ideal Wire; The Lumped Model; The Lumped RC model; Elmore delay formula; The Distributed rc Line; The Transmission Line: The Lossless Transmission Line and The Lossy Transmission Line

The course program

4. The CMOS inverter

The CMOS Inverter; The voltage transfer characteristic; Qualitative analysis of the transient behavior; The Static Behavior: Switching Threshold, Noise Margins; Device Variations; Scaling the Supply Voltage; The Dynamic Behavior; Capacitances; Propagation Delay: First Order Analysis; Sizing Inverters for Performance; Sizing a Chain of Inverters; Delay in the Presence of (Long) Interconnect Wires; Dynamic Power Consumption; Low Energy/Power Design Techniques; Dissipation Due to Direct Path Currents; Static Consumption; The total power consumption; Power delay product; Energy-Delay Product

5. Combinational logic gates in CMOS

Static CMOS Design; Static Properties of Complementary CMOS Gates; Propagation Delay of Complementary CMOS Gates; Design Techniques for Large Fan-in; Ratioed Logic or Pseudo-NMOS Logic; Differential Cascode Voltage Switch Logic (or DCVSL)

6. BiCMOS Logic , Wired Logic , Three-state logic

BiCMOS inverter, Wired logic, Three-state logic

7. Combinational circuits

Matrix and Bit-slice structure; Decoders, Encoders, Demultiplexer, Logic element, Programmable logic array (PLA)

The course program

8. CMOS structures for VLSI
   Pass-Transistor; CMOS transmission gate; Phase signal disturbance; Pass-transistor logic; Dynamic logic; Domino logic; NORA CMOS Logic
9. Semiconductor Memories
   Memory Classification: Size, Timing parameters, Function, Access Pattern, Input/Output Architecture; Memory Architecture and Building Blocks; ROMs; Non Volatile Memories; The Dual Gate MOS; Hot Electrons and Thin Oxide Tunneling; EPROM; EEPROM; FLASH memories; SRAM memories; DRAM memories.