UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

Introduction

A.Carini – Digital Integrated Circuits

Digital electronics

Analog signals -> Analog Electronics
Digital signals -> Digital Electronics

- With digital electronics, we refer to the electronic treatment of binary digital signal.
- Binary signals: assume two possible values or states, indicated with 0 1.
- In electronic circuits they are represented with two discrete values of an electric quantity (typically a voltage).
- The two states can also be identified as: high and low, or off and on.

Digital electronics field

- The digital electronic field deals with the study, the understanding, the design of the basic digital electronic circuits that are the building blocks for the implementation of more complex digital systems.
- The digital circuits can be described using the logic function they implement, i.e., the relationship between the input and output logic variables.
- Nevertheless, no digital circuit has an ideal behavior:
  - The input and output values vary in analog way,
  - With delays passing from input to output,
  - With levels different from the ideal ones,
  - With variable power dissipation according to the operative conditions.
- The study and design of these circuits cannot disregard an electric analysis of all the values in play.

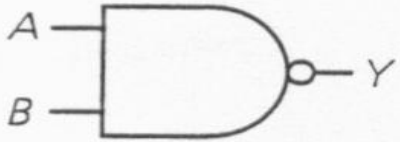
Logic representation

$$Y = \overline{A \cdot B}$$

Relazione booleana

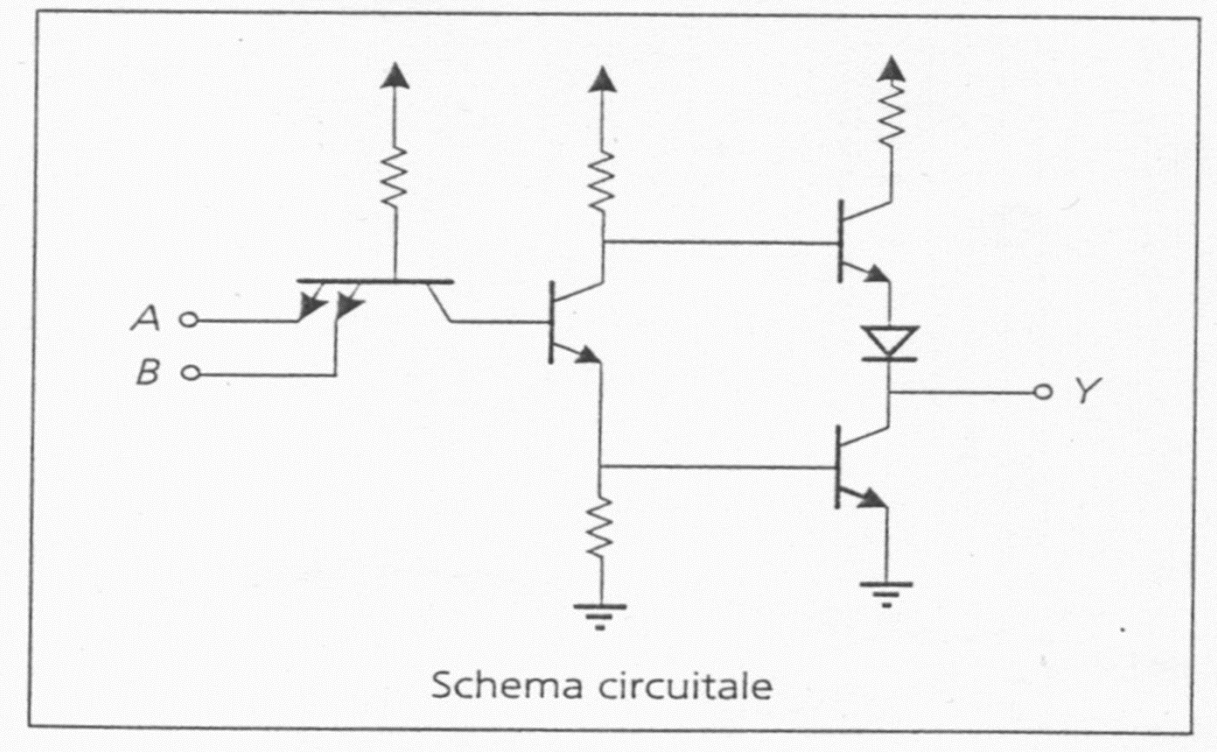
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Tabella della verità

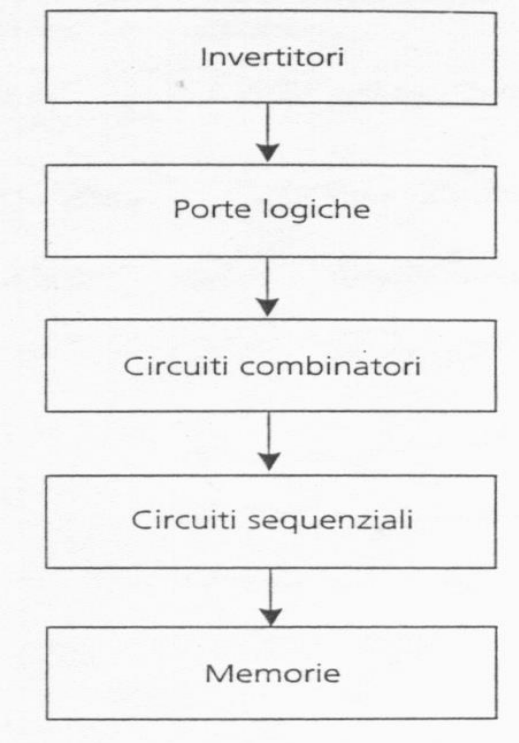


Simbolo logico

Circuit representation



Hieratical classification of digital systems



Cost of an integrated circuit

- The total cost can be separated into two components: fixed and variable costs.
- *Fixed cost* is independent form the production volumes.
  - Effort in time and manpower it takes to produce the design.
  - Influenced by complexity of the design, aggressiveness of the specifications, and productivity of the designer.
  - Includes the indirect costs: R&D, manufacturing equipment, marketing, …
- *Variable cost* depends on the production volumes.
  - accounts for the cost directly attributable to a manufactured product, hence, is proportional to the product volume.
  - include costs of parts used in product, assembly costs, and testing costs.

$$\text{cost per IC} = \text{variable cost per IC} + \left(\frac{\text{fixed cost}}{\text{volume}}\right)$$

Cost of an integrated circuit

$$\text{cost per IC} = \text{variable cost per IC} + \left(\frac{\text{fixed cost}}{\text{volume}}\right)$$

$$\text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}$$

- The die cost depends upon the number of dies on a wafer, and the percentage of those that are functional, *die yield*.

$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}$$

- The number of dies per wafer is the area of the wafer divided by the die area.
- The cost of a circuit is dependent upon the chip area.

Cost of an integrated circuit

- The actual relation between cost and area depends upon the die yield.
- Both the substrate material and the manufacturing process introduce faults that can cause a chip to fail.
- Assuming that the defects are randomly distributed over the wafer, and that the yield is inversely proportional to the complexity of the fabrication process:

$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

- α is a parameter that depends upon the complexity of the manufacturing process, and is roughly proportional to the number of masks ($\alpha \approx 3$)
- The defects per unit area $\approx$ 0.5 and 1 defects/cm^2

Cost of an integrated circuit

- It results that die costs are proportional to the fourth power of the area

$$\text{cost of die} = f(\text{die area})^4$$

- The area is a function that is directly controllable by the designer(s) and is the prime metric for cost.
- Small area is hence a desirable property for a digital gate.
- The smaller the gate, the higher the integration density and the smaller the die size.
- Smaller gates furthermore tend to be faster and consume less energy, as the total gate capacitance often scales with the area.

Functionality and Robustness

- The measured behavior of a manufactured circuit normally deviates from the expected response.
- One reason for this aberration are the variations in the manufacturing process.
- Another source of deviation is due to the presence of disturbing noise sources on or off the chip.
- The word noise in the context of digital circuits means *“unwanted variations of voltages and currents at the logic nodes.”*

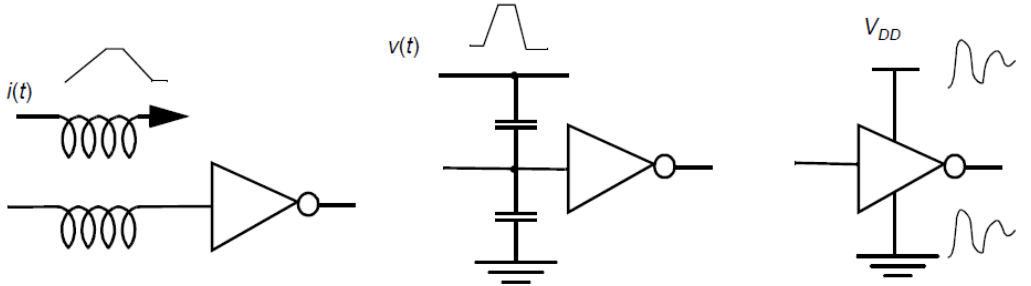


Figure 1.10 Noise sources in digital circuits.

Functionality and Robustness

- Most noise in a digital system is internally generated, and the noise value is proportional to the signal swing.
  - Noise sources that are a function of the signal level are better expressed as a fraction or percentage of the signal level.
- Other noise sources such as input power supply noise are external to the system, and their value is not related to the signal levels.
  - For these sources, the noise level is directly expressed in Volt or Ampere.
- The steady-state parameters (also called the *static behavior*) of a gate measure how robust the circuit is with respect to both variations in the manufacturing process and noise disturbances.

Nominal voltage levels

- The logic variables are represented by electrical quantities.
- This is most often a node voltage that is not discrete but can adopt a continuous range of values.
- This electrical voltage is turned into a discrete variable by associating *a nominal voltage level* with each logic state:

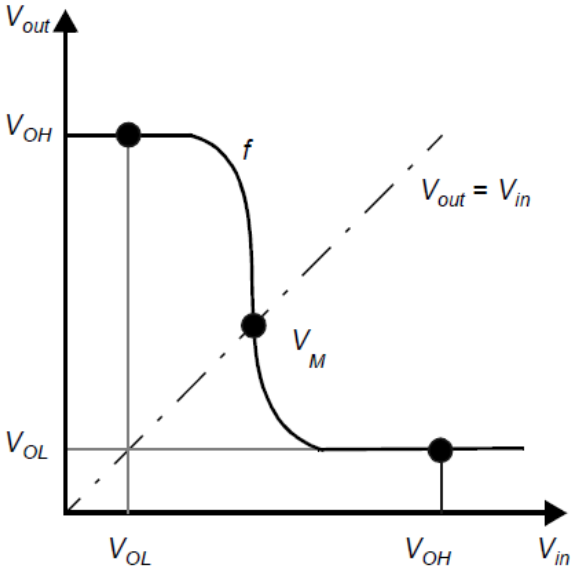
$$1 \Leftrightarrow V_{OH}, 0 \Leftrightarrow V_{OL},$$

- V_{OH} and V_{OL} represent the *high* and *low* logic levels, respectively.

- The difference between the two, V_{OH}-V_{OL}, is the *logic* or *signal swing* $V_{sw.}$

The Voltage-Transfer Characteristic

- The electrical function of a gate is best expressed by its *voltage-transfer characteristic* (VTC) (sometimes called the *DC transfer characteristic*), which plots the output voltage as a function of the input voltage $V_{out} = f(V_{in})$.



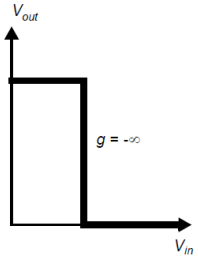
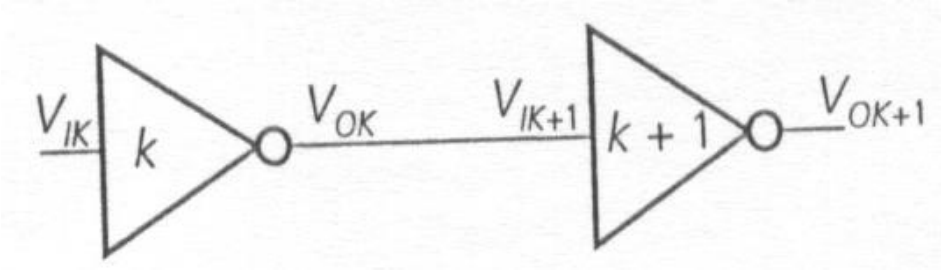


Figure 1.17 Ideal voltage-transfer characteristic.

Figure 1.11 Inverter voltage-transfer characteristic.

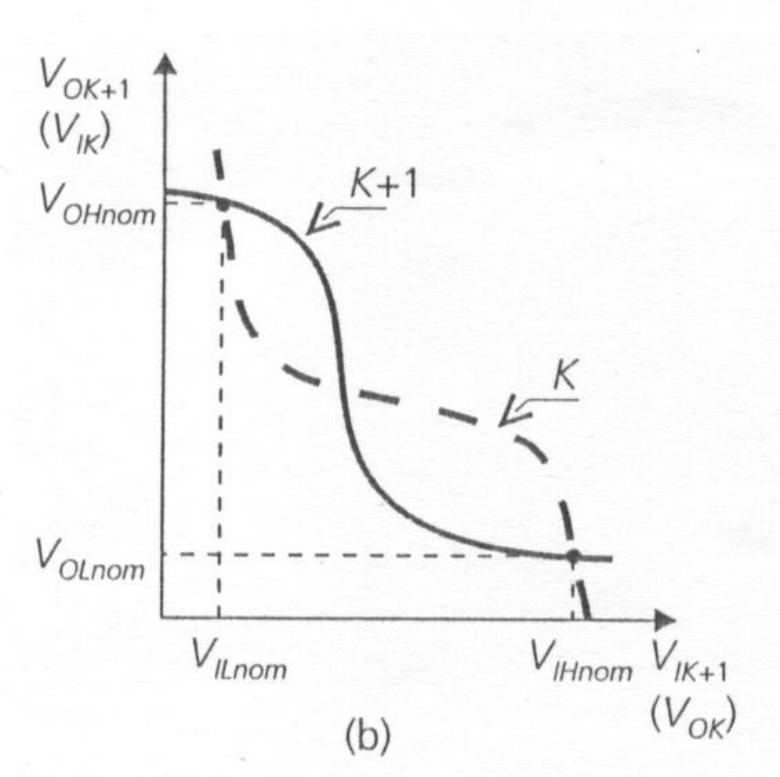
Nominal voltage level definition

- Considering the cascade of two inverters, we would like the output of the second inverter to be equal to the input of the first one.

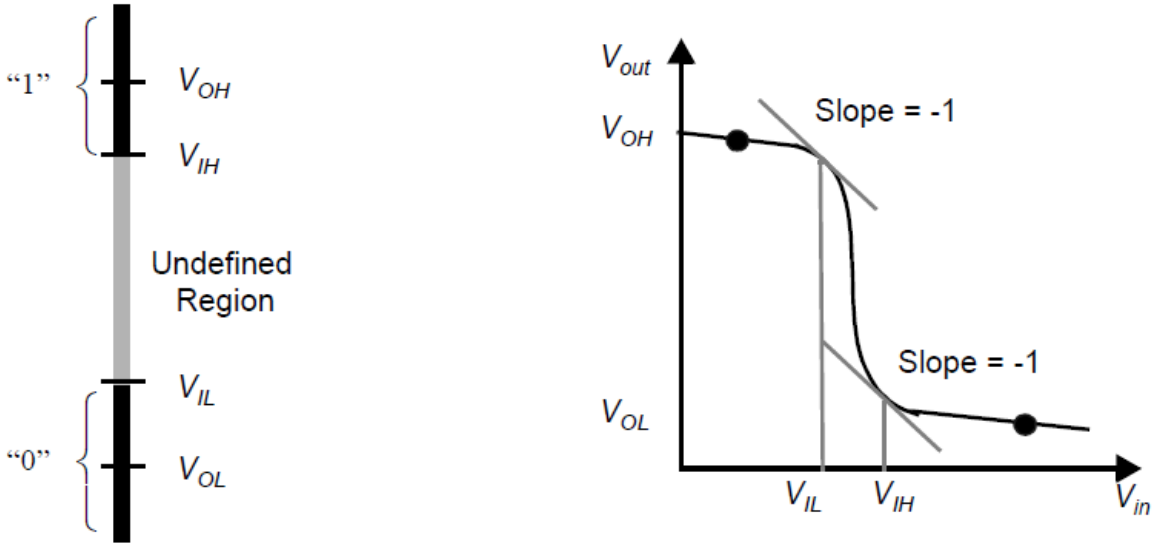


- We would like $V_{O,K+1}=V_{I,K}$
- Take the VTC and rotate it around the 45° axis.
- There are three intersections that guarantee $V_{O,K+1}=V_{I,K}$.
- The external ones define the *low and high nominal voltages.*
- The middle one defines the *gate or switching threshold voltage* V_M.

Nominal voltage level definition



Low and high limit voltage



(a) Relationship between voltage and logic levels

(b) Definition of V_{IH} and V_{IL}

Figure 1.12 Mapping logic levels to the voltage domain.

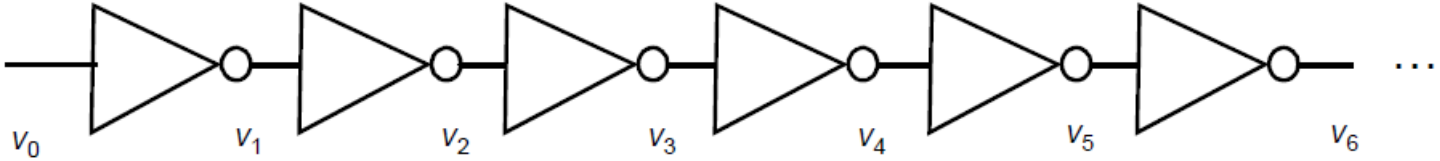
Low and high limit voltage & noise margins

- The regions of acceptable high and low voltages are delimited by $\boldsymbol{V}_{IH}$ and $\boldsymbol{V}_{IL}$. These represent by definition the points where the gain (= dV_{out} / dV_{in}) of the VTC equals -1.
- The region between V_{IH} and V_{IL} is called the *undefined region.*
- The noise margins NM_L (*n. m. low*) and NM_H (*n. m. high*) quantize the size of the legal "0" and "1", respectively, and set a fixed maximum threshold on the noise value:

$$NM_L = V_{IL} - V_{OL}$$
$$NM_H = V_{OH} - V_{IH}$$

- It is obvious that the margins should be larger than 0 for a digital circuit to be functional and by preference should be as large as possible.

Regenerative Property



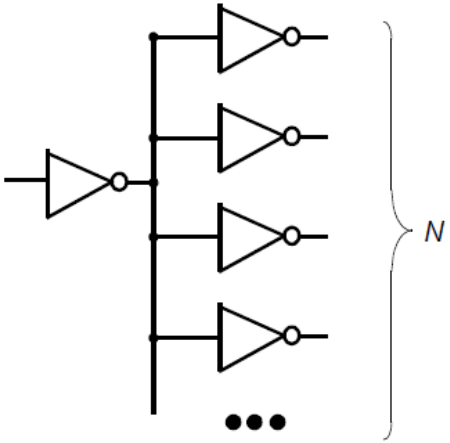
- An input voltage v_{in} ($v_{in} \in$ "0") is applied to a chain of *N* inverters.
- Assuming that the number of inverters in the chain is even, the output voltage v_{out} ($N \rightarrow \infty$) will equal V_{OL} if and only if the inverter possesses the *regenerative property*. Similarly, when an input voltage v_{in} ($v_{in} \in$ "1") is applied to the inverter chain, the output voltage will approach the nominal value V_{OH}.
- To be regenerative, the VTC should have a transient region (or undefined region) with a gain *greater than* 1 in absolute value, bordered by the two legal zones, where the gain should be *smaller than* 1.

Directivity

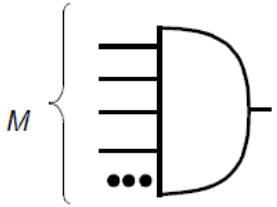
- The directivity property requires a gate to be *unidirectional*, that is, changes in an output level should not produce any change on the input of the circuit.
- In real gate implementations, full directivity can never be achieved.
- Some feedback of changes in output levels to the inputs cannot be avoided.
- Capacitive coupling between inputs and outputs is a typical example of such a feedback.
- It is important to minimize these changes so that they do not affect the logic levels of the input signals.

Fan-In and Fan-Out

- The *fan-out* denotes *the number of load gates N that are connected to the output of the driving gate.*
- The *fan-in* of a gate is defined as the *number of inputs* to the gate.



(a) Fan-out *N*



(b) Fan-in *M*

Figure 1.16 Definition of fan-out and fan-in of a digital gate.

Ideal digital gate

- Has infinite gain in the transition region, and gate threshold located in the middle of the logic swing, with high and low noise margins equal to half the swing.
- The input and output impedances of the ideal gate are infinity and zero, respectively.

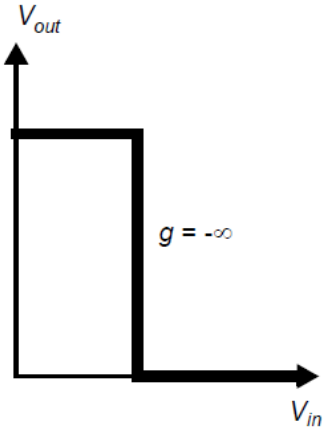


Figure 1.17 Ideal voltage-transfer characteristic.

Performance

- When focusing on the pure design of complex digital systems, performance is most often expressed by the duration of the clock period (*clock cycle time)*, or its rate (*clock frequency*).
- The minimum value of the clock is set by a number of factors such as
  - the time it takes for the signals to propagate through the logic,
  - the time it takes to get the data in and out of the registers,
  - and the uncertainty of the clock arrival times.

Propagation delay

- The *propagation delay* t_p of a gate defines how quickly it responds to a change at its input(s).
- It expresses *the delay experienced by a signal when passing through a gate*.
- It is measured between the 50% transition points of the input and output waveforms.
- The t_{pLH} defines the response time of the gate for a *low to high* (or positive) output transition, while t_{pHL} refers to a *high to low* (or negative) transition.
- The propagation delay t_p is defined as the average of the two.

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$

Propagation delay

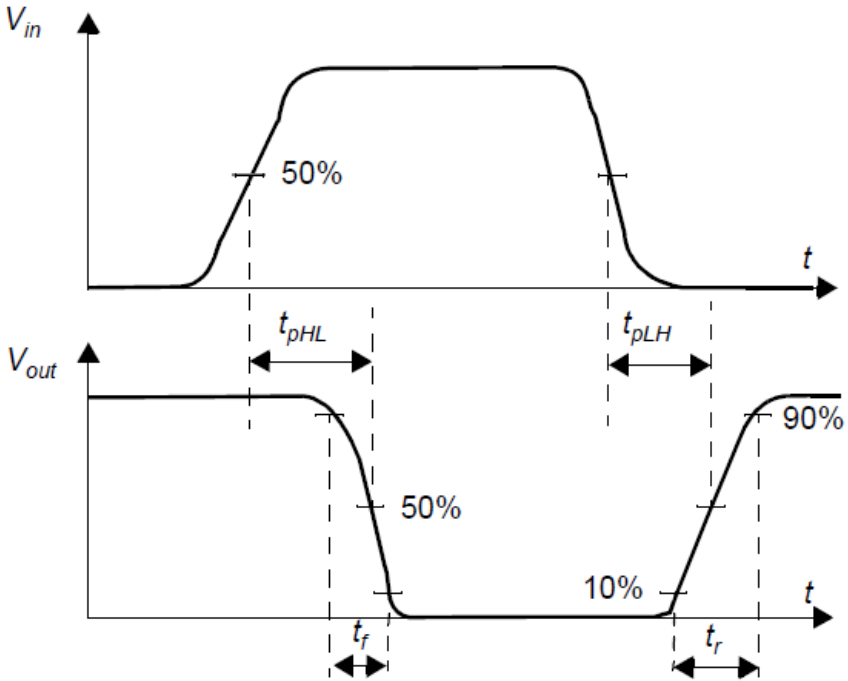
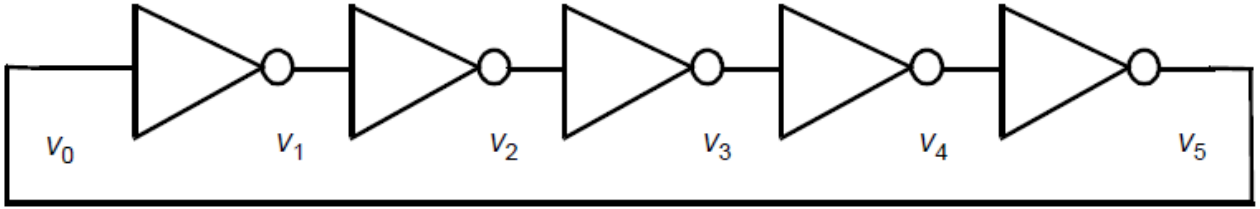


Figure 1.19 Definition of propagation delays and rise and fall times.

Rise and fall times

- The *rise and fall times* t_r and t_f are metrics that apply to individual signal waveforms rather than gates.
- They express how fast a signal transits between the different levels and are defined as the time between the 10% and 90% points of the waveforms.
- The rise/fall time of a signal is largely determined by the strength of the driving gate, and the load presented by the node itself.

Circuit for delay measurement



- The de-facto standard circuit for delay measurement is the *ring oscillator*, which consists of an odd number of inverters connected in a circular chain.
- Due to the odd number of inversions, this circuit does not have a stable operating point and oscillates.
- The period *T* of the oscillation is determined by the propagation time of a signal transition through the complete chain

$$T = 2 \times t_p \times N$$

Propagation Delay of First-Order *RC* Network

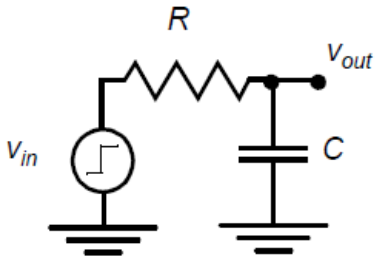


Figure 1.21 First-order *RC* network.

- When applying a step input: $v_{out}(t) = (1 - e^{-t/\tau})\ V$ $\tau = RC$.

- The time to reach the 50% point is easily computed as $t = \ln(2)\tau = 0.69\ \tau$.
- Similarly, the rise time to pass from 10% till 90% is $t = \ln(9)\ \tau = 2.2\ \tau$.

Power and Energy Consumption

- The power consumption of a design determines how much energy is consumed per operation, and how much heat the circuit dissipates.
- These factors influence a great number of critical design decisions, such as the power-supply capacity, the battery lifetime, supply-line sizing, packaging and cooling requirements.
- Therefore, power dissipation is an important property of a design that affects feasibility, cost, and reliability.
- Power consumption limits, dictated by the chip package and the heat removal system, determine the number of circuits that can be integrated onto a single chip, and how fast they are allowed to switch.

Power and Energy Consumption

- The **peak power** P_{peak} is important when studying supply-line sizing.
- When addressing cooling or battery requirements, one is predominantly interested in the **average power** dissipation P_{av}.

$$P_{peak} = i_{peak} V_{supply} = max[p(t)]$$

$$P_{av} = \frac{1}{T}\int_0^T p(t)dt = \frac{V_{supply}}{T}\int_0^T i_{supply}(t)dt$$

- where $p(t)$ is the instantaneous power, i_{supply} is the current being drawn from the supply voltage V_{supply} over the interval $t \in [0,T]$, and i_{peak} is the maximum value of i_{supply} over that interval.

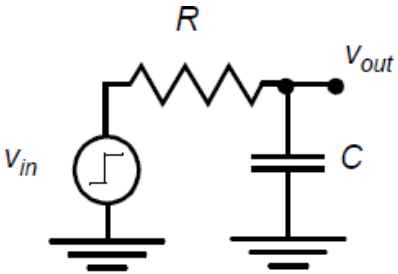
Power and Energy Consumption

- The dissipation can further be decomposed into *static* and *dynamic* components.
- The **dynamic component** occurs only during transients, when the gate is switching. It is attributed to the charging of capacitors and temporary current paths between the supply rails, and is, therefore, proportional to the switching frequency: *the higher the number of switching events, the higher the dynamic power consumption.*
- The **static component** is present even when no switching occurs and is caused by static conductive paths between the supply rails or by leakage currents.
- The propagation delay and the power consumption of a gate are related.
- For a given technology and gate topology, the product of power consumption and propagation delay (the ***power-delay product*** - PDP) is generally a constant.
- The PDP is simply the *energy* consumed by the gate *per switching event*.

Energy Dissipation of First-Order RC Network

- When applying a step input (with V_{in} going from 0 to V), an amount of energy is provided by the signal source to the network.
- The total energy delivered by the source is

$$E_{in} = \int_0^\infty i_{in}(t)v_{in}(t)dt = V\int_0^\infty C\frac{dv_{out}}{dt}dt = (CV)\int_0^V dv_{out} = CV^2$$



- We can also compute how much of the delivered energy gets stored on the capacitor at the end of the transition:

$$E_C = \int_0^\infty i_C(t)v_{out}(t)dt = \int_0^\infty C\frac{dv_{out}}{dt}v_{out}dt = C\int_0^V v_{out}dv_{out} = \frac{CV^2}{2}$$

See:

- J. M. Rabaey, A. Chandrakasan, B. Nikolic, «Digital Integrated Circuits: A Design Perspective», Pearson, 2003
  - Cap. 1.3