UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

The Wire

A.Carini – Digital Integrated Circuits

Introduction

- The parasitics effects introduced by the wires display a scaling behavior that differs from the active devices such as transistors, and tend to gain in importance as device dimensions are reduced and circuit speed is increased.
- In fact, they start to dominate some of the relevant metrics of digital integrated circuits such as speed, energy-consumption, and reliability.
- This situation is aggravated by the fact that improvements in technology make the production of ever-larger die sizes economically feasible, which results in an increase in the average length of an interconnect wire and in the associated parasitic effects.

A First Glance

- State-of-the-art processes offer multiple layers of Aluminum, and at least one layer of polysilicon.
- Even the heavily doped n+ or p+ layers, typically used for the realization of source and drain regions, can be employed for wiring purposes.
- The wiring of today's integrated circuits forms a complex geometry that introduces capacitive, resistive, and inductive parasitics.
- All three have multiple effects on the circuit behavior:
  1. An increase in propagation delay, or, equivalently, a drop in performance.
  2. An impact on the energy dissipation and the power distribution.
  3. An introduction of extra noise sources, which affects the reliability of the circuit.

A First Glance

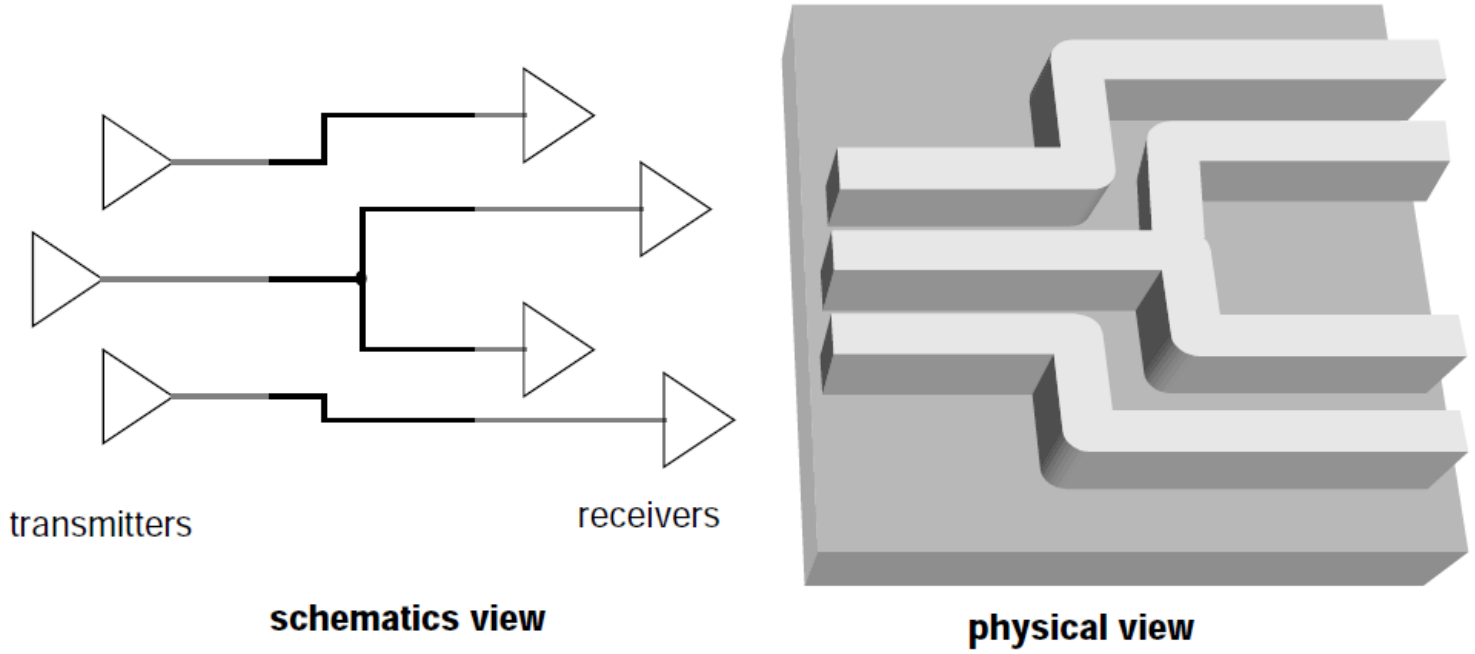


Figure 4.1 Schematic and physical views of wiring of bus-network. The latter shows only a limited area (as indicated by the shadings in the schematics).

A First Glance

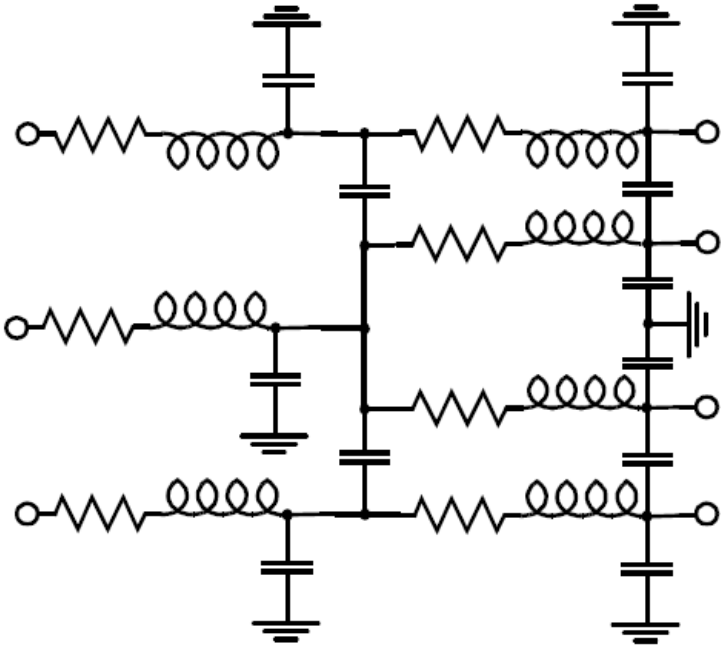
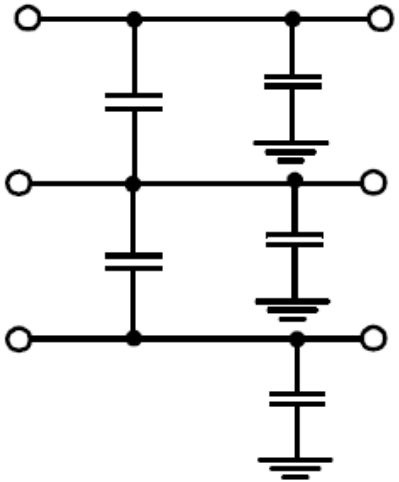


Figure 4.2 Wire models for the circuit of Figure 4.1. Model (a) considers most of the wire parasitics (with the exception of inter-wire resistance and mutual inductance), while model (b) only considers capacitance.

A First Glance

- Analyzing the behavior of this schematic, which only models a small part of the circuit, is slow and cumbersome.
- Fortunately, substantial simplifications can often be made:
  - Inductive effects can be ignored if the resistance of the wire is substantial — this is for instance the case for long Aluminum wires with a small cross-section — or if the rise and fall times of the applied signals are slow.
  - When the wires are short, the cross-section of the wire is large, or the interconnect material used has a low resistivity, a capacitance-only model can be used (see next figure).
  - Finally, when the separation between neighboring wires is large, or when the wires only run together for a short distance, inter-wire capacitance can be ignored, and all the parasitic capacitance can be modeled as capacitance to ground.

A First Glance



(b)

Figure 4.2 Wire models for the circuit of Figure 4.1. Model (a) considers most of the wire parasitics (with the exception of inter-wire resistance and mutual inductance), while model (b) only considers capacitance.

Electrical Wire Models

- These parasitic elements have an impact on the electrical behavior of the circuit and influence its delay, power dissipation, and reliability.
- To study these effects requires the introduction of electrical models that estimate and approximate the real behavior of the wire as a function of its parameters.
- These models vary from very simple to very complex depending upon the effects that are being studied and the required accuracy.

The Ideal Wire

- In schematics, wires occur as simple lines with no attached parameters or parasitics.
- These wires have no impact on the electrical behavior of the circuit.
- A voltage change at one end of the wire propagates immediately to its other ends, even if those are some distance away.
- Hence, it may be assumed that the same voltage is present at every segment of the wire at the every point in time, and that the whole wire is an *equipotential region*.
- While this *ideal-wire model* is simplistic, it has its value, especially in the early phases of the design process, or when studying small circuit components such as gates and the wires tend to be very short and their parasitics ignorable.

The Lumped Model

- The circuit parasitics of a wire are distributed along its length and are not lumped into a single position.
- Yet, when only a single parasitic component is dominant, when the interaction between the components is small, or when looking at only one aspect of the circuit behavior, it is often useful to lump the different fractions into a single circuit element.
- As long as the resistive component of the wire is small and the switching frequencies are in the low to medium range, it is meaningful to consider only the capacitive component of the wire, and to lump the distributed capacitance into a single capacitor.

The Lumped Model

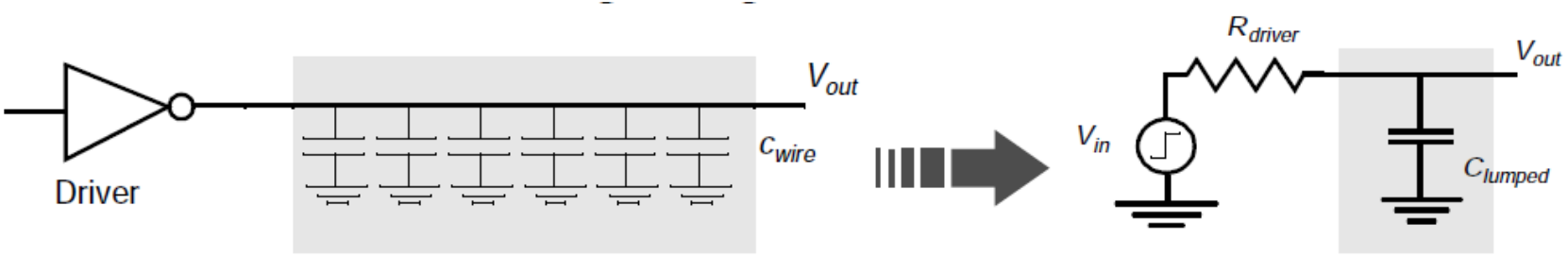
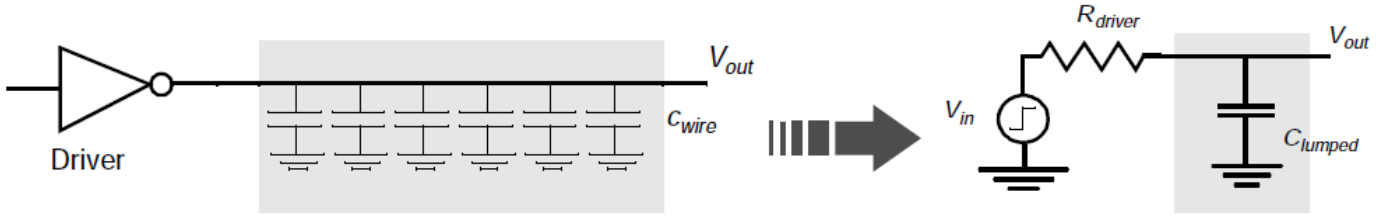


Figure 4.11 Distributed versus lumped capacitance model of wire. $C_{lumped} = L \times c_{wire}$, with L the length of the wire and c_{wire} the capacitance per unit length. The driver is modeled as a voltage source and a source resistance R_{driver}.

- In this model the wire still represents an equipotential region, and that the wire itself does not introduce any delay.
- The only impact on performance is introduced by the loading effect of the capacitor on the driving gate.

The Lumped Model



- A driver with a source resistance of 10 kΩ is used to drive a 10 cm long, 1 um wide.
- The total lumped capacitance for this wire equals 11 pF.

$$C_{lumped}\frac{dV_{out}}{dt} + \frac{V_{out} - V_{in}}{R_{driver}} = 0$$

- When applying a step input (with V_{in} going from 0 to V):

$$V_{out}(t) = (1 - e^{-t/\tau})\, V \qquad \tau = R_{driver} \times C_{lumped}$$

$t_{50\%} = \ln(2)\tau = 0.69\tau$
$t_{90\%} = \ln(9)\tau = 2.2\tau$

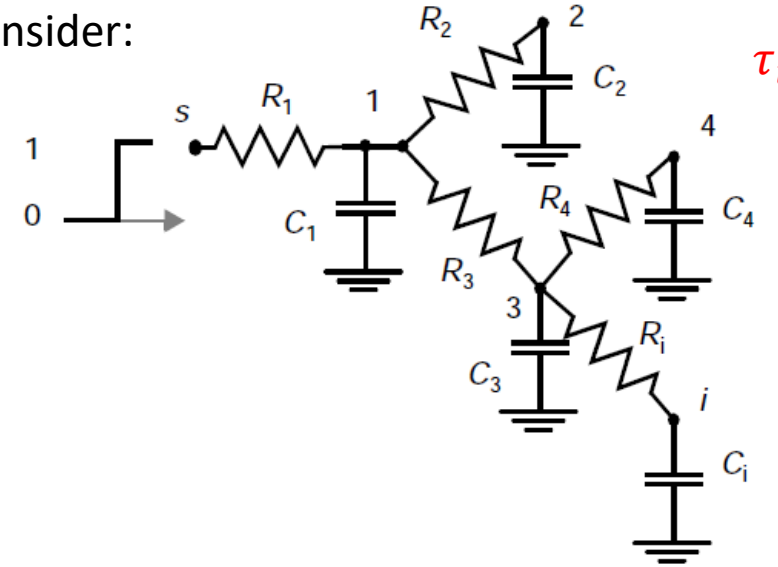
$t_{50\%} = 0.69 \times 10\ \text{K}\Omega \times 11\ \text{pF} = 76\ \text{nsec}$
$t_{90\%} = 2.2 \times 10\ \text{K}\Omega \times 11\ \text{pF} = 242\ \text{nsec}$

The Lumped RC model

- On-chip metal wires of over a few mm length have a significant resistance.
- The equipotential assumption, presented in the lumped-capacitor model, is no longer adequate, and a resistive-capacitive model has to be adopted.
- A first approach lumps the total wire resistance of each wire segment into one single *R* and similarly combines the global capacitance into a single capacitor *C*.
- This simple model, called the *lumped RC model* is pessimistic and inaccurate for long interconnect wires (more adequately represented by a distributed rc-model).
- We will see it for the following reasons:
  - The distributed *rc*-model is complex and no closed form solutions exist.
  - A common practice in the study of the transient behavior of complex transistor-wire networks is to reduce the circuit to an *RC* network.

Elmore delay formula

- Consider:



$$\tau_i = C_1R_1 + C_2R_1 + C_3(R_1 + R_3) + C_4(R_1 + R_3) + C_i(R_1 + R_3 + R_i)$$

Figure 4.12 Tree-structured *RC* network.

- This circuit is called an *RC tree* and has the following properties:
  - the network has a single input node
  - all the capacitors are between a node and the ground
  - the network does not contain any resistive loops

Elmore delay formula

- The total resistance along a path is called the *path resistance* R_{ii}.

$$R_{44} = R_1 + R_3 + R_4$$

- The *shared path resistance* R_{ik} represents the resistance shared among the paths from the root node *s* to nodes *k* and *i*:

$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \rightarrow i) \cap path(s \rightarrow k)])$$

$R_{i4} = R_1 + R_3$ while $R_{i2} = R_1$.

- Assume now that each of the *N* nodes of the network is initially discharged to GND, and that a step input is applied at node *s* at time $t = 0$.
- The Elmore delay at node *i* is then given by the following expression:

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

Elmore delay formula

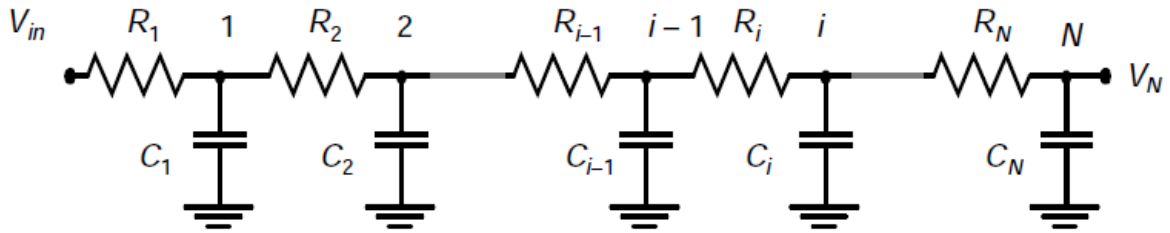


Figure 4.13 *RC* chain.

- This network is often encountered in digital circuits, and also it represents an approximative model of a resistive-capacitive wire.
- The Elmore delay is:

$$\tau_{DN} = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j = \sum_{i=1}^{N} C_i R_{ii}$$

$$\tau_{Di} = C_1 R_1 + C_2(R_1 + R_2) + \ldots + C_i(R_1 + R_2 + \ldots + R_i)$$

Time-Constant of Resistive-Capacitive Wire

- The model presented in the previous Figure can be used as an approximation of a resistive-capacitive wire.
- The wire with a total length of *L* is partitioned into *N* identical segments, each with a length of *L*/*N*.
- The resistance and capacitance of each segment are hence given by *rL*/*N* and *cL*/*N*, respectively.
- Using the Elmore formula, we can compute the dominant time-constant of the wire

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

- with $R = rL$ and $C = cL$ the total lumped resistance and capacitance of the wire.
- For $N \rightarrow +\infty$, this model asymptotically approaches the distributed *rc* line:

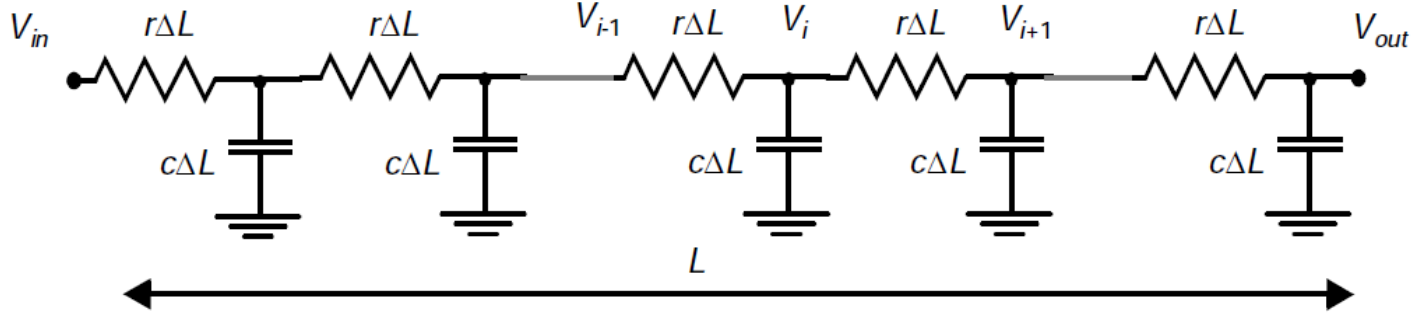
$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

Time-Constant of Resistive-Capacitive Wire

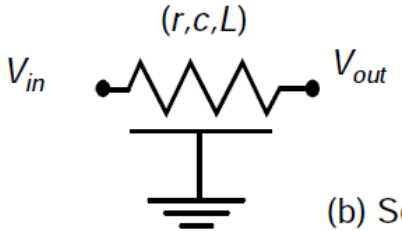
$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

- The equation leads to two important conclusions:
  - The delay of a wire is **a quadratic function of its length**!
    - Doubling the length of the wire quadruples its delay.
  - The delay of the distributed *rc*-line is **one half of the delay** that would have been predicted by the lumped *RC* model.
    - This confirms that the lumped model presents a pessimistic view on the delay of resistive wire.

The Distributed rc Line



(a) Distributed model



(b) Schematic symbol for distributed *RC* line

Figure 4.14 Distributed RC line wire-model and its schematic symbol.

The Distributed rc Line

- The voltage at node *i* of this network can be determined by solving the following set of partial differential equations:

$$c\Delta L\frac{\partial V_i}{\partial t} = \frac{(V_{i+1} - V_i) + (V_{i-1} - V_i)}{r\Delta L}$$

- For $\Delta L \to 0$, it becomes the well-known *diffusion equation*:

$$rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$$

- No closed-form solution exists for this equation, but approximative expressions can be derived:

$$V_{out}(t) = 2erfc\left(\sqrt{\frac{RC}{4t}}\right) \qquad t \ll RC$$

$$= 1.0 - 1.366e^{-2.5359\frac{t}{RC}} + 0.366e^{-9.4641\frac{t}{RC}} \qquad t \gg RC$$

The distributed rc Line

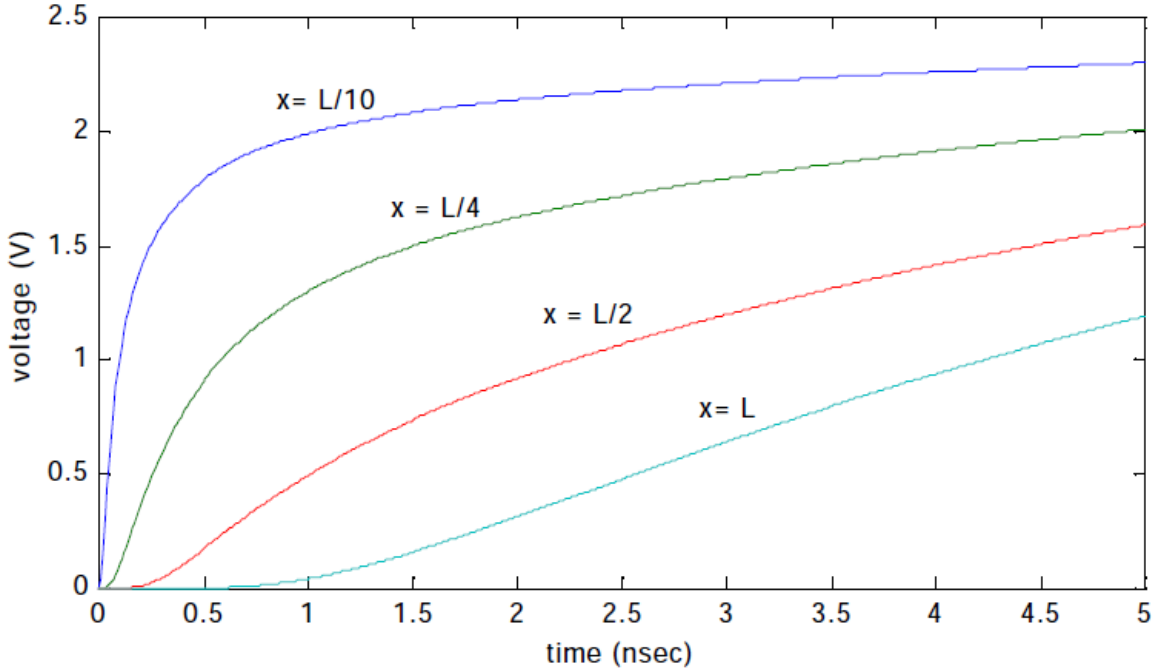


Figure 4.15 Simulated step response of resistive-capacitive wire as a function of time and place.

The distributed rc Line

Table 4.7 Step response of lumped and distributed *RC* networks—points of Interest.

Voltage range	Lumped *RC* network	Distributed *RC* network
$0 \rightarrow 50\%$ (t_p)	$0.69\ RC$	$0.38\ RC$
$0 \rightarrow 63\%$ (τ)	RC	$0.5\ RC$
$10\% \rightarrow 90\%$ (t_r)	$2.2\ RC$	$0.9\ RC$
$0\% \rightarrow 90\%$	$2.3\ RC$	$1.0\ RC$

Design Rules of Thumb

- An important question to answer when analyzing an interconnect network:
  - whether the effects of *RC* delays should be considered, or
  - whether we can get away with a simpler lumped capacitive model.
- ***rc* delays should only be considered when $t_{pRC} >> t_{pgate}$ of the driving gate**

$$L_{crit} >> \sqrt{\frac{t_{pgate}}{0.38rc}}$$

- ***rc* delays should only be considered when the rise (fall) time at the line input is smaller than *RC*, the rise (fall) time of the line.**

$$t_{rise} < RC$$

- with R and C the total resistance and capacitance of the wire.

The Transmission Line

- When the switching speeds of the circuits become sufficiently fast, and the wire has low resistance, the inductance of the wire starts to dominate the delay behavior, and transmission line effects must be considered.
- This is more precisely the case when the rise and fall times of the signal become comparable to the time of flight of the signal waveform across the line.

Transmission Line Model

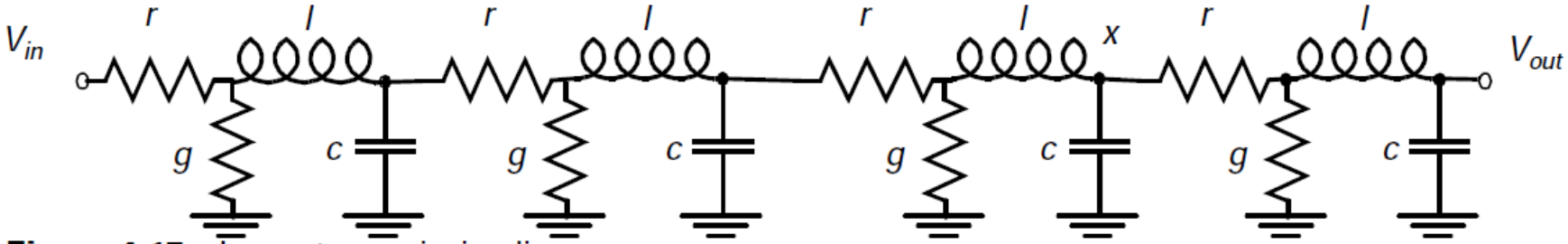


Figure 4.17 Lossy transmission line.

- The transmission line has the prime property that a signal propagates over the interconnection medium as a *wave*.
- This is in contrast to the distributed *rc* model, where the signal *diffuses* from the source to the destination.

Transmission Line Model

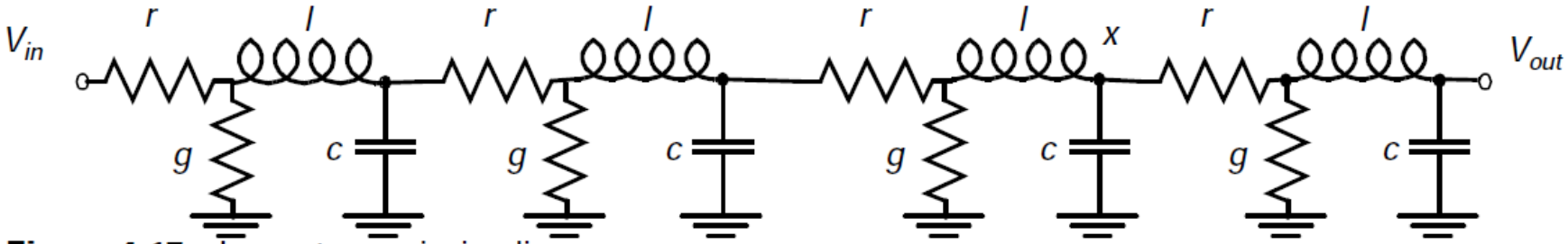


Figure 4.17 Lossy transmission line.

- Consider the point *x* at time *t:*

$$\frac{\partial v}{\partial x} = -ri - l\frac{\partial i}{\partial t}$$

$$\frac{\partial i}{\partial x} = -gv - c\frac{\partial v}{\partial t}$$

- Assuming that the leakage conductance *g* equals 0, we get the *wave propagation equation:*

$$\frac{\partial^2 v}{\partial x^2} = rc\frac{\partial v}{\partial t} + lc\frac{\partial^2 v}{\partial t^2}$$

The Lossless Transmission Line

- Let us first assume the resistance of the line is small, a *lossless transmission line*
- We get the *ideal wave* equation:

$$\frac{\partial^2 v}{\partial x^2} = lc\frac{\partial^2 v}{\partial t^2} = \frac{1}{\overline{v}^2}\frac{\partial^2 v}{\partial t^2}$$

- A step input propagates along the line with speed

$$\overline{v} = \frac{1}{\sqrt{lc}} = \frac{1}{\sqrt{\varepsilon\mu}} = \frac{c_0}{\sqrt{\varepsilon_r\mu_r}}$$

- Even though the values of both *l* and *c* depend on the geometric shape of the wire, their product is a constant and is only a function of the surrounding media.
- The propagation delay per unit wire length *(t_p)* is the inverse of the speed:

$$t_p = \sqrt{lc}$$

The Lossless Transmission Line

- Let us now analyze how a wave propagates along a lossless transmission line.
- Suppose that a voltage step *V* has been applied at the input and has propagated to point *x* of the line.

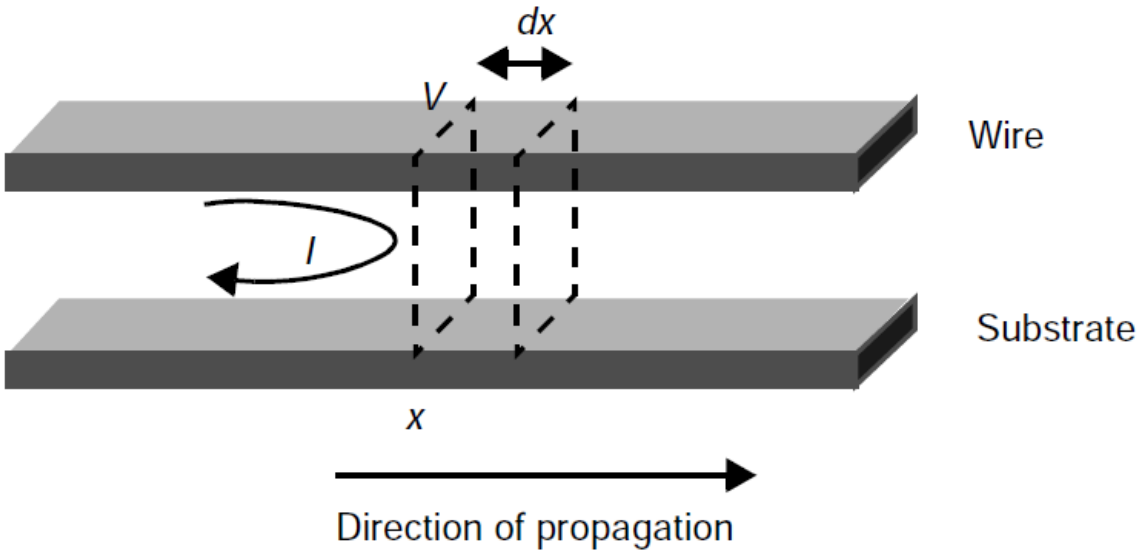


Figure 4.18 Propagation of voltage step along a lossless transmission line.

The Lossless Transmission Line

- All currents are equal to 0 at the right side of *x*, while the voltage over the line equals *V* at the left side.
- An additional capacitance *cdx* must be charged for the wave to propagate over an additional distance *dx*.
- This requires the following current:

$$I = \frac{\mathrm{d}Q}{\mathrm{d}t} = c\frac{\mathrm{d}x}{\mathrm{d}t}V = c\bar{v}V = \sqrt{\frac{c}{l}}V$$

- since the propagation speed of the signal *dx/dt* equals $\bar{v}$.
- This means that the signal sees the remainder of the line as a real impedance,

$$Z_0 = \frac{V}{I} = \sqrt{\frac{l}{c}} = \frac{\sqrt{\varepsilon\mu}}{c} = \frac{1}{c\bar{v}}.$$

The Lossless Transmission Line

$$Z_0 = \frac{V}{I} = \sqrt{\frac{l}{c}} = \frac{\sqrt{\varepsilon\mu}}{c} = \frac{1}{c\overline{v}}.$$

- This impedance, called the *characteristic impedance* of the line, is a function of the dielectric medium and the geometry of the conducting wire and isolator, and is independent of the length of the wire and the frequency.
- Typical values of the characteristic impedance of wires in semiconductor circuits range from 10 to 200 Ω.

Termination

- The behavior of the transmission line is strongly influenced by the termination of the line.
- The termination determines how much of the wave is reflected upon arrival at the wire end.
- This is expressed by the *reflection coefficient* ρ that determines the relationship between the voltages and currents of the incident and reflected waveforms,

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{-I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$

- *R* is the value of the termination resistance.
- The total voltages and currents at the termination end are the sum of incident and reflected waveforms

$$V = V_{inc}(1 + \rho)$$

$$I = I_{inc}(1 - \rho)$$

Termination

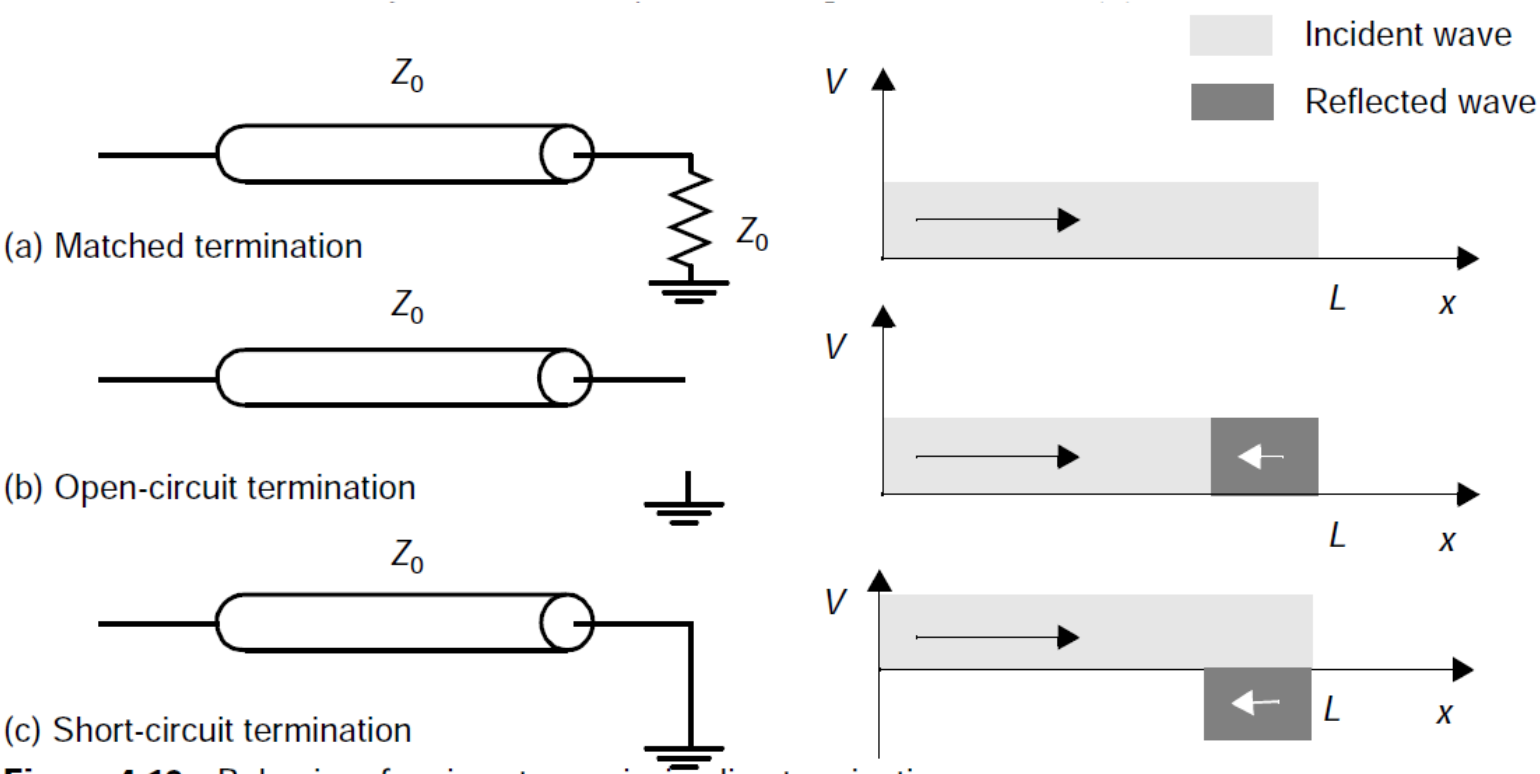


Figure 4.19 Behavior of various transmission line terminations.

Termination

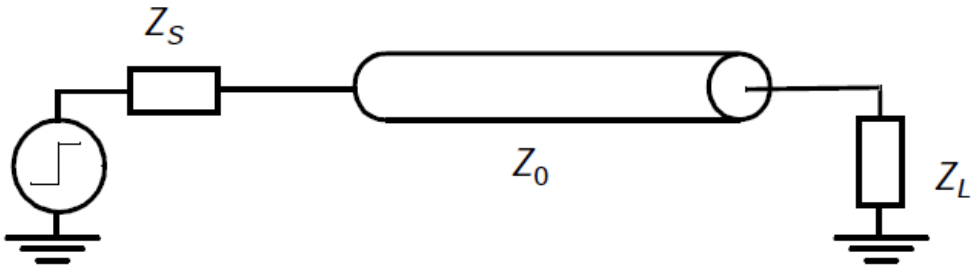
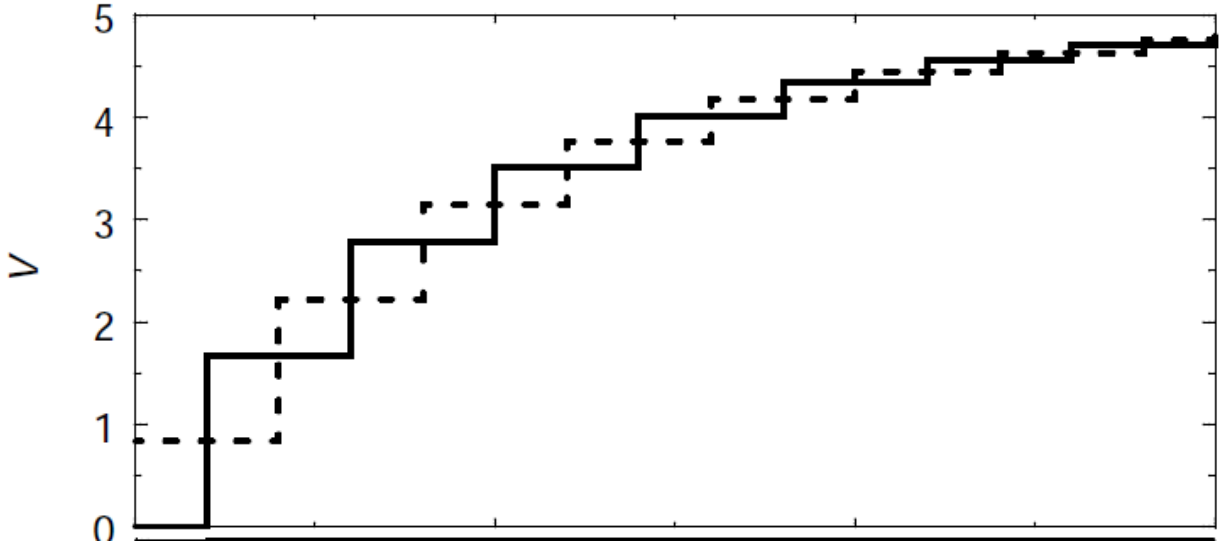


Figure 4.20 Transmission line with terminating impedances.

- Consider first the case where the wire is open at the destination end, or $Z_L = \infty$, and $\rho_L = 1$.
- Three possible scenarios are sketched

$$R_S = 5\ Z_0,\ R_S = Z_0, \text{ and } R_S = 1/5\ Z_0.$$

Termination



(a) $R_S = 5Z_0$, $R_L = \times$

$$V_{source} = (Z_0 / (Z_0 + R_S))\, V_{in} = 1/6 \times 5\ \text{V} = 0.83\ \text{V}$$

$$\rho_S = \frac{5Z_0 - Z_0}{5Z_0 + Z_0} = \frac{2}{3}$$

Termination

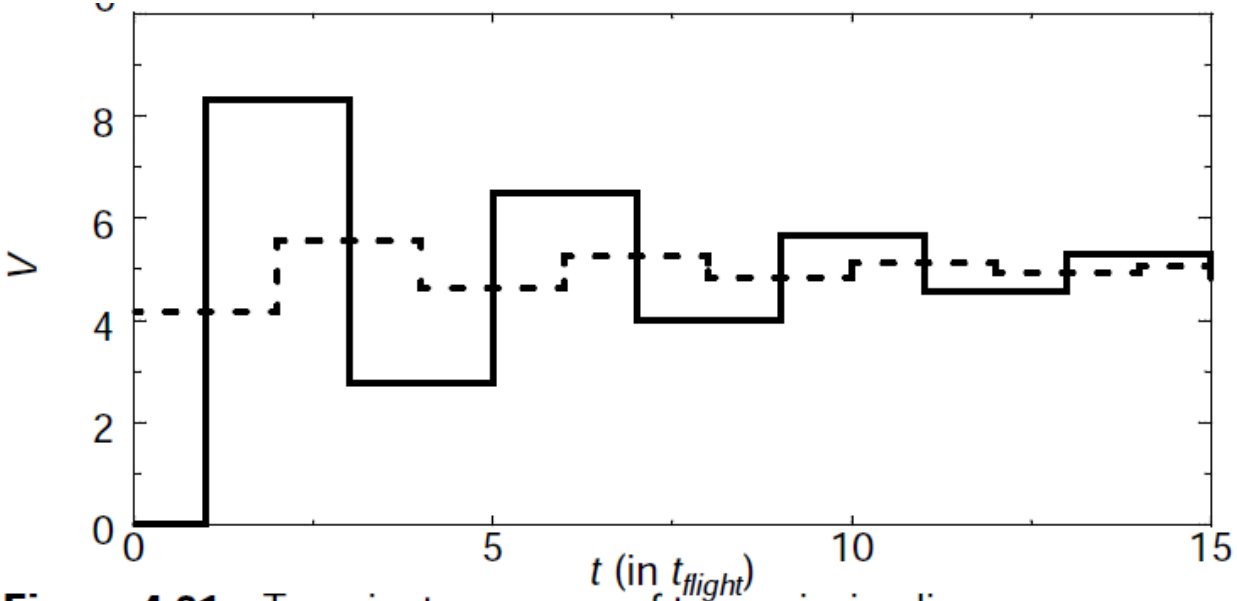
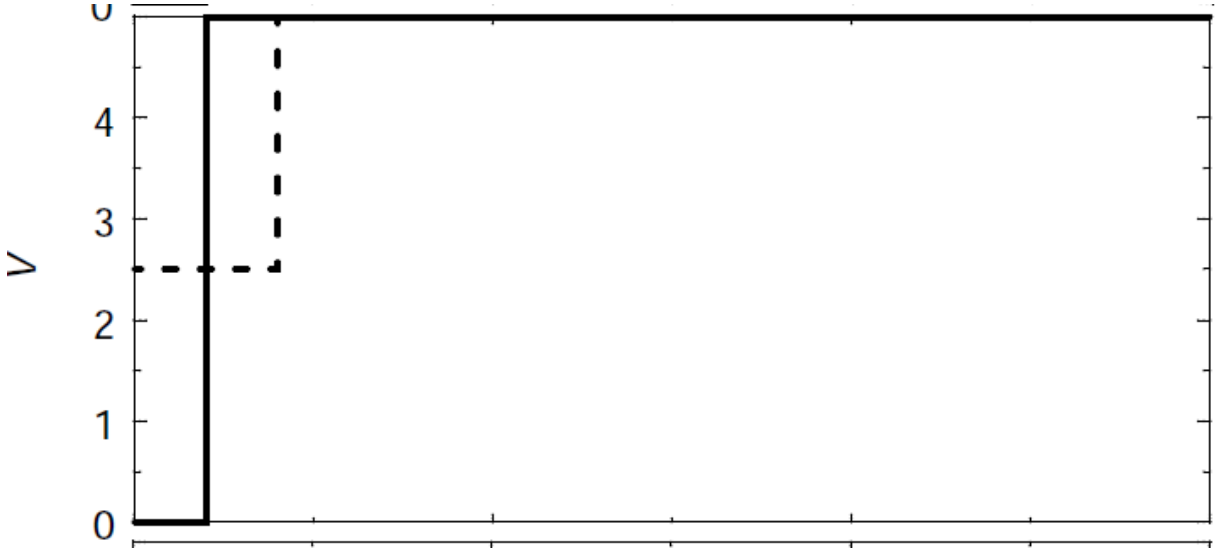


Figure 4.21 Transient response of transmission line.

(c) $R_S = Z_0/5$, $R_L = \times$

$$\rho_S = -2/3$$

Termination



(b) $R_S = Z_0$, $R_L = \times$

Capacitive Termination

- Loads in MOS digital circuits tend to be of a capacitive nature.
- Z_0 determines the current that can be supplied to charge capacitive load C_L.
- From the load's point of the view, the line behaves as a resistance with value Z_0.
- The transient response at the capacitor node displays a time constant Z_0C_L.

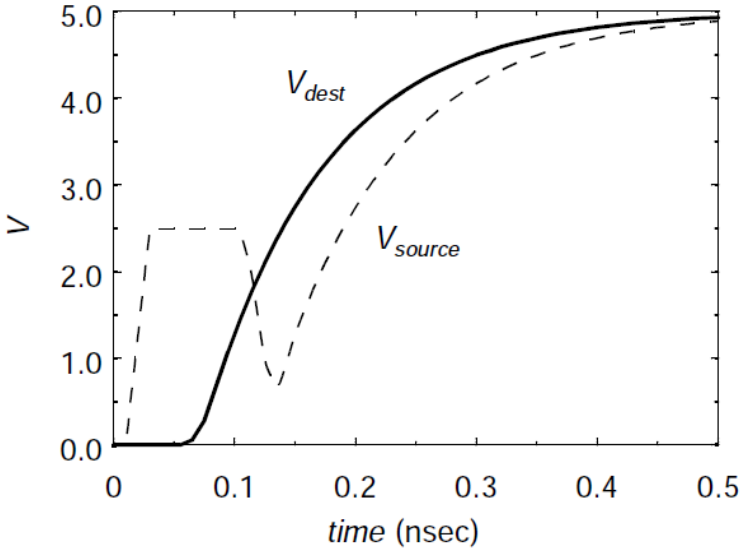


Figure 4.24 Capacitively terminated transmission line: R_S = 50 Ω, $R_L = \infty$, C_L = 2 pF, Z_0 = 50 Ω, t_{flight} = 50 psec.

The Lossy Transmission Line

- The response of a lossy *RLC line* to a unit step combines wave propagation with a diffusive component.
- The step still propagates as a wave but the amplitude is attenuated along the line:

$$\frac{V_{step}(x)}{V_{step}(0)} = e^{-\frac{r}{2Z_0}x}$$

- The farther it is from the source, the more the response resembles the behavior of a distributed *RC* line.
- In fact, the resistive effect becomes dominant, and the line behaves as a distributed *RC* line when R (= rL, the total resistance of the line) >> $2\,Z_0$.

Design Rules of Thumb

- When it is appropriate to consider transmission line effects?

- **Transmission line effects should be considered when the rise or fall time of the input signal (t_r, t_f) is smaller than the time-of-flight of the transmission line (t_{flight}).**

- **Transmission line effects should only be considered when the total resistance of the wire is limited:**

$$R < 5Z_0$$

- **The transmission line is considered lossless when the total resistance is substantially smaller than the characteristic impedance, or**

$$R < \frac{Z_0}{2}$$

From:

- J. M. Rabaey, A. Chandrakasan, B. Nikolic, «Digital Integrated Circuits: A Design Perspective», Pearson, 2003
  - Cap. 4.1, 4.2, 4.4