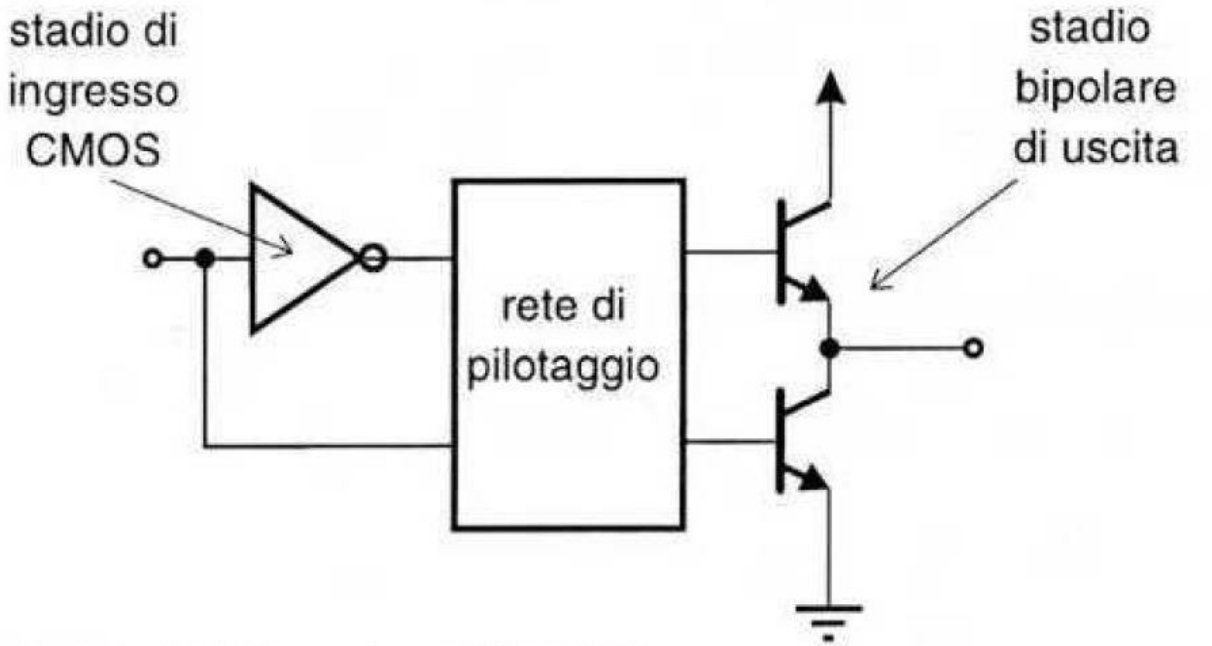
UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

BiCMOS Logic, Wired Logic, Three state logic

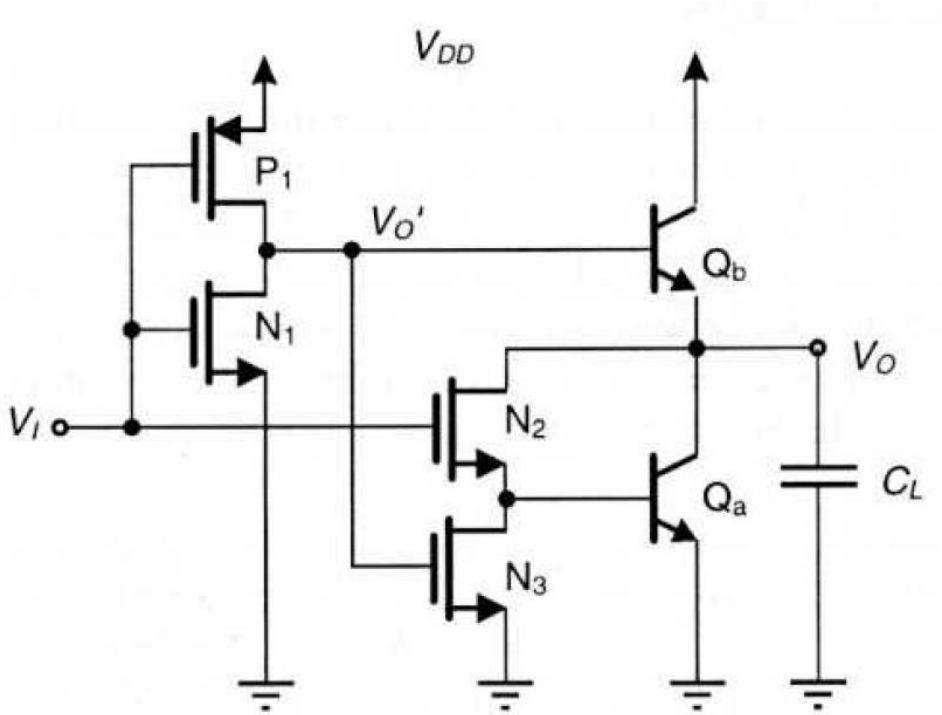
A.Carini – Digital Integrated Circuits

BiCMOS inverter



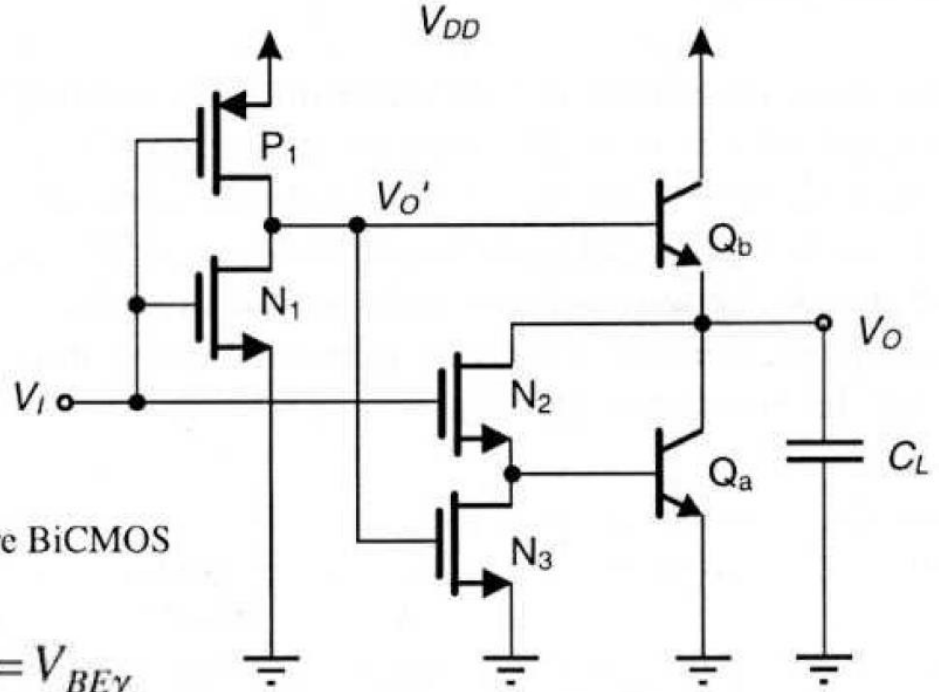
Schema di principio dell'invertitore BiCMOS

BiCMOS inverter



Schema elettrico dell'invertitore elementare BiCMOS

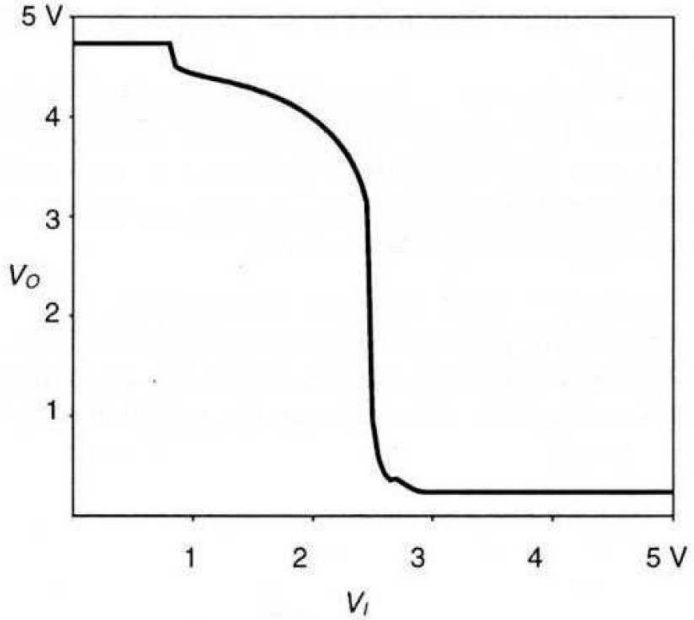
BiCMOS inverter



Schema elettrico dell'invertitore elementare BiCMOS

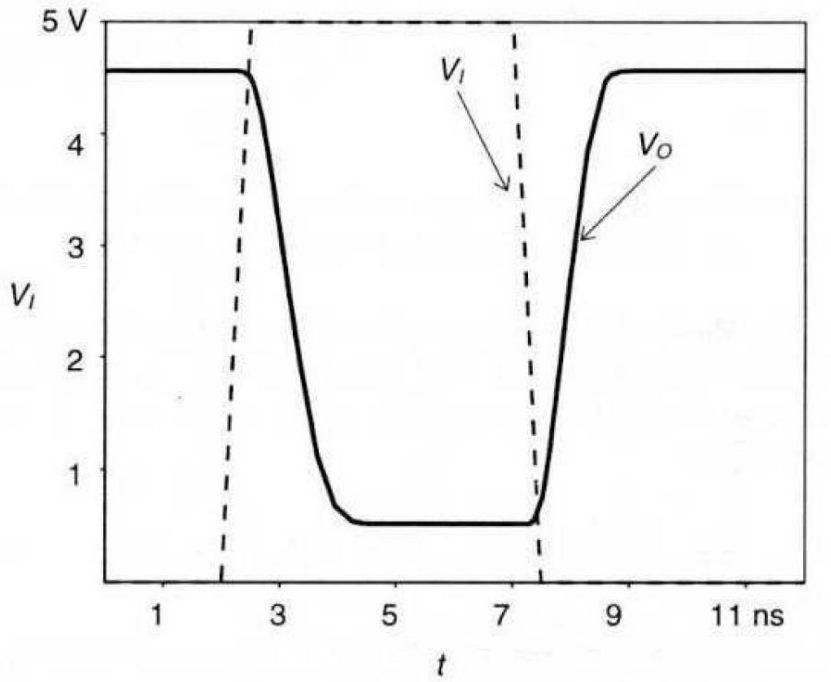
$$V_{OH} = V_{DD} - V_{BE\gamma} \; ; \qquad V_{OL} = V_{BE\gamma}$$

BiCMOS inverter



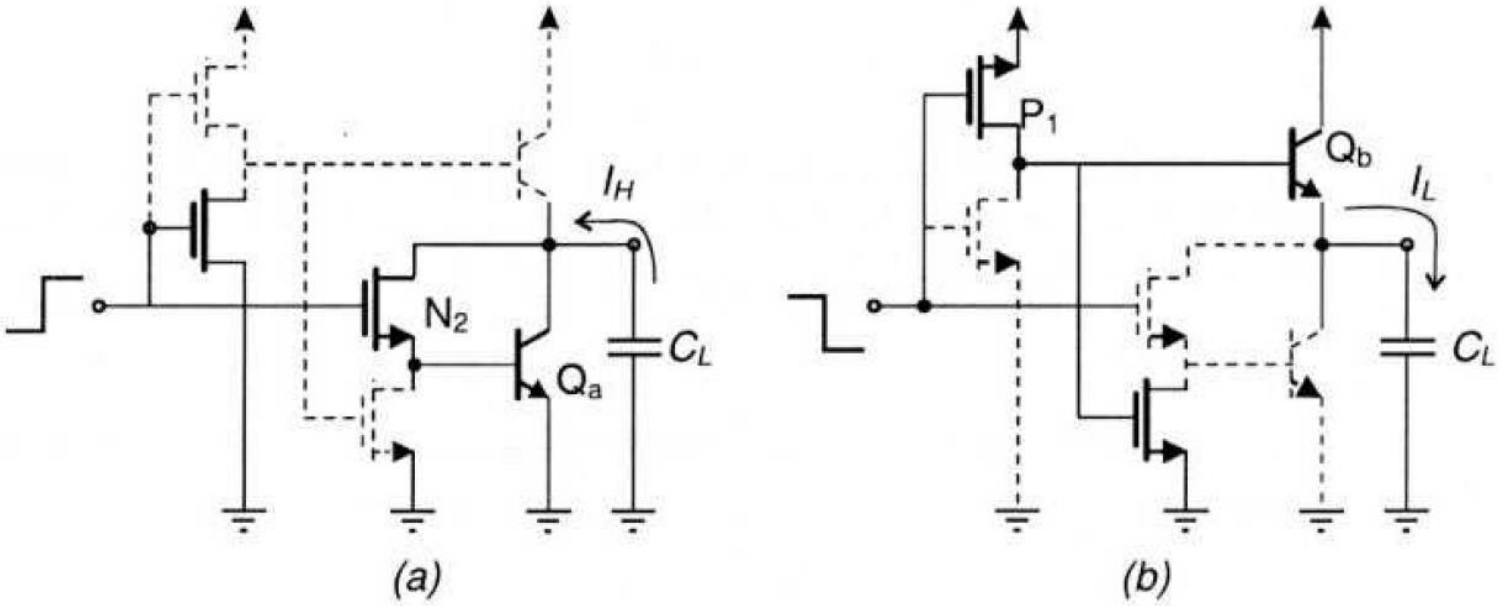
Simulazione SPICE della caratteristica di trasferimento dell'invertitore BiCMOS di Figura 10.23. I valori dei parametri sono: $W/L|_N = 2\ \mu m/1\ \mu m$, $W/L|_P = 5\ \mu m/1\ \mu m$, $V_{TN} = |V_{TP}| = 0.8\ V$, $\beta_F = 50$.

BiCMOS inverter



Comportamento dinamico dell'invertitore BiCMOS caricato da una capacità C_L= 5 pF

BiCMOS inverter



Reti equivalenti semplificate per la dinamica dell'invertitore BiCMOS: a) rete per la transizione alto-basso; b) rete per la transizione basso-alto

BiCMOS inverter

Caso a) :

$$I_H = I_{Qa} + I_{N2} = (\beta_F + 1) K_{N2} [V_{DD} - V_{BEa} - V_T]^2$$

$$t_{PHL} = \frac{C_L (V_{OH} - V_{OL})}{2\, I_H}$$

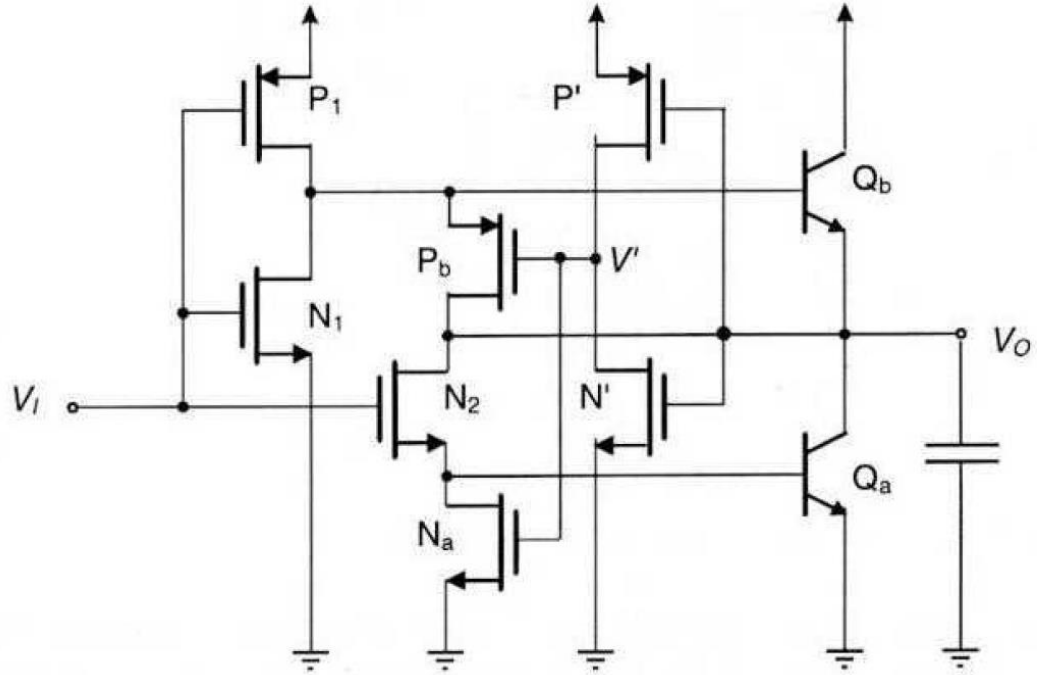
$$t_{PHL} = \frac{C_L (V_{DD} - 2V_{BE\gamma})}{2(\beta_F + 1) K_{N2} [V_{DD} - V_{BEa} - V_T]^2}$$

Caso b) :

$$I_L = I_{Qb} + I_{P1} = (\beta_F + 1) K_{P1} [V_{DD} - V_T]^2$$

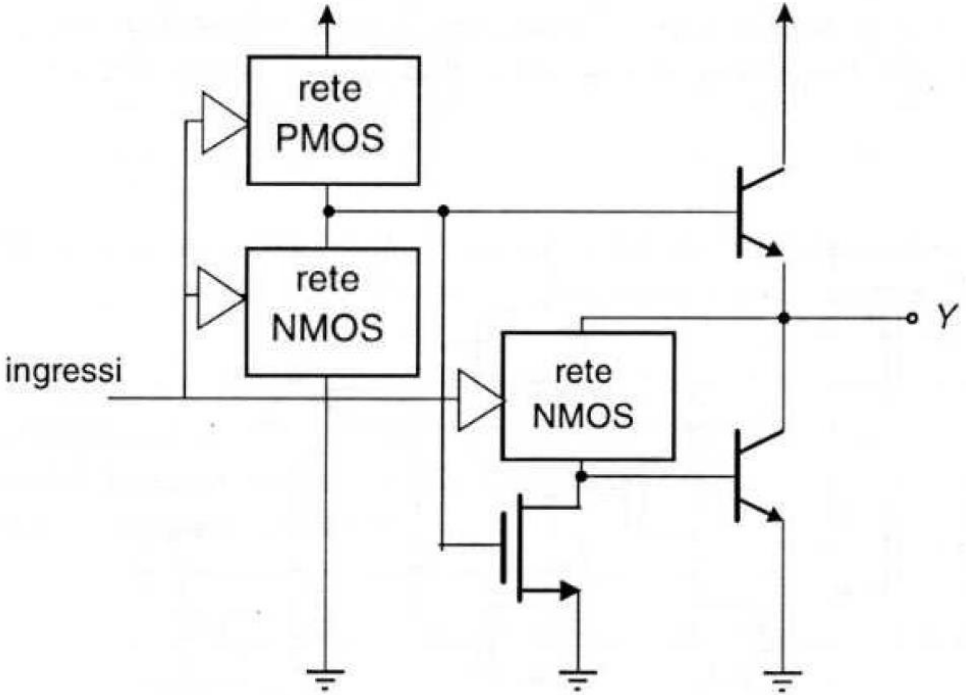
$$t_{PLH} = \frac{C_L (V_{DD} - 2V_{BE\gamma})}{2(\beta_F + 1) K_{P1} [V_{DD} - V_T]^2}$$

BiCMOS inverter



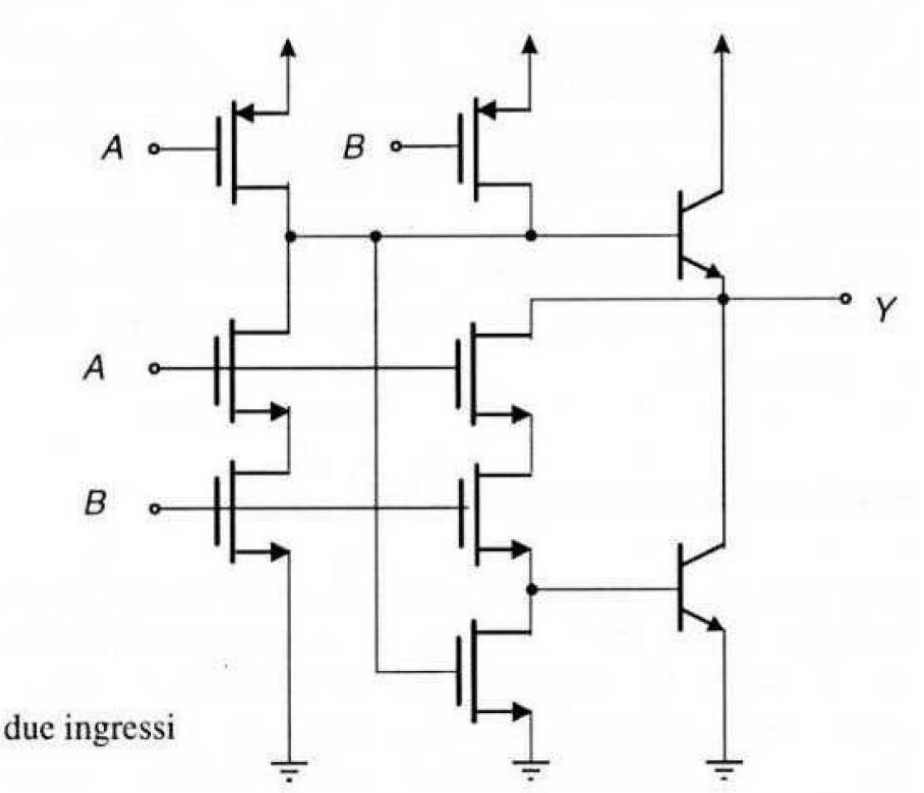
Invertitore BiCMOS con escursione logica completa

BiCMOS inverter



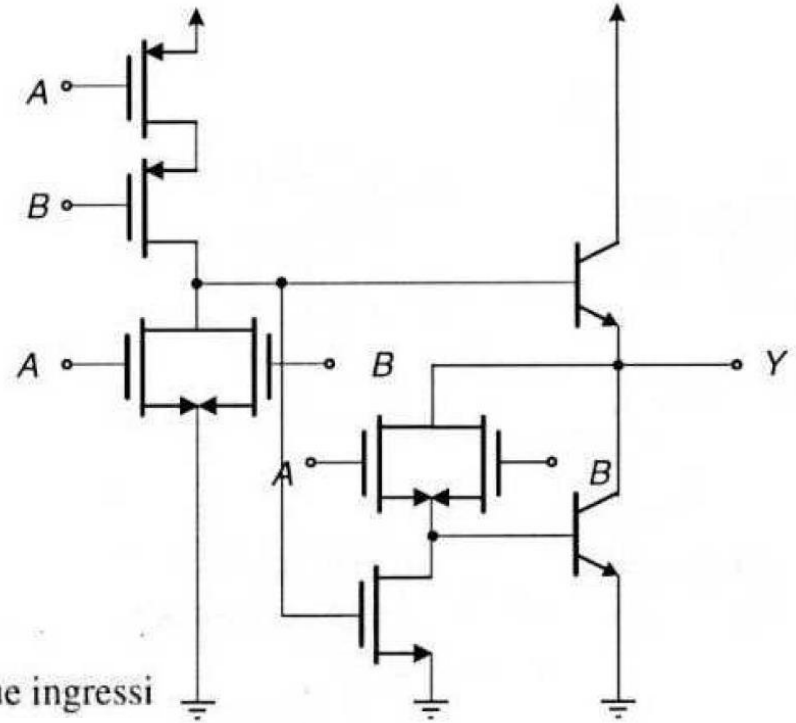
Circuito di principio di una porta logica BiCMOS

BiCMOS inverter



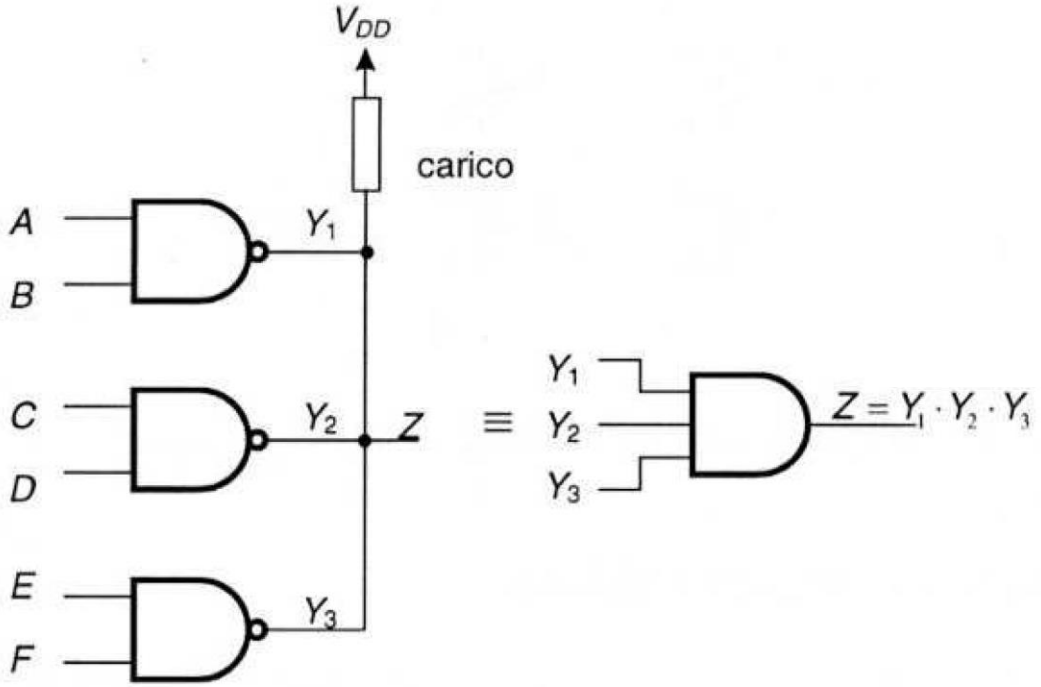
Porta logica NAND BiCMOS a due ingressi

BiCMOS inverter

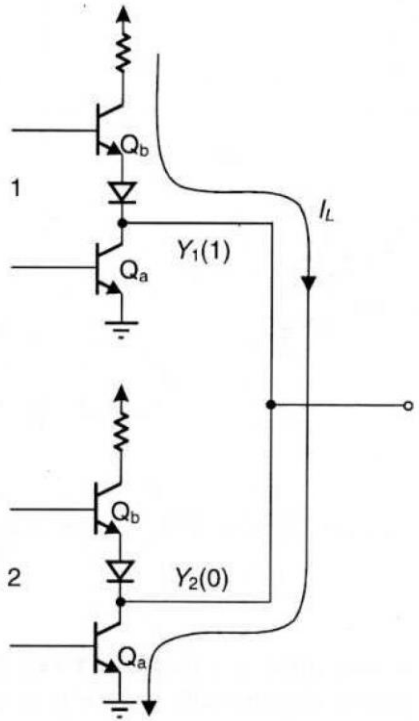


Porta logica NOR BiCMOS a due ingressi

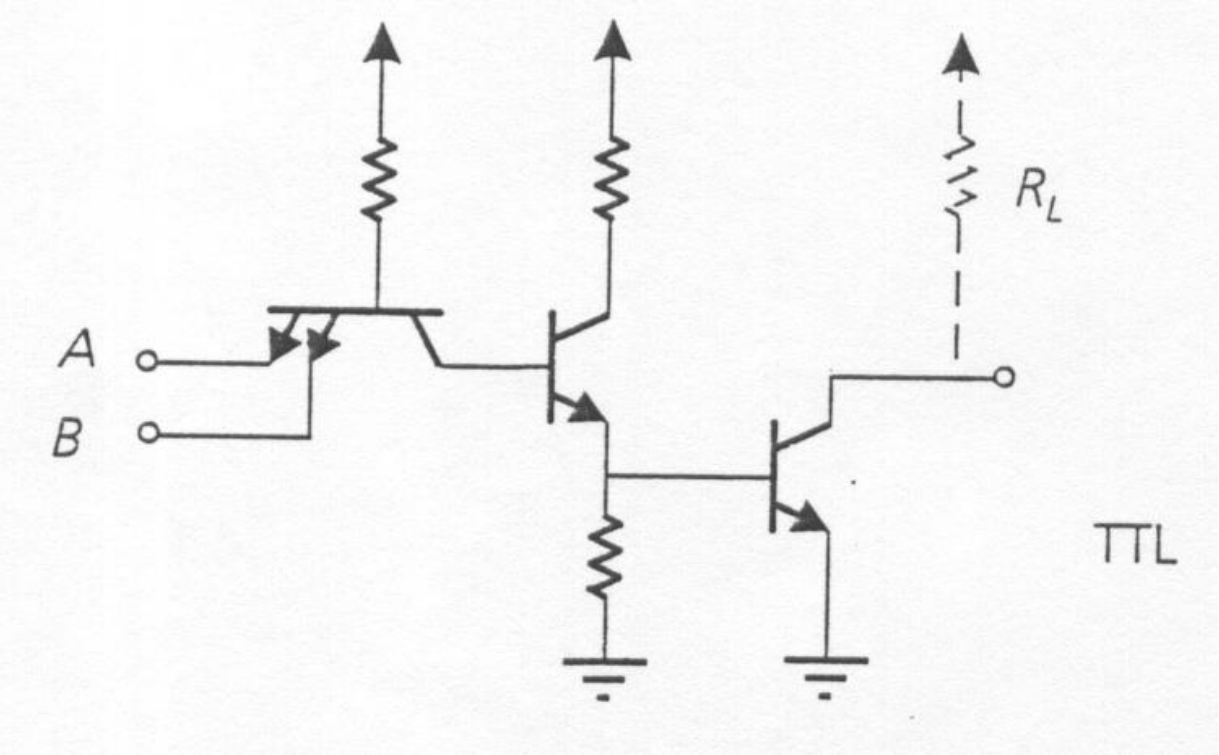
Wired logic



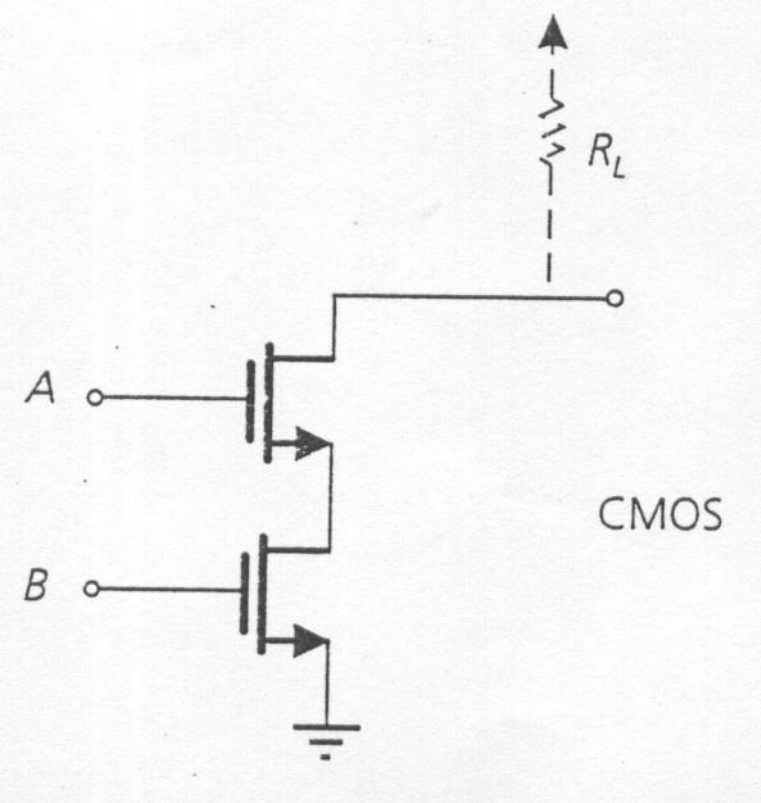
Wired logic

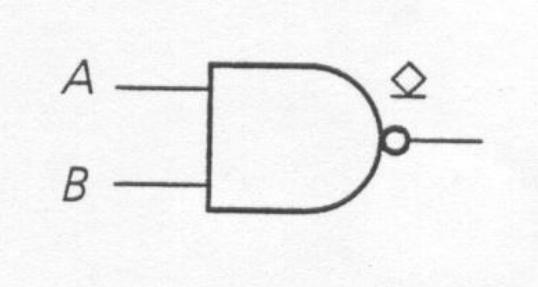


Wired logic

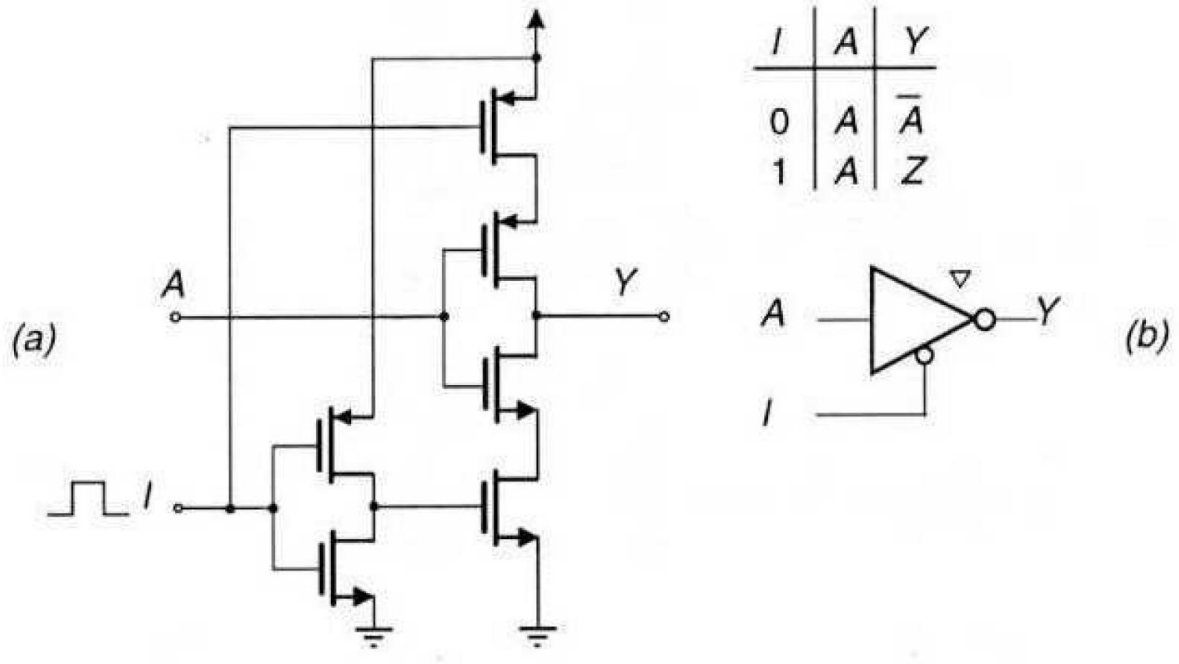


Wired logic

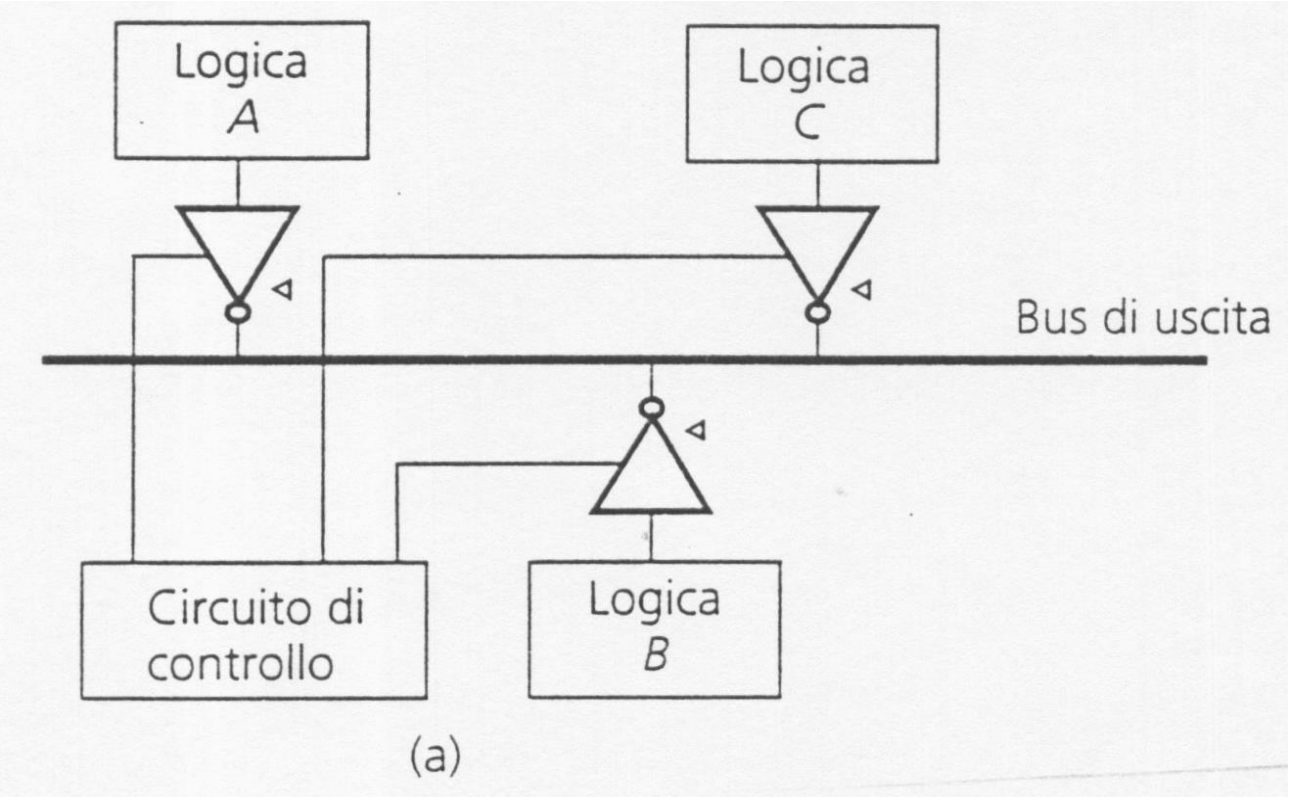




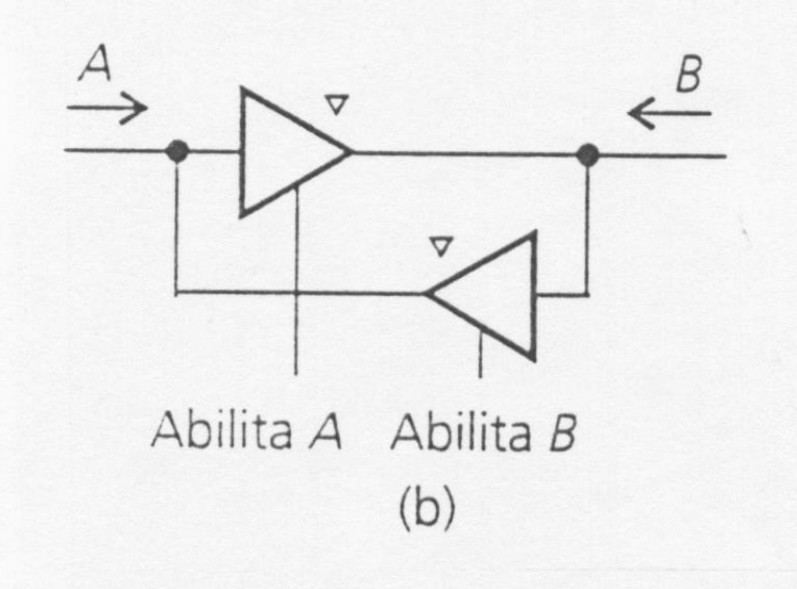
Three-state logic

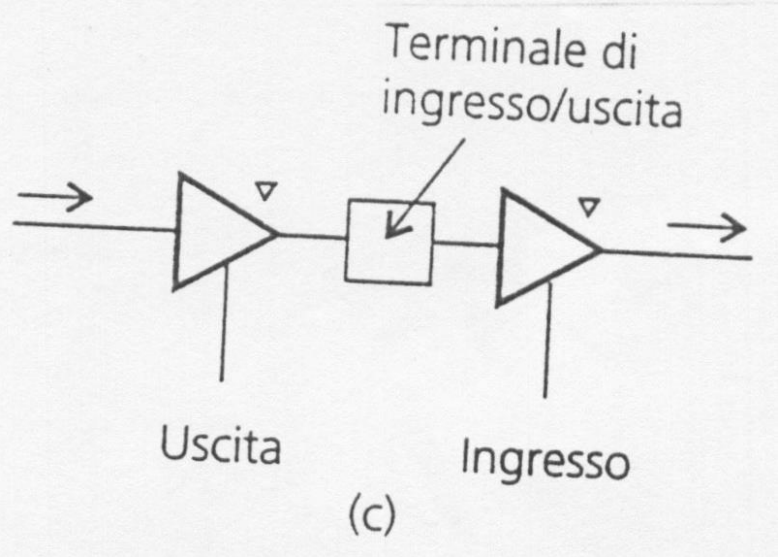


Three-state logic



Three-state logic





Vedere:

- Paolo Spirito, “Elettronica Digitale”, Ed. McGraw-Hill
  - Cap. 9.3-9.4, 9.7