UNIVERSITÀ
DEGLI STUDI DI TRIESTE

dipartimento
di ingegneria
e architettura

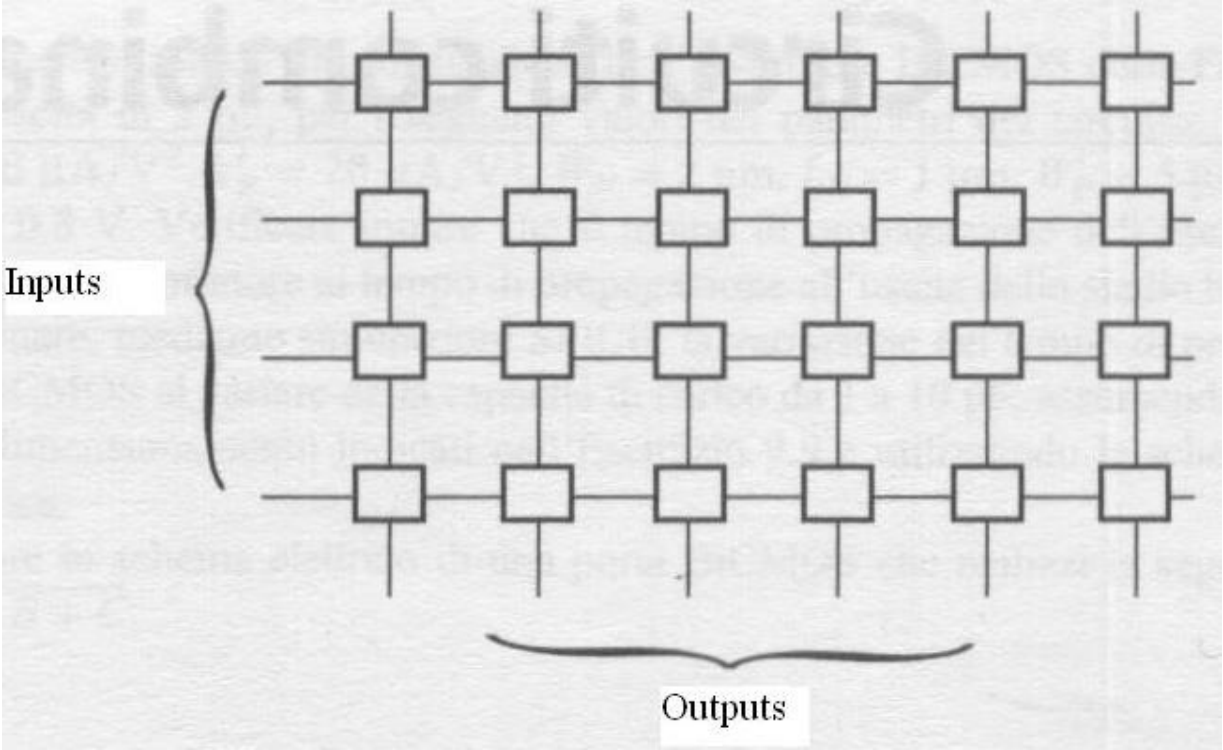
Combinational circuits

A.Carini – Digital Integrated Circuits

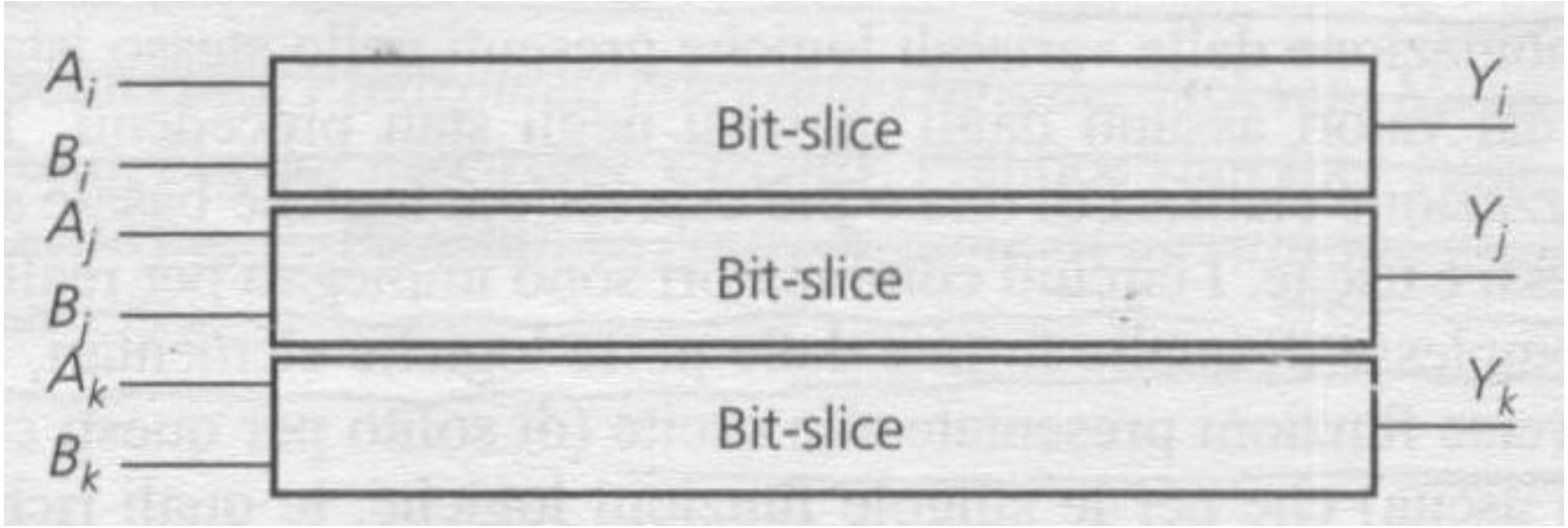
Combinational circuits

- Implement the following functions:
  - Numerical operations
  - Data addressing and selection
    - Coders and decodes
    - Multiplexers and demultiplexers
  - Implementation of generic logic functions
    - Logic elements
    - Programmable logic arrays

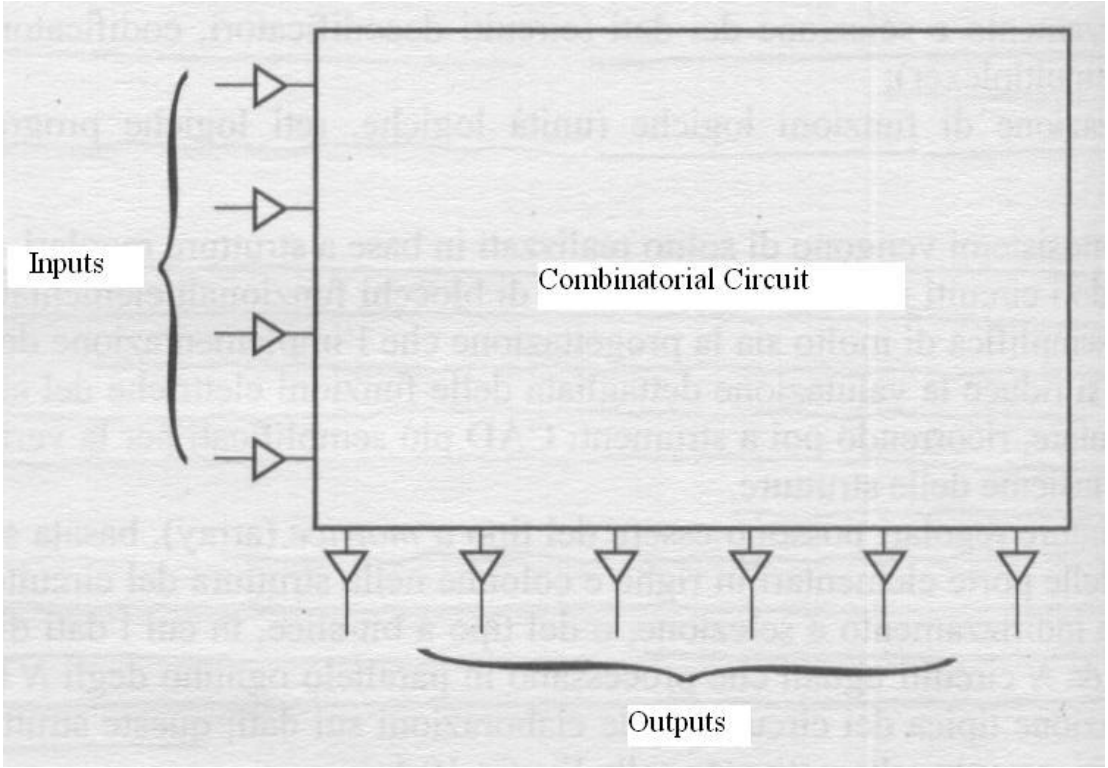
Matrix structure



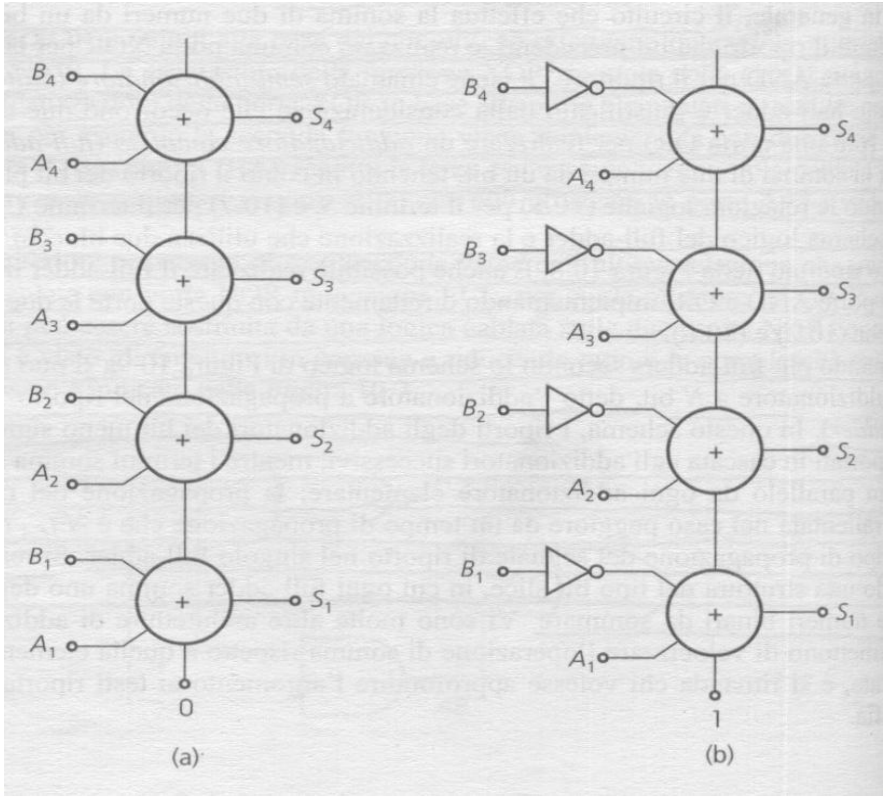
Bit-slice



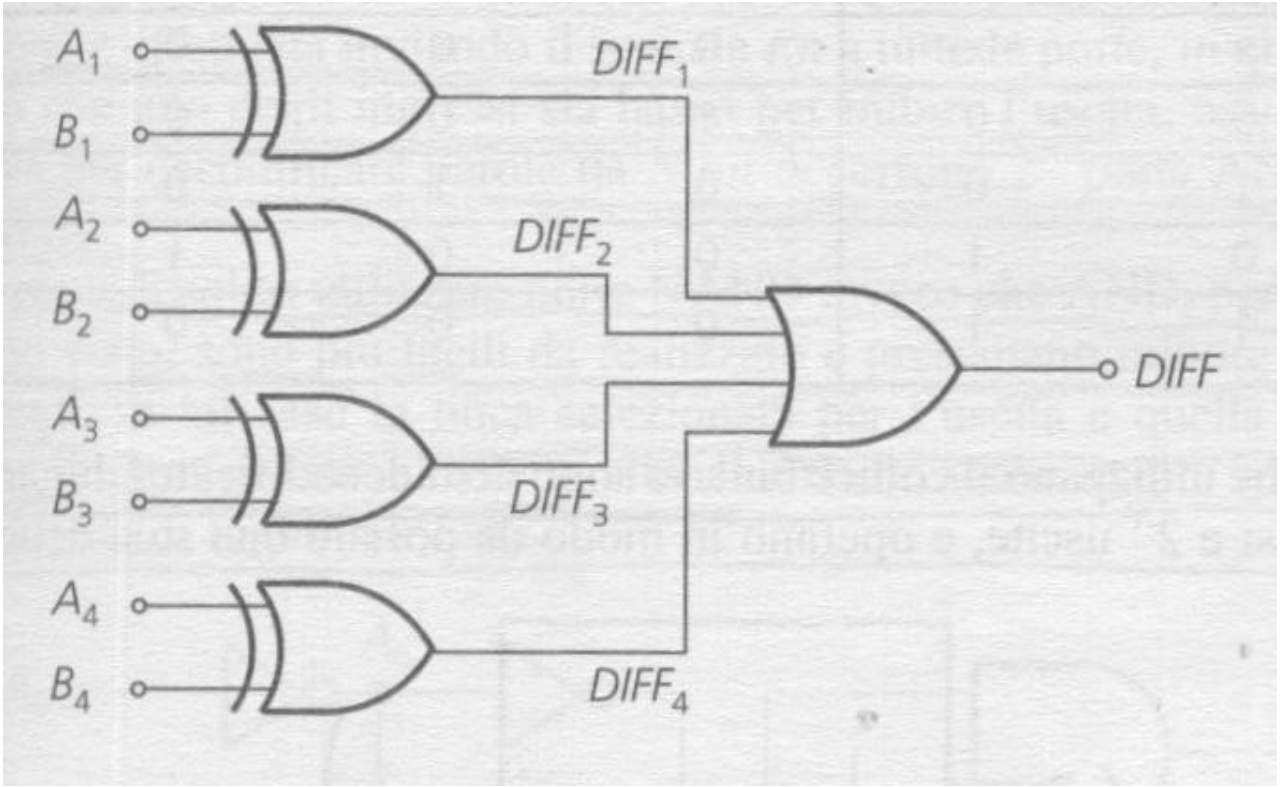
Input and output buffer stages



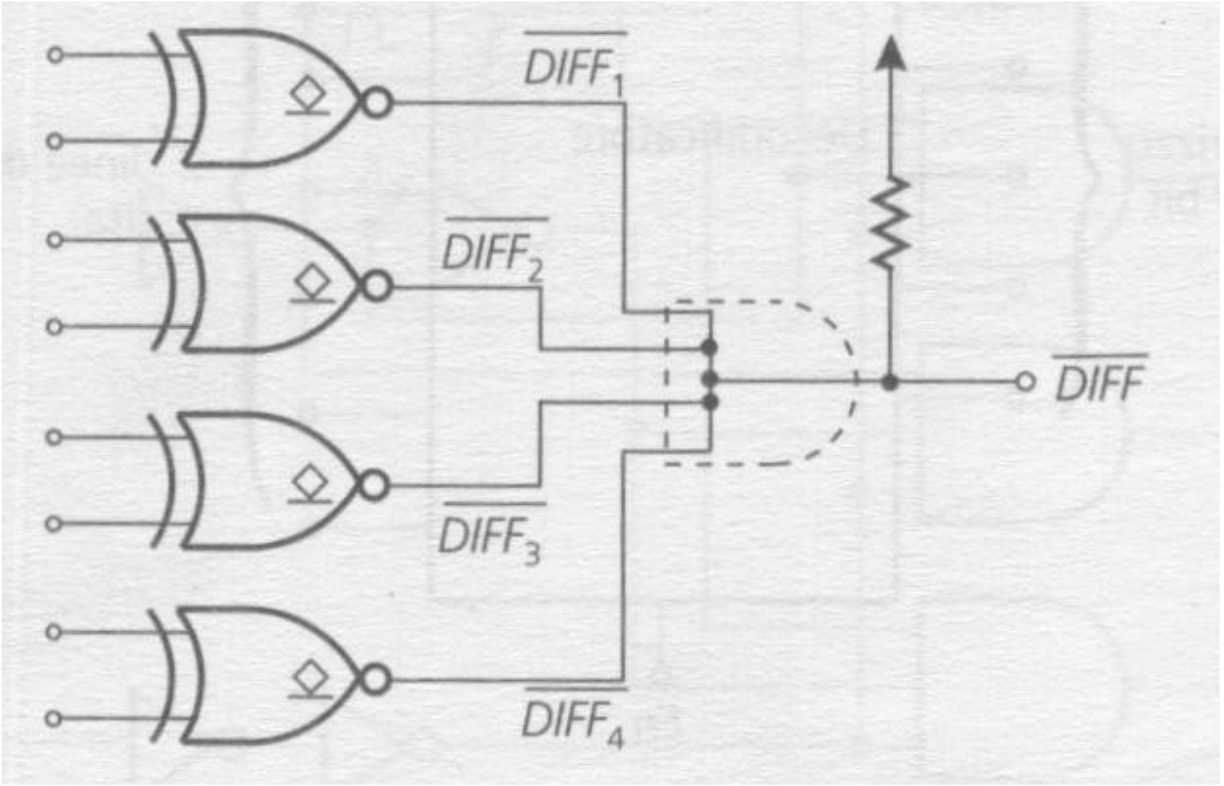
Adders and subtracters



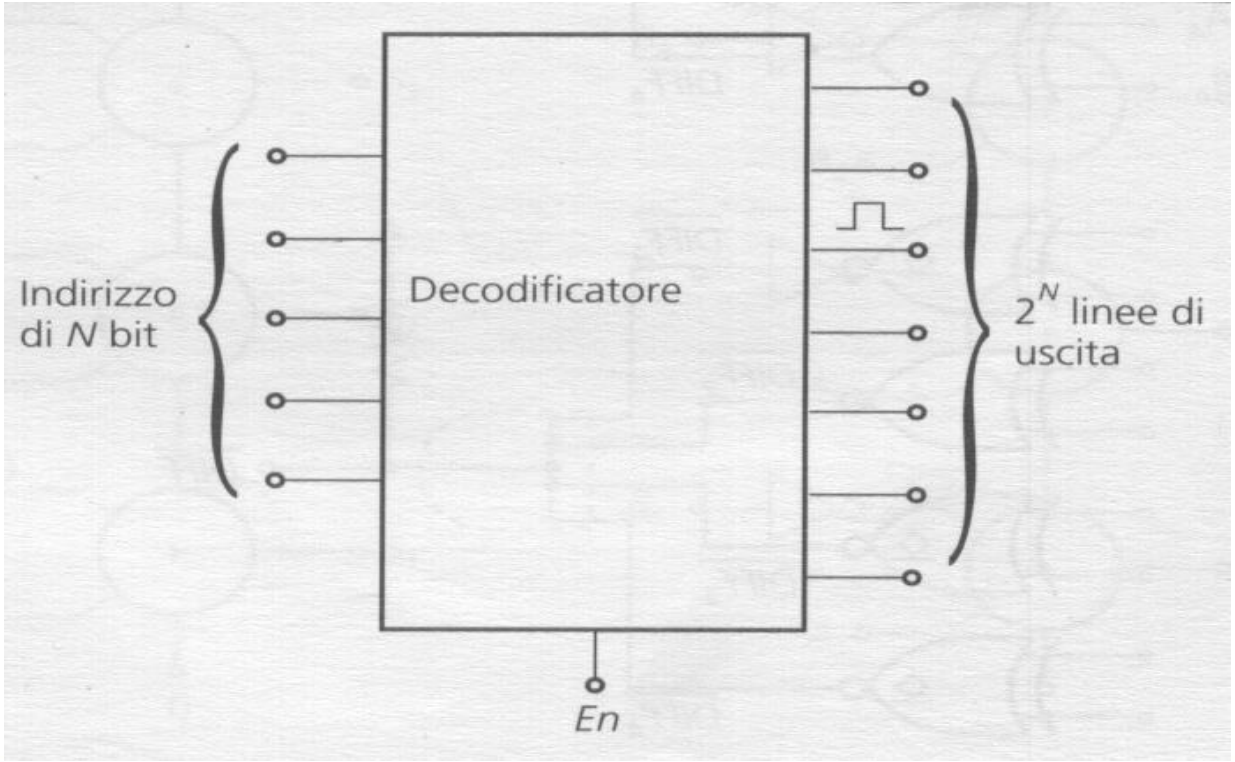
Comparators



Comparators



Decoders

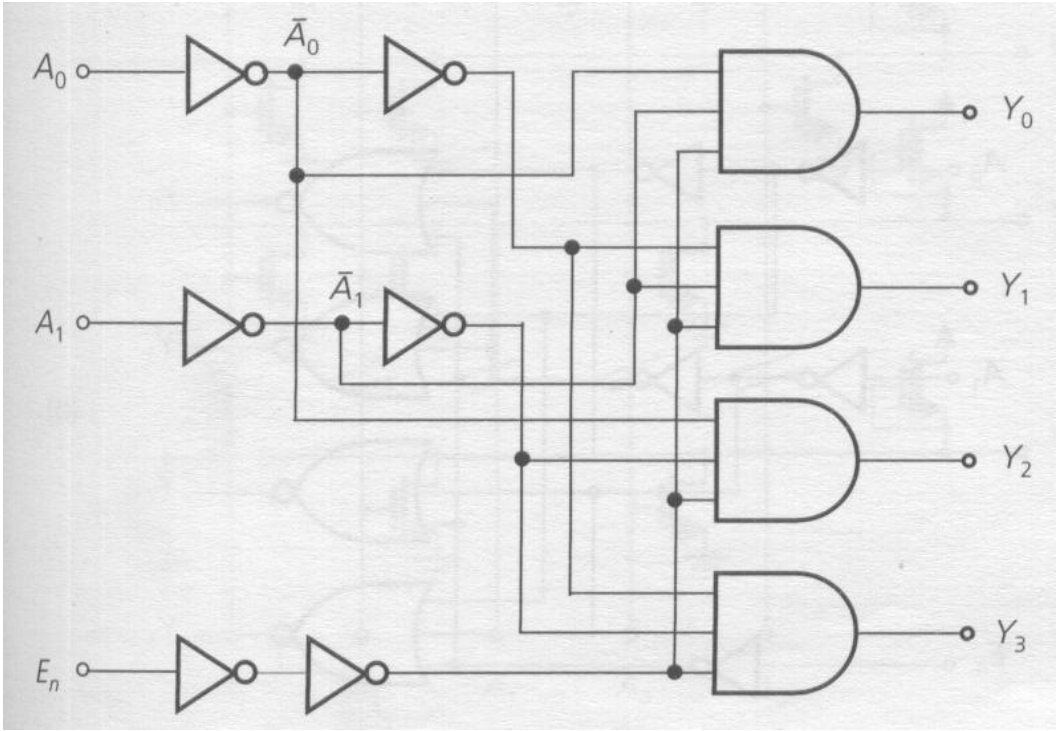


Decoders

Tabella 10.1 Tabella della verità per un decodificatore da 2 bit.

Ingressi			Uscite			
En	A_0	A_1	Y_0	Y_1	Y_2	Y_3
0	x	x	0	0	0	0
1	0	0	1	0	0	0
1	1	0	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1

Decoders



Decoders

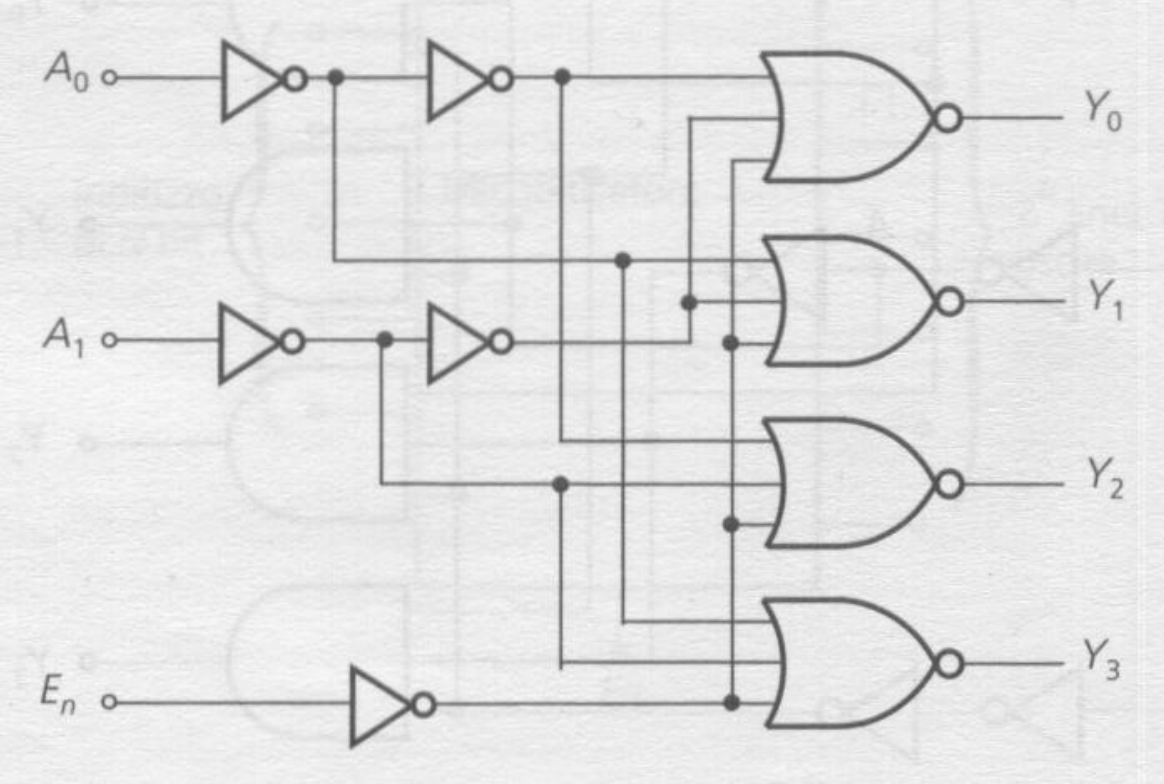
$$Y_0 = \overline{A_0} \cdot \overline{A_1} = \overline{A_0 + A_1}$$

$$Y_1 = A_0 \cdot \overline{A_1} = \overline{\overline{A_0} + A_1}$$

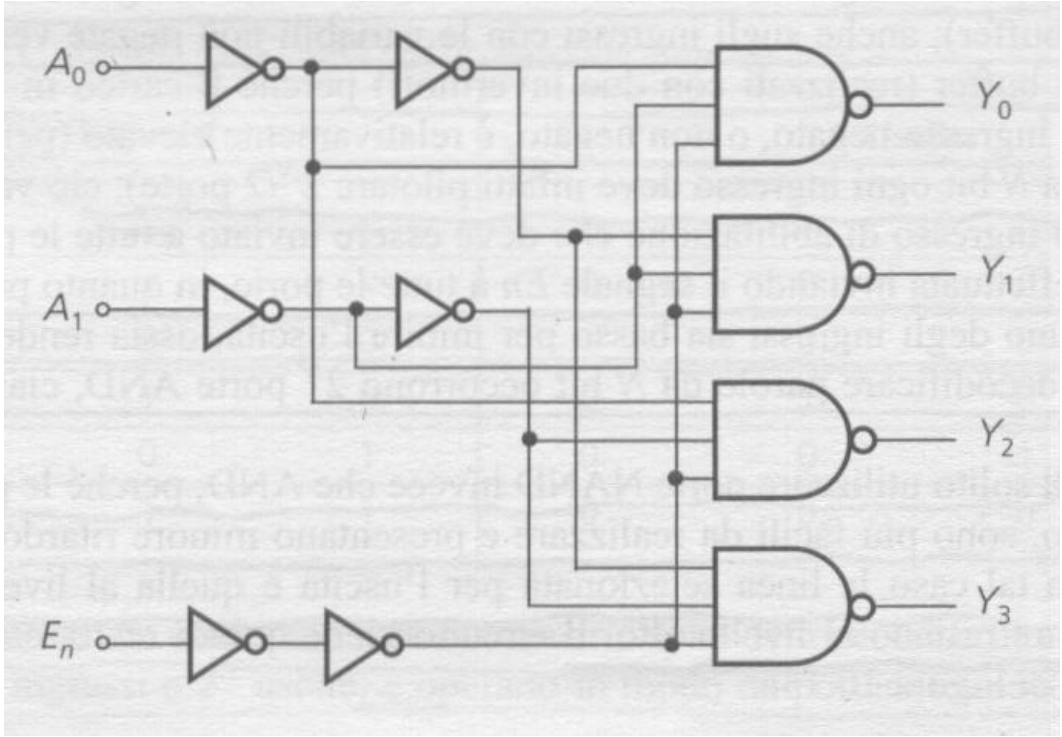
$$Y_2 = \overline{A_0} \cdot A_1 = \overline{A_0 + \overline{A_1}}$$

$$Y_3 = A_0 \cdot A_1 = \overline{\overline{A_0} + \overline{A_1}}$$

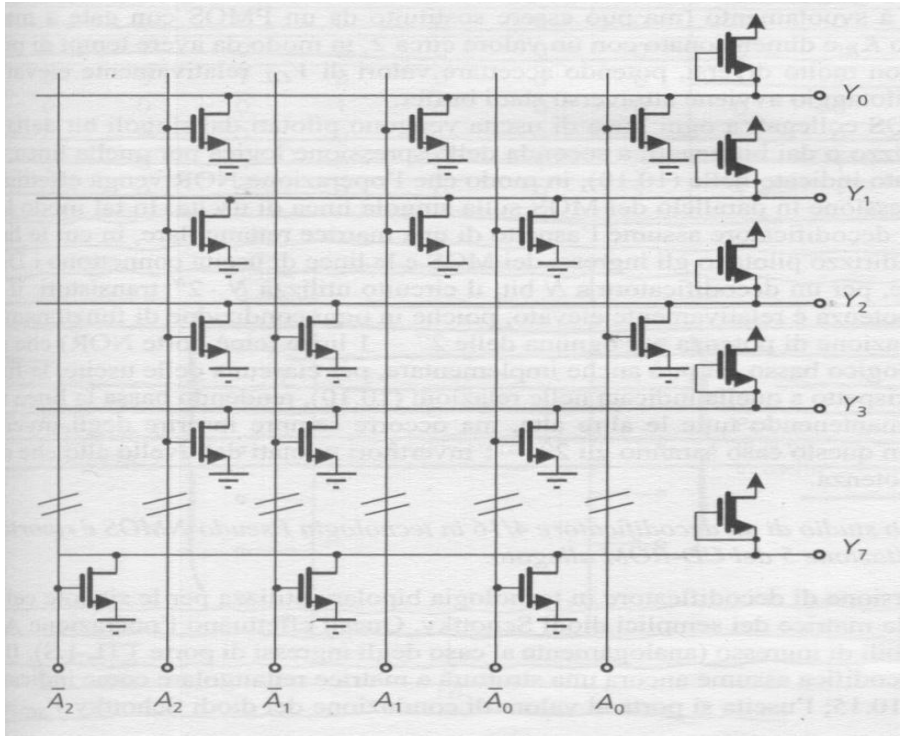
Decoders



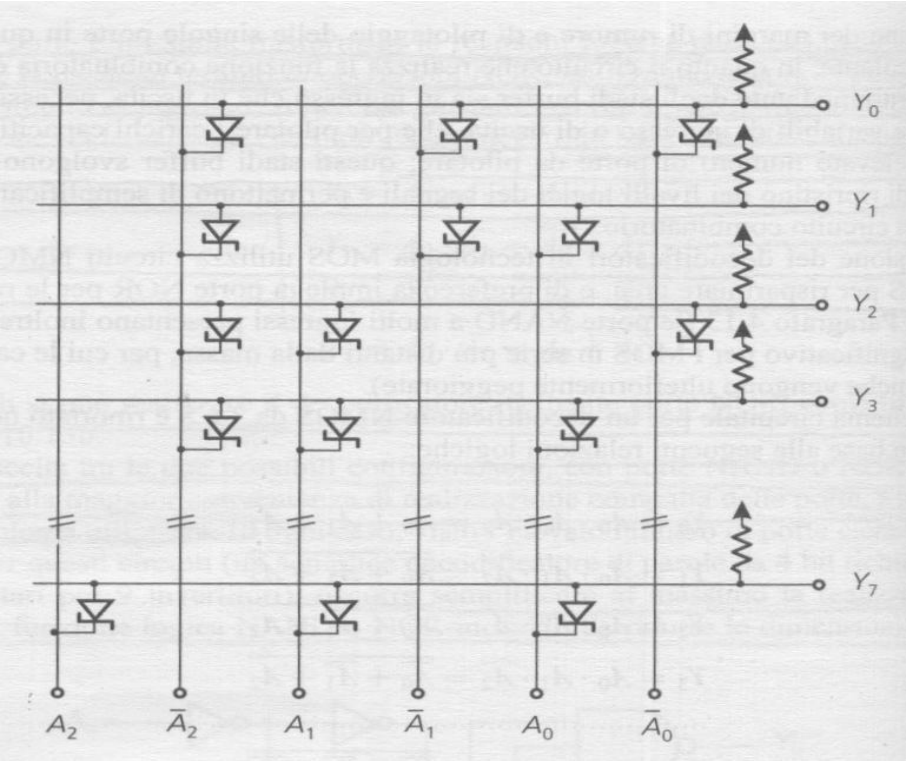
Decoders



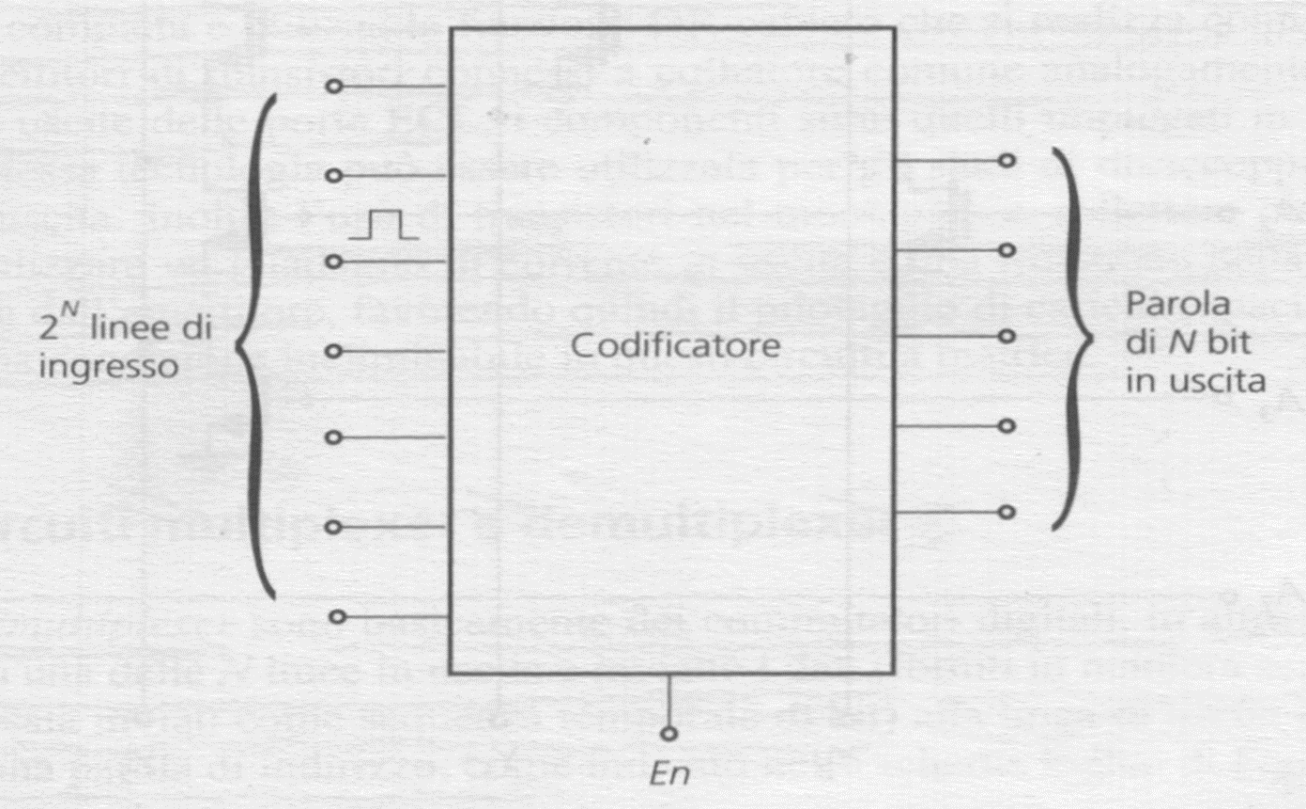
Decoders



Decoders



Encoders


2^N linee di ingresso
Codificatore
Parola di N bit in uscita
En

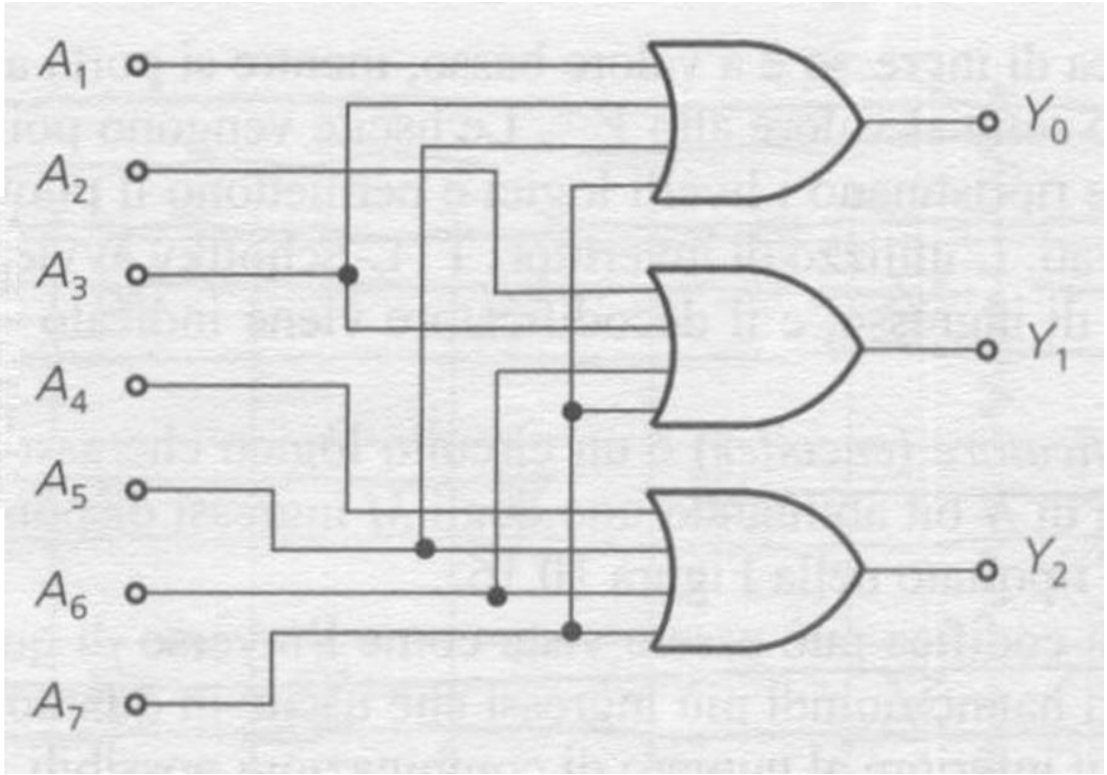
Encoders

Tabella 10.2 Tabella della verità per il codificatore 8-3.

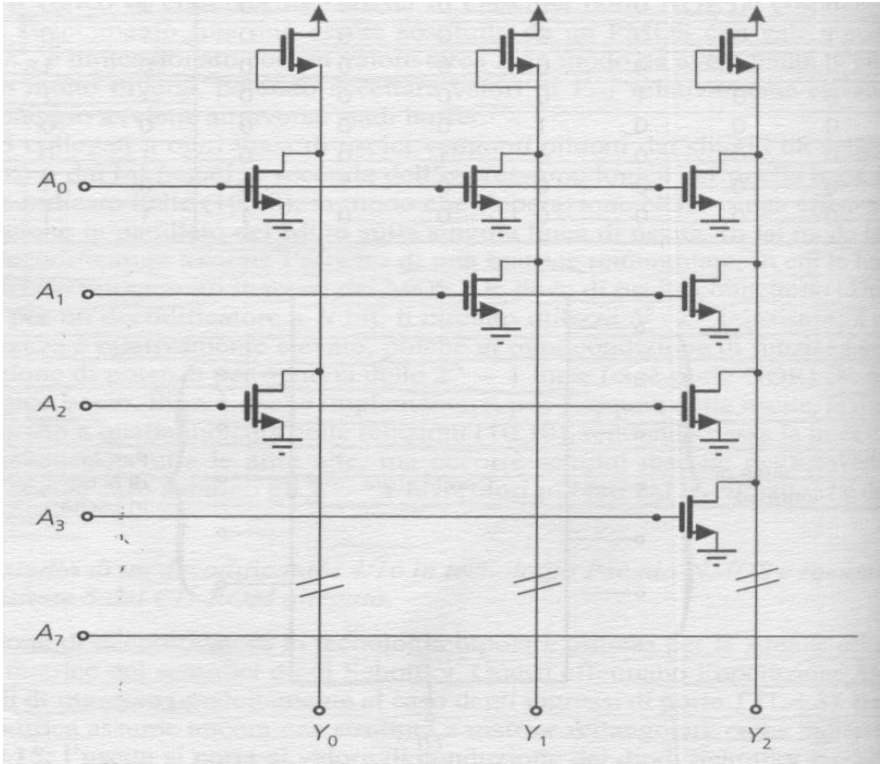
Ingressi								Uscite		
A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Y_0	Y_1	Y_2
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	1	1	0
0	0	0	0	1	0	0	0	0	0	1
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	0	1	1
0	0	0	0	0	0	0	1	1	1	1

Encoders

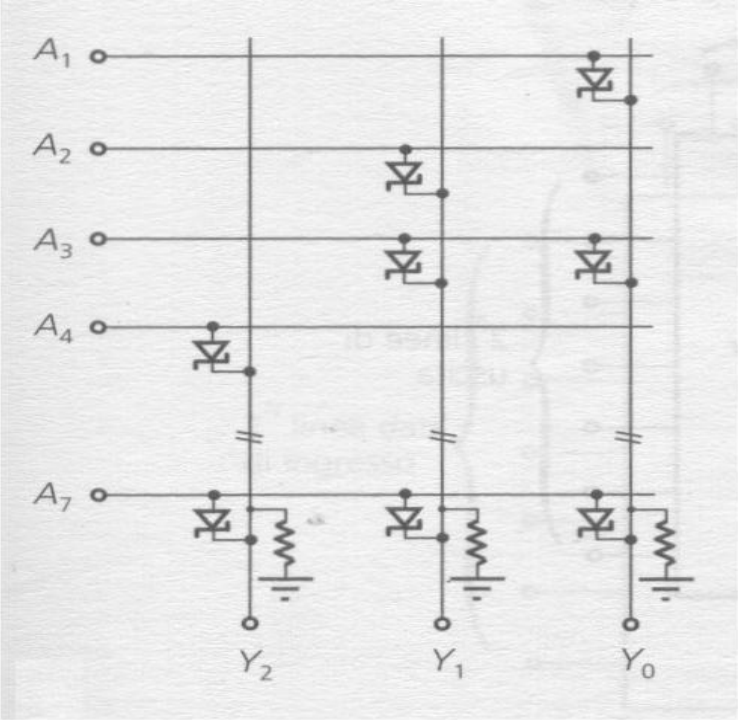
$$Y_0 = A_1 + A_3 + A_5 + A_7$$
$$Y_1 = A_2 + A_3 + A_6 + A_7$$
$$Y_2 = A_4 + A_5 + A_6 + A_7$$



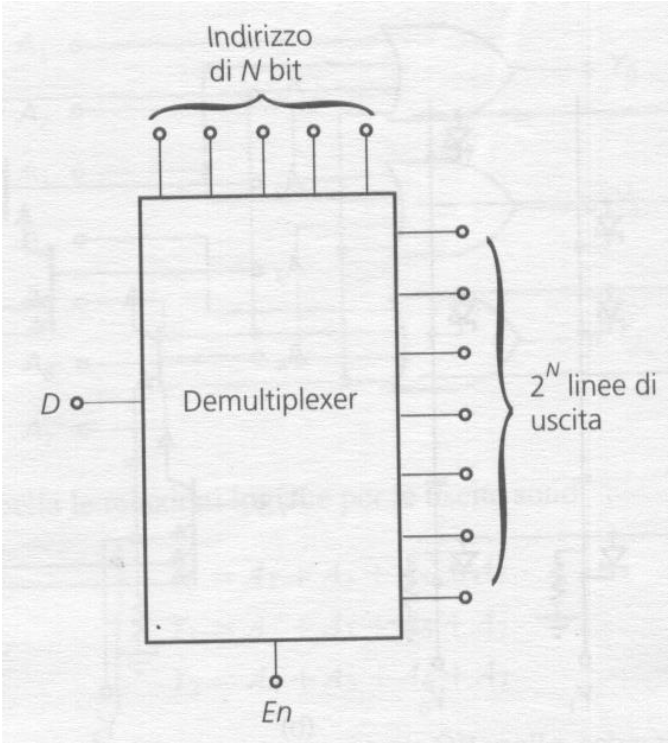
Encoders



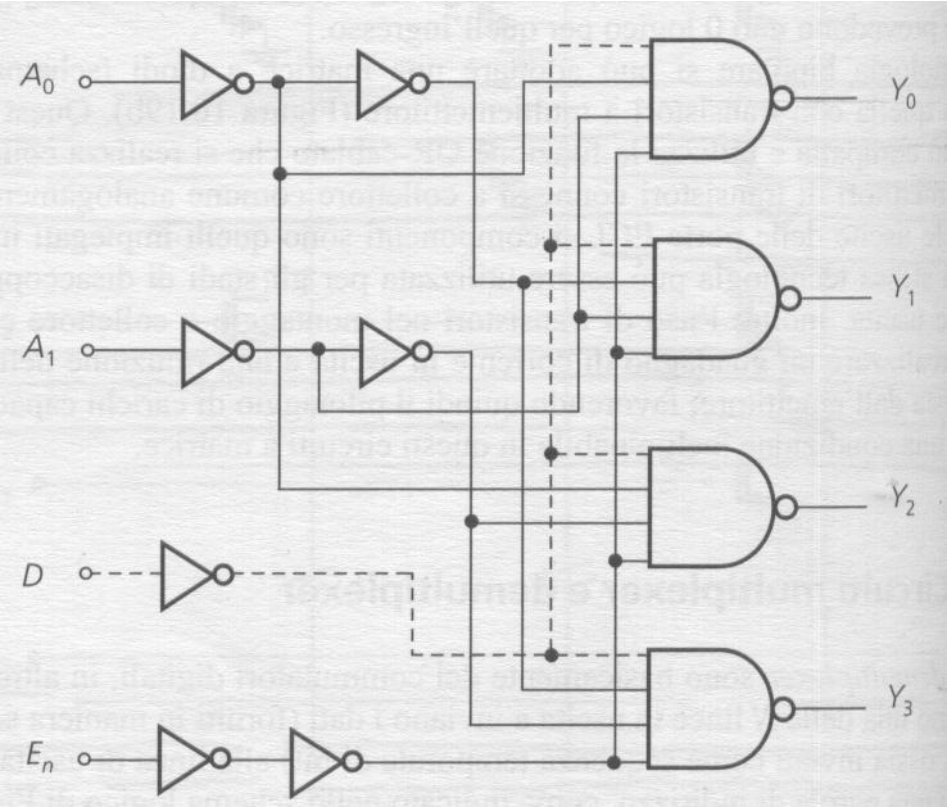
Encoders



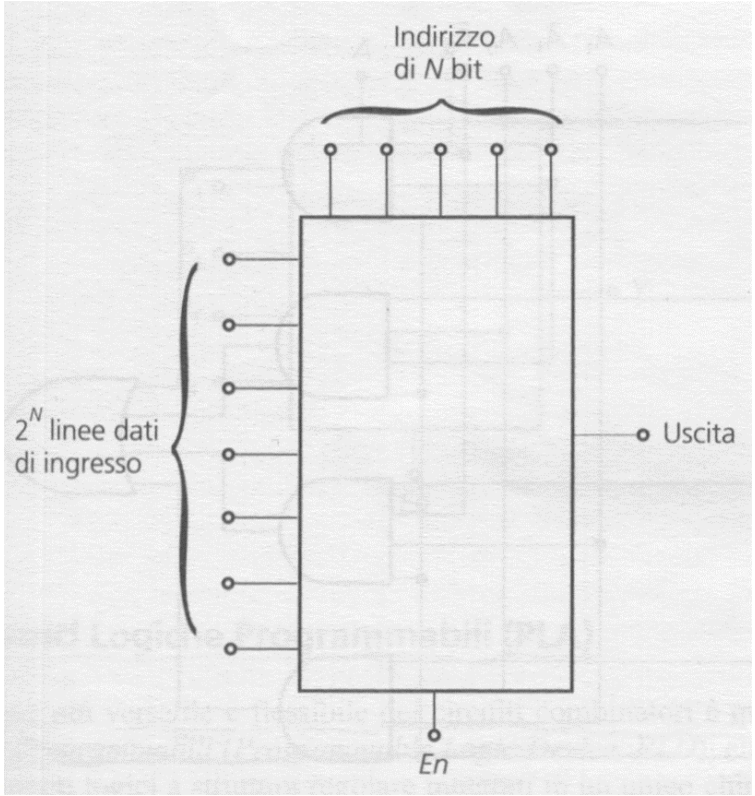
Demultiplexer



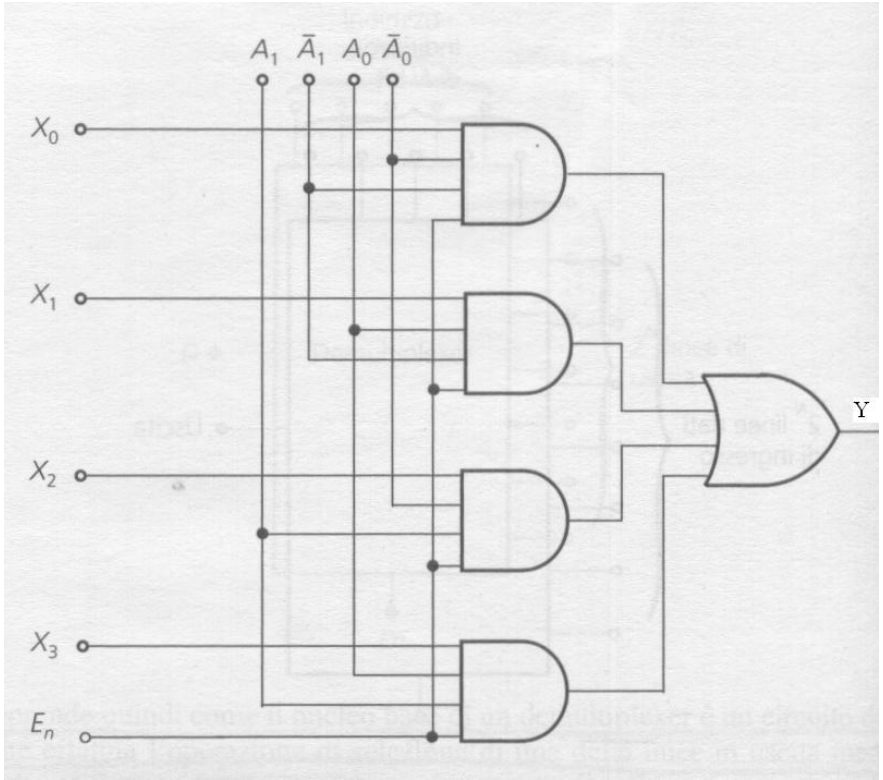
Demultiplexer



Multiplexer



Multiplexer

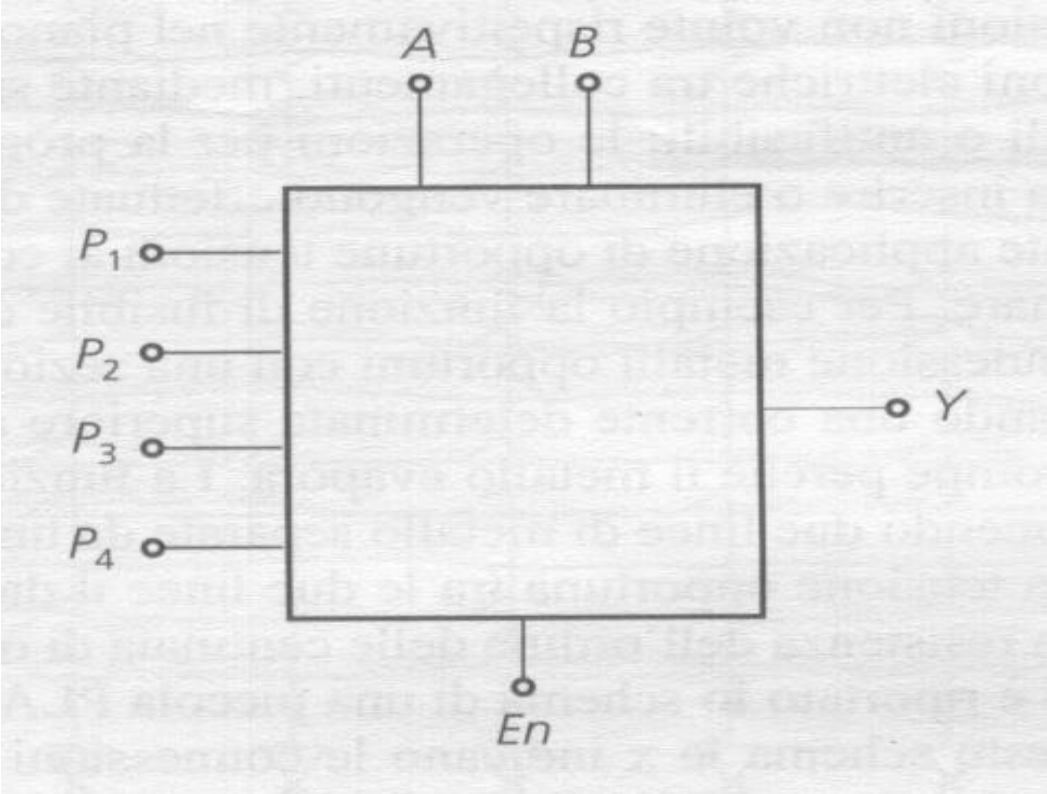


Logic element

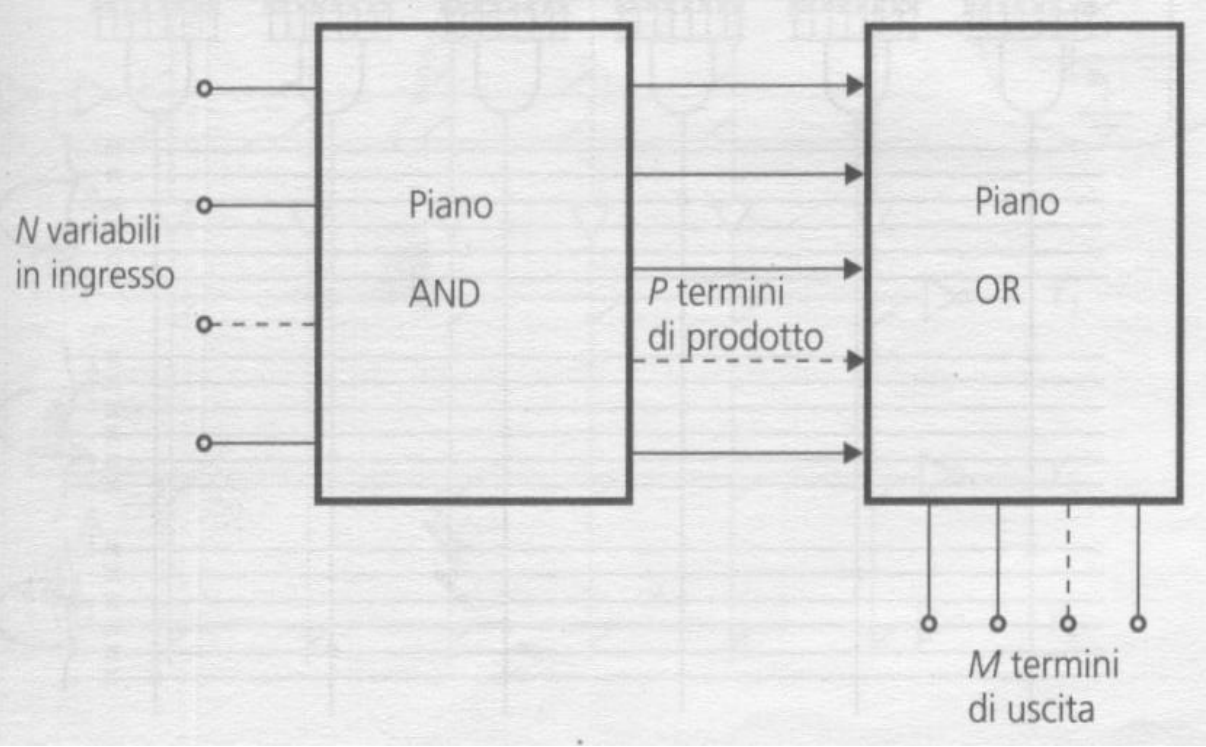
Tabella 10.3 Funzioni logiche implementabili nell'Unità Logica Booleana.

Y	P_1	P_2	P_3	P_4
OR (A, B)	1	1	1	0
NOR (A, B)	0	0	0	1
AND (A, B)	1	0	0	0
NAND (A, B)	0	1	1	1
XOR (A, B)	0	1	1	0
XNOR (A, B)	1	0	0	1

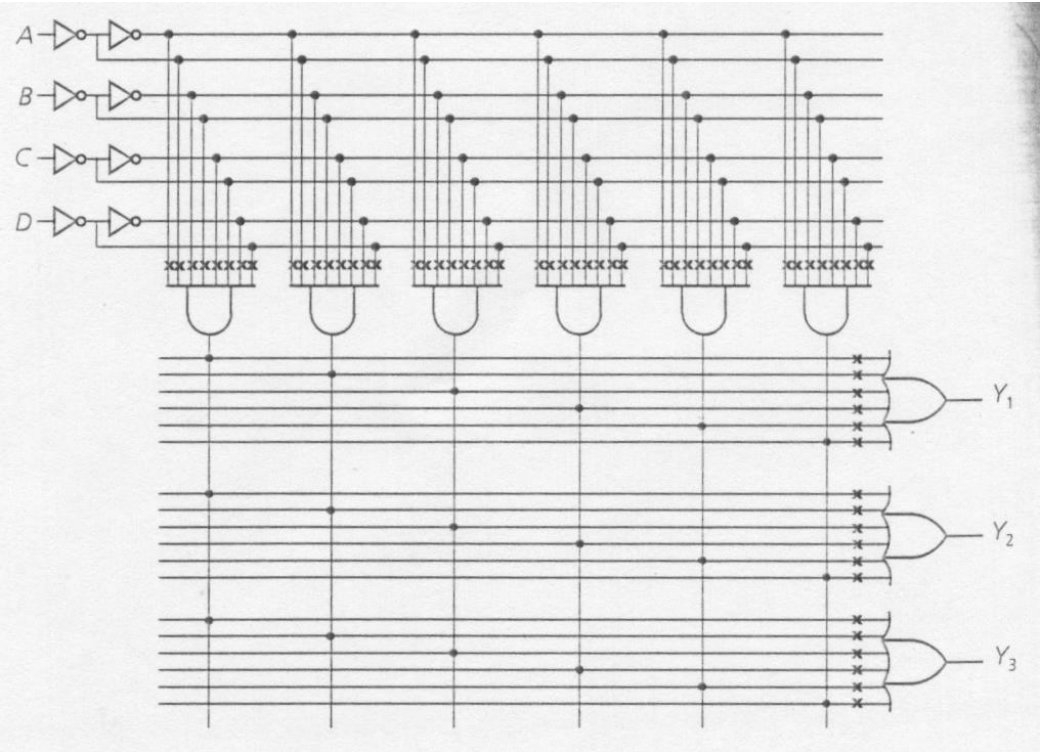
Logic element



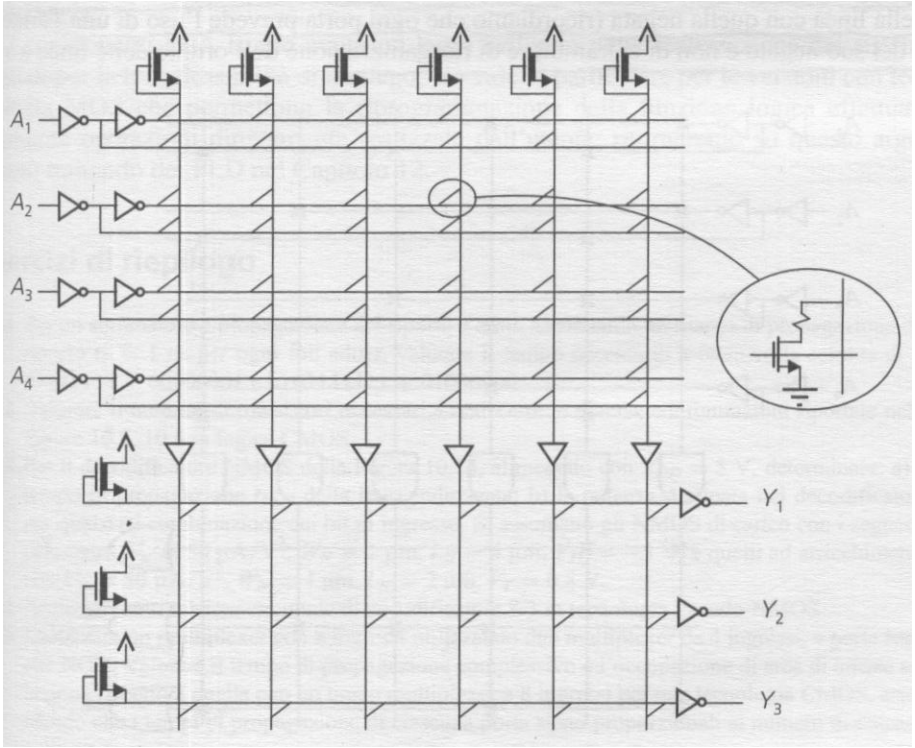
Programmable logic array (PLA)



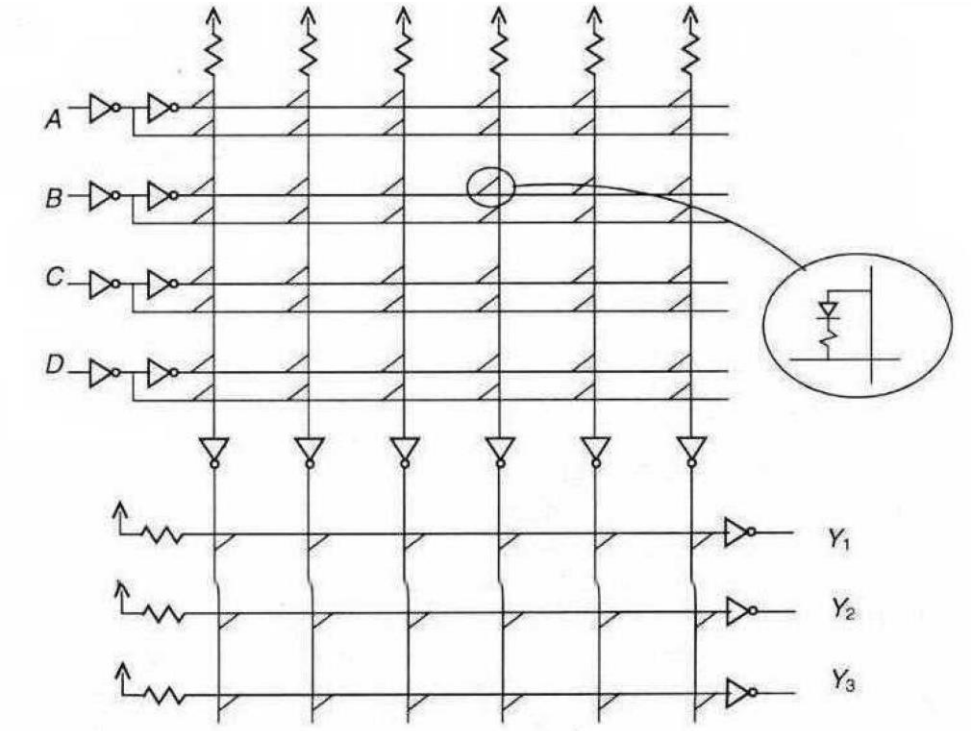
Programmable logic array (PLA)



Programmable logic array (PLA)



Programmable logic array (PLA)



Vedere:

- Paolo Spirito, “Elettronica Digitale”, Ed. McGraw-Hill
  - Cap. 10.09-10.10