15. Analyzing and Optimizing the Design Floorplan with the Chip Planner

QII52006-13.1.0

As FPGA designs grow larger in density, the ability to analyze the design for performance, routing congestion, and logic placement to meet the design requirements becomes critical. This chapter discusses how to analyze the design floorplan with the Chip Planner.

Design floorplan analysis is a valuable method for achieving timing closure and optimal performance in highly complex designs. With analysis capability, the Quartus II Chip Planner helps you close timing quickly on your designs. Using the Chip Planner together with LogicLock and Incremental Compilation enables you to compile your designs hierarchically, preserving the timing results from individual compilation runs. You can use LogicLock regions as part of an incremental compilation methodology to improve your productivity.

You can perform design analysis, as well as creating and optimizing the design floorplan with the Chip Planner. To make I/O assignments, use the Pin Planner.

For information about the Pin Planner, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

You can use the Design Partition Planner with the Chip Planner to customize the floorplan of your design. For more information, refer to the *Quartus II Incremental Compilation for Hierarchical and Team-Based Design* and the *Best Practices for Incremental Compilation Partitions and Floorplan Assignments* chapters in volume 1 of the *Quartus II Handbook*.

This chapter includes the following topics:

For a list of devices supported by the Chip Planner, refer to *About the Chip Planner* in *Quartus II Help*.

For more information about the Chip Planner, refer to the Altera Training page of the Altera website.

Chip Planner Overview

The Chip Planner provides a visual display of chip resources. The Chip Planner can show logic placement, LogicLock regions, relative resource usage, detailed routing information, fan-in and fan-out connections between nodes, timing paths between registers, delay estimates for paths, and routing congestion information.

You can also make assignment changes with the Chip Planner, such as creating and deleting resource assignments, and you can perform post-compilation changes such as creating, moving, and deleting logic cells and I/O atoms. With the Chip Planner, you can view and create assignments for a design floorplan, perform power and design analyses, and implement ECOs. With the Chip Planner and Resource Property Editor, you can change connections between resources and make post-compilation changes to the properties of logic cells, I/O elements, PLLs, and RAM and digital signal processing (DSP) blocks.

For details about how to implement ECOs in your design using the Chip Planner in the Quartus II software, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

Starting the Chip Planner

To start the Chip Planner, on the Tools menu, click **Chip Planner (Floorplan & Chip Editor)**. You can also start the Chip Planner by the following methods:

- Click the Chip Planner icon on the Quartus II software toolbar
- On the Shortcut menu in the following tools, click **Locate** and then click **Locate in Chip Planner (Floorplan and Chip Editor)**:
  - Design Partition Planner
  - Compilation Report
  - LogicLock Regions window
  - Technology Map Viewer
  - Project Navigator window
  - RTL source code
  - Node Finder
  - Simulation Report
  - RTL Viewer
  - Report Timing panel of the TimeQuest Timing Analyzer

Chip Planner Toolbar

The Chip Planner provides powerful tools for design analysis with a GUI. You can access Chip Planner commands from the View menu and the Shortcut menu, or by clicking the icons on the toolbar.

Chip Planner Presets, Layers, and Editing Modes

The Chip Planner models types of resource objects as unique display layers, and uses presets— which are predefined sets of layer settings—to control the display of resources. The Chip Planner provides a set of default presets, and you can create custom presets to customize the display for your particular needs. The Basic, Detailed, and Floorplan Editing presets provided with the Chip Planner are useful for general ECO and assignment-related activities, while the Design Partition Planner preset is optimized for specific activities.

The Chip Planner has two editing modes, which determine the types of operations that you can perform. The Assignment editing mode allows you to make assignment changes that are applied by the Fitter during the next place and route operation. The ECO editing mode allows you to make post-compilation changes, commonly referred to as engineering change orders (ECOs).

You should choose the editing mode appropriate for the work that you want to perform, and a preset that displays the resources that you want to view, in a level of detail appropriate for your design.

Locate History Window

As you optimize your design floorplan, you might have to locate a path or node in the Chip Planner many times. The Locate History window lists all the nodes and paths you have displayed using a **Locate in Chip Planner (Floorplan and Chip Editor)** command, providing easy access to the nodes and paths of interest to you. If you locate a required path from the TimeQuest Timing Analyzer Report Timing pane, the Locate History window displays the required clock path. If you locate an arrival path from the TimeQuest Timing Analyzer Report Timing pane, the Locate History window displays the path from the arrival clock to the arrival data. Double-clicking a node or path in the Locate History window displays the selected node or path in the Chip Planner.

For more information about the Chip Planner, refer to *About the Chip Planner* and *Layers Settings Dialog Box* in Quartus II Help. For more information about the **ECO** editing mode, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

LogicLock Regions

LogicLock regions are floorplan location constraints that help you place logic on the target device. When you assign entity instances or nodes to a LogicLock region, you direct the Fitter to place those entity instances or nodes within the region during fitting. Your floorplan can contain several LogicLock regions.

A LogicLock region is defined by its height, width, and location; you can specify the size or location of a region, or both, or the Quartus II software can generate these properties automatically. The Quartus II software bases the size and location of a region on the contents of the region and the timing requirements of the module. Table 15–1 describes the options for creating LogicLock regions.

Table 15–1. Types of LogicLock Regions

Property	Value	Behavior
State	Floating (1), Locked	Floating allows the Quartus II software to determine the location of the region on the device. Floating regions are shown with a dashed boundary in the floorplan. Locked allows you to specify the location of the region. Locked regions are shown with a solid boundary in the floorplan. A locked region must have a fixed size.
Size	Auto (1), Fixed	Auto allows the Quartus II software to determine the appropriate size of a region given its contents. Fixed regions have a shape and size that you define.
Reserved	Off (1), On	Allows you to define whether the Fitter can use the resources within a region for entities that are not assigned to the region. If the reserved property is turned on, only items assigned to the region can be placed within its boundaries.
Origin	Any Floorplan Location	Specifies the location of the LogicLock region on the floorplan. For Arria series, Stratix series, Cyclone series, MAX II, and MAX V devices, the origin is located at the lower left corner of the LogicLock region. For other Altera® device families, the origin is located at the upper left corner of the LogicLock region.

Note to Table 15–1:
(1) Default value.

The Quartus II software cannot automatically define the size of a region if the location is locked. Therefore, if you want to specify the exact location of the region, you must also specify the size.

You can use the Design Partition Planner in conjunction with LogicLock regions to create a floorplan for your design. For more information about using the Design Partition Planner, refer to the *Quartus II Incremental Compilation for Hierarchical and Team-Based Designs* and the *Best Practices for Incremental Compilation Partition and Floorplan Assignments* chapters in volume 1 of the *Quartus II Handbook*.

Creating LogicLock Regions

You can create LogicLock Regions with the Project Navigator, the LogicLock Regions window, the Design Partition Planner, the Chip Planner, and with Tcl commands.

Creating LogicLock Regions with the Project Navigator

After you perform either a full compilation or analysis and elaboration on the design, the Quartus II software displays the hierarchy of the design. On the View menu, **Utility Windows**, then **Project Navigator.** With the hierarchy of the design fully expanded, right-click on any design entity in the design, and click **Create New LogicLock Region** to create a LogicLock region and assign the entity to the new region.

Creating LogicLock Regions with the LogicLock Regions window

To create a LogicLock region with the LogicLock Regions window, on the Assignments menu, click **LogicLock Regions Window**. In the LogicLock Regions window, click **<<new>>**.

Creating LogicLock Regions with the Design Partition Planner

To create a LogicLock region and assign a partition to it with the Design Partition Planner, right-click the partition and then click **Create LogicLock Region**.

Creating LogicLock Regions with the Chip Planner

To create a LogicLock region in the Chip Planner, click **LogicLock Regions** then **Create LogicLock Region** command on the View menu, then click and drag on the Chip Planner floorplan to create a region of your preferred location and size.

Creating Nonrectangular LogicLock Regions

When you create a floorplan for your design, you may want to create nonrectangular LogicLock regions to exclude certain resources from the LogicLock region. You might also create a nonrectangular LogicLock region to place certain parts of your design around specific device resources to improve performance.

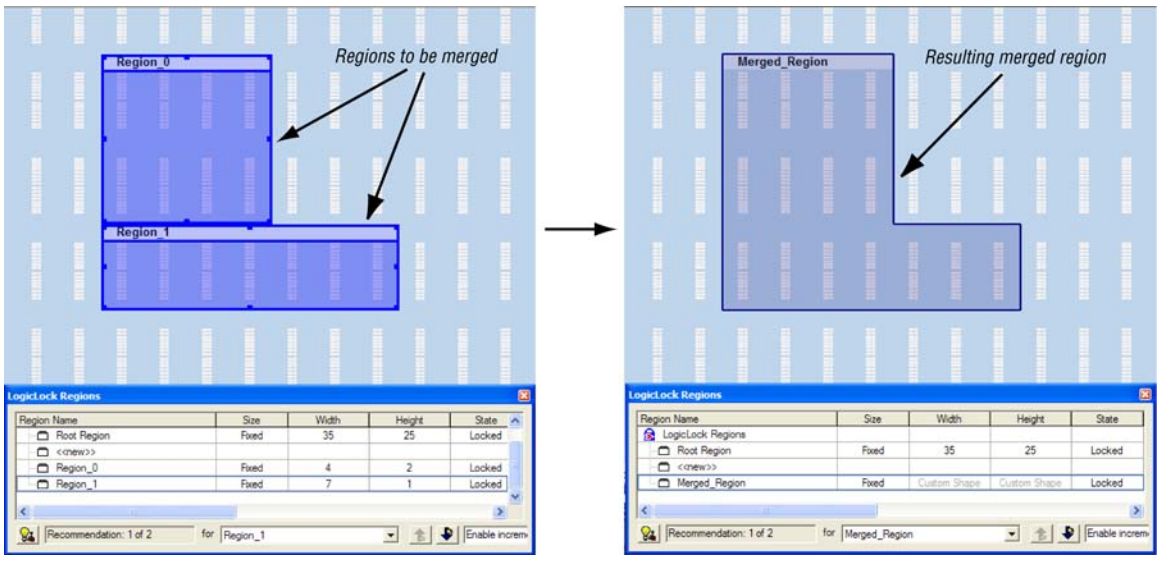
To create a nonrectangular region with the **Merge LogicLock Region** command, follow these steps:

1. In the Chip Planner, create two or more contiguous or non-contiguous rectangular regions as described in "Creating LogicLock Regions" on page 15–4.
2. Arrange the regions that you have created into the locations where you want the nonrectangular region to be.
3. Select all the individual regions that you want to merge by clicking each of them while pressing the Shift key.
4. Right-click the title bar of any of the LogicLock regions that you want to merge, point to **LogicLock Regions**, and then click **Merge LogicLock Region**. The individual regions that you select merge to create a single new region.

By default, the new LogicLock region has the same name as the component region containing the greatest number of resources; however, you can rename the new region. In the **LogicLock Regions Window**, the new region is shown as having a **Custom Shape**.

Figure 15–1 illustrates using the **Merge LogicLock Region** command to form a nonrectangular LogicLock region by merging two rectangular LogicLock regions.

Figure 15–1. Using the Merge LogicLock Region command to create a nonrectangular region



Hierarchical (Parent and Child) LogicLock Regions

To further constrain module locations, you can define a hierarchy for a group of regions by declaring parent and child regions. The Quartus II software places a child region completely within the boundaries of its parent region; a child region must be placed entirely within the boundary of its parent. Additionally, parent and child regions allow you to further improve the performance of a module by constraining nodes in the critical path of a module.

To make one LogicLock region a child of another LogicLock region, in the LogicLock Regions window, select the new child region and drag and drop the new child region into its new parent region.

The LogicLock region hierarchy does not have to be the same as the design hierarchy.

You can create both auto-sized and fixed-sized LogicLock regions within a parent LogicLock region; however, the parent of a fixed-sized child region must also be fixed-sized. The location of a locked parent region is locked relative to the device; the location of a locked child region is locked relative to its parent region. If you change the parent's location, the locked child's origin changes, but maintains the same placement relative to the origin of its parent. The location of a floating child region can float within its parent. Complex region hierarchies might result in some LABs not being used, effectively increasing the resource utilization in the device. Do not create more levels of hierarchy than you need.

Placing LogicLock Regions

A fixed region must contain all resources required by the design block assigned to the region. Although the Quartus II software can automatically place and size LogicLock regions to meet resource and timing requirements, you can manually place and size regions to meet your design requirements. You should consider the following if you manually place or size a LogicLock region:

- LogicLock regions with pin assignments must be placed on the periphery of the device, adjacent to the pins. For the Arria series, Cyclone series, MAX II, MAX V, and Stratix series of devices, you must also include the I/O block within the LogicLock Region.
- Floating LogicLock regions can overlap with their ancestors or descendants, but not with other floating LogicLock regions.

Placing Device Resources into LogicLock Regions

A LogicLock region includes all device resources within its boundaries, including memory and pins. The Quartus II software does not include pins automatically when you assign an entity to a region—you can manually assign pins to LogicLock regions; however, this placement puts location constraints on the region. The software only obeys pin assignments to locked regions that border the periphery of the device. For the Arria series, Cyclone series, MAX II, MAX V, and Stratix series of devices, the locked regions must include the I/O pins as resources.

Pin assignments to LogicLock regions are effective only in fixed and locked regions. Pin assignments to floating regions do not influence the placement of the region.

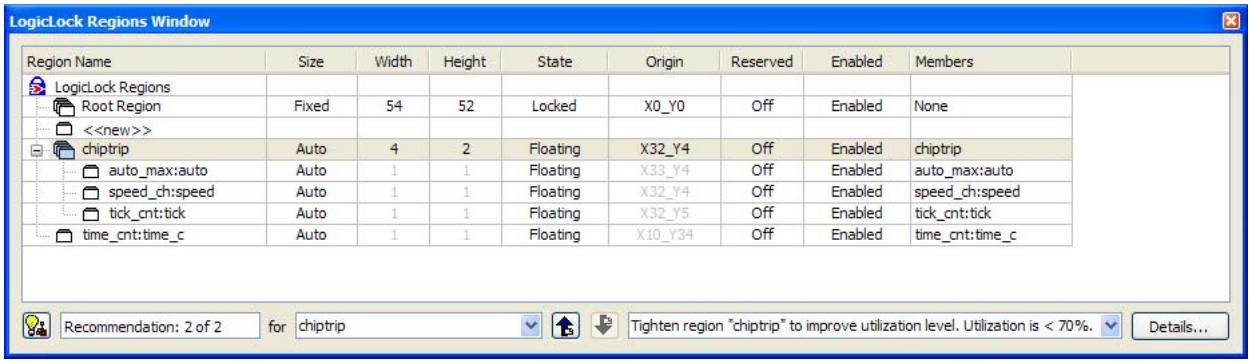
Only one LogicLock region can claim a device resource. If a LogicLock region boundary includes part of a device resource, the Quartus II software allocates the entire resource to that LogicLock region. When the Quartus II software places a floating auto-sized region, it places the region in an area that meets the requirements of the contents of the LogicLock region.

If you want to import multiple instances of a module into a top-level design, you must ensure that the device has two or more locations with exactly the same device resources. (You can determine this from the applicable device handbook.) If the device does not have another area with exactly the same resources, the Quartus II software generates a fitting error during compilation of the top-level design.

LogicLock Regions Window

You can use the LogicLock Regions window to create LogicLock regions, assign nodes and entities to them, and modify the properties of a LogicLock region such as size, state, width, height, origin, and whether the region is a reserved region. The LogicLock Regions window also has a recommendations toolbar; select a LogicLock region from the drop-down list in the recommendations toolbar to display the relevant suggestions to optimize that LogicLock region. You can customize the LogicLock Regions window by dragging and dropping the columns to change their order; you can also show and hide optional columns by right-clicking any column heading and then selecting the appropriate columns in the shortcut menu.

Figure 15–2. LogicLock Regions Window



The **LogicLock Region Properties** dialog box provides a summary of all LogicLock regions in your design. Use the **LogicLock Region Properties** dialog box to obtain detailed information about your LogicLock region, such as which entities and nodes are assigned to your region and which resources are required. The **LogicLock Region Properties** dialog box shows the properties of the current selected regions and allows you to modify them. To open the **LogicLock Region Properties** dialog box, double-click any region in the LogicLock Regions window, or right-click the region and click **Properties**.

For designs that target Arria series, Cyclone series, Stratix series, MAX II, and MAX V devices, the Quartus II software automatically creates a LogicLock region that encompasses the entire device. This default region is labelled `Root_Region`, and is locked and fixed.

For Arria series, Cyclone series, Stratix series, MAX II, and MAX V devices, the origin of the LogicLock region is located at the lower-left corner of the region. For all other supported devices, the origin is located at the upper-left corner of the region.

Reserved LogicLock Region

The Quartus II software honors all entity and node assignments to LogicLock regions. Occasionally, entities and nodes do not occupy an entire region, which leaves some of the region's resources unoccupied. To increase the region's resource utilization and performance, the Quartus II software's default behavior fills the unoccupied resources with other nodes and entities that have not been assigned to another region. You can prevent this behavior by turning on **Reserved** on the **General** tab of the **LogicLock Region Properties** dialog box. When you turn on this option, your LogicLock region contains only the entities and nodes that you specifically assigned to your LogicLock region.

Excluded Resources

The Excluded Resources feature allows you to easily exclude specific device resources such as DSP blocks or M4K memory blocks from a LogicLock region. For example, you can assign a specific entity to a LogicLock region but allow the DSP blocks of that entity to be placed anywhere on the device. Use the Excluded Resources feature on a per-LogicLock region member basis.

To exclude certain device resources from an entity, in the **LogicLock Region Properties** dialog box, highlight the entity in the **Design Element** column, and click **Edit**. In the **Edit Node** dialog box, under **Excluded Element Types**, click the **Browse** button. In the **Excluded Resources Element Types** dialog box, you can select the device resources you want to exclude from the entity. When you have selected the resources to exclude, the **Excluded Resources** column is updated in the **LogicLock Region Properties** dialog box to reflect the excluded resources.

The Excluded Resources feature prevents certain resource types from being included in a region, but it does not prevent the resources from being placed inside the region unless you set the region's **Reserved** property to **On**. To indicate to the Fitter that certain resources are not required inside a LogicLock region, define a resource filter. For more information about resource filters, refer to "LogicLock Resource Exclusions" in the *Best Practices for Incremental Compilation Partitions and Floorplan Assignments* chapter in volume 1 of the *Quartus II Handbook*.

Additional Quartus II LogicLock Design Features

To complement the **LogicLock Regions** window, the Quartus II software has additional features to help you design with LogicLock regions.

Analysis and Synthesis Resource Utilization by Entity

The Compilation Report contains an **Analysis and Synthesis Resource Utilization by Entity** section, which reports resource usage statistics, including entity-level information. You can use this feature to verify that any LogicLock region you manually create contains enough resources to accommodate all the entities you assign to it.

Quartus II Revisions Feature

When you evaluate different LogicLock regions in your design, you might want to experiment with different configurations to achieve your desired results. The Quartus II Revisions feature allows you to organize the same project with different settings until you find an optimum configuration.

To use the Revisions feature, on the Project menu, click **Revisions**. In the **Revisions** dialog box, you can create and specify revisions. You can create a revision from the current design or any previously created revisions. Each revision can have an associated description. You can use revisions to organize the placement constraints created for your LogicLock regions.

LogicLock Assignment Precedence

You can encounter conflicts during the assignment of entities and nodes to LogicLock regions. For example, an entire top-level entity might be assigned to one region and a node within this top-level entity assigned to another region. To resolve conflicting assignments, the Quartus II software maintains an order of precedence for LogicLock assignments. The following order of precedence, from highest to lowest, applies:

1. Exact node-level assignments
2. Path-based and wildcard assignments
3. Hierarchical assignments

For more information about LogicLock assignment precedence, refer to *Understanding Assignment Priority* in Quartus II Help.

Open the **Priority** dialog box by selecting **Priority** on the **General** tab of the **LogicLock Regions Properties** dialog box. You can change the priority of path-based and wildcard assignments with the **Up** and **Down** buttons in the **Priority** dialog box. To prioritize assignments between regions, you must select multiple LogicLock regions and then open the **Priority** dialog box from the **LogicLock Regions Properties** dialog box.

Virtual Pins

A virtual pin is an I/O element that is temporarily mapped to a logic element and not to a pin during compilation, and is then implemented as a LUT. Virtual pins should be used only for I/O elements in lower-level design entities that become nodes when imported to the top-level design. You can create virtual pins by assigning the Virtual Pin logic option to an I/O element.

You might use virtual pin assignments when you compile a partial design, because not all the I/Os from a partial design drive chip pins at the top level.

The virtual pin assignment identifies the I/O ports of a design module that are internal nodes in the top-level design. These assignments prevent the number of I/O ports in the lower-level modules from exceeding the total number of available device pins. Every I/O port that you designate as a virtual pin becomes mapped to either a logic cell or an adaptive logic module (ALM), depending on the target device.

The Virtual Pin logic option must be assigned to an input or output pin. If you assign this option to a bidirectional pin, tri-state pin, or registered I/O element, Analysis and Synthesis ignores the assignment. If you assign this option to a tri-state pin, the Fitter inserts an I/O buffer to account for the tri-state logic; therefore, the pin cannot be a virtual pin. You can use multiplexer logic instead of a tri-state pin if you want to continue to use the assigned pin as a virtual pin. Do not use tri-state logic except for signals that connect directly to device I/O pins.

In the top-level design, you connect these virtual pins to an internal node of another module. By making assignments to virtual pins, you can place those pins in the same location or region on the device as that of the corresponding internal nodes in the top-level module. You can use the **Virtual Pin** option when compiling a LogicLock module with more pins than the target device allows. The **Virtual Pin** option can enable timing analysis of a design module that more closely matches the performance of the module after you integrate it into the top-level design.

In the Node Finder, you can set **Filter Type** to **Pins: Virtual** to display all assigned virtual pins in the design. Alternatively, to access the Node Finder from the Assignment Editor, double-click the **To** field; when the arrow appears on the right side of the field, click the arrow and select **Node Finder**.

Using LogicLock Regions in the Chip Planner

You can easily create LogicLock regions in the Chip Planner and assign resources to them.

Viewing Connections Between LogicLock Regions in the Chip Planner

You can view and edit LogicLock regions using the Chip Planner. To view and edit LogicLock regions, select the **Floorplan Editing** mode in **Layers Settings**, or any Layers setting mode that has the **User-assigned LogicLock regions** setting enabled.

The Chip Planner shows the connections between LogicLock regions. By default, you can view each connection as an individual line. You can choose to display connections between two LogicLock regions as a single bundled connection rather than as individual connection lines. To use this option, open the Chip Planner and on the View menu, click **Inter-region Bundles**.

For more information about the **Inter-region Bundles** dialog box, refer to *Inter-region Bundles Dialog Box* in Quartus II Help.

Using LogicLock Regions with the Design Partition Planner

You can optimize timing in a design by placing entities that share significant logical connectivity close to each other on the device. By default, the Fitter usually places closely connected entities in the same area of the device; however, you can use LogicLock regions, together with the Design Partition Planner and the Chip Planner, to help ensure that logically connected entities retain optimal placement from one compilation to the next.

You can view the logical connectivity between entities with the Design Partition Planner, and the physical placement of those entities with the Chip Planner. In the Design Partition Planner, you can identify entities that are highly interconnected, and place those entities in a partition. In the Chip Planner, you can create LogicLock regions and assign each partition to a LogicLock region, thereby preserving the placement of the entities.

For more information about using LogicLock regions with design partitions, refer to the *Quartus II Incremental Compilation for Hierarchical and Team-Based Design* and the *Best Practices for Incremental Compilation Partition and Floorplan Assignments* chapters in volume 1 of the *Quartus II Handbook*. For more information about using the Design Partition Planner with the Chip Planner, refer to *About the Design Partition Planner* and *Using the Design Partition Planner* in Quartus II Help.

Design Floorplan Analysis Using the Chip Planner

The Chip Planner helps you visually analyze the floorplan of your design at any stage of your design cycle. With the Chip Planner, you can view post-compilation placement, connections, and routing paths. You can also create LogicLock regions and location assignments. The Chip Planner allows you to create new logic cells and I/O atoms and to move existing logic cells and I/O atoms in your design. You can also see global and regional clock regions within the device, and the connections between I/O atoms, PLLs and the different clock regions.

From the Chip Planner, you can launch the Resource Property Editor, which you can use to change the properties and parameters of device resources, and modify connectivity between certain types of device resources. The Change Manager records any changes that you make to your design floorplan so that you can selectively undo changes if necessary.

For more information about the Resource Property Editor and the Change Manager, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*, and to *About the Resource Property Editor* and *About the Change Manager* in Quartus II Help.

The following sections present Chip Planner floorplan views and design analysis procedures which you can use with any Chip Planner preset, unless a procedure requires a specific preset or editing mode.

Chip Planner Floorplan Views

The Chip Planner uses a hierarchical zoom viewer that shows various abstraction levels of the targeted Altera device. As you zoom in, the level of abstraction decreases, revealing more details about your design.

For more information about Chip Planner floorplan views, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

Bird's Eye View

The Bird's Eye View displays a high-level picture of resource usage for the entire chip and provides a fast and efficient way to navigate between areas of interest in the Chip Planner.

The Bird's Eye View is particularly useful when the parts of your design that you want to view are at opposite ends of the chip and you want to quickly navigate between resource elements without losing your frame of reference.

For more information about the Bird's Eye View, refer to *Bird's Eye View* and *Displaying Resources and Information* in Quartus II Help.

Properties Window

The Properties Window displays detailed properties of the objects (such as atoms, paths, LogicLock regions, or routing elements) currently selected in the Chip Planner. To display the Properties Window, click **Properties** on the **View** menu in the Chip Planner.

Viewing Architecture-Specific Design Information

By adjusting the **Layers Settings** in the Chip Planner, you can view the following architecture-specific information related to your design:

- **Device routing resources used by your design**—View how blocks are connected, as well as the signal routing that connects the blocks.
- **LE configuration**—View logic element (LE) configuration in your design. For example, you can view which LE inputs are used; if the LE utilizes the register, the look-up table (LUT), or both; as well as the signal flow through the LE.
- **ALM configuration**—View ALM configuration in your design. For example, you can view which ALM inputs are used, if the ALM utilizes the registers, the upper LUT, the lower LUT, or all of them. You can also view the signal flow through the ALM.
- **I/O configuration**—View device I/O resource usage. For example, you can view which components of the I/O resources are used, if the delay chain settings are enabled, which I/O standards are set, and the signal flow through the I/O.
- **PLL configuration**—View phase-locked loop (PLL) configuration in your design. For example, you can view which control signals of the PLL are used with the settings for your PLL.
- **Timing**—View the delay between the inputs and outputs of FPGA elements. For example, you can analyze the timing of the `DATAB` input to the `COMBOUT` output.

In addition, you can modify the following device properties with the Chip Planner:

- LEs and ALMs
- I/O cells
- PLLs
- Registers in RAM and DSP blocks
- Connections between elements

- Placement of elements

For more information about LEs, ALMs, and other resources of an FPGA device, refer to the relevant device handbook.

Viewing Available Clock Networks in the Device

When you select a task with clock region layer preset enabled, you can display the areas of the chip that are driven by global and regional clock networks. This global clock display feature is available for Arria GX, Arria II, Arria V, Cyclone II, Cyclone III, Cyclone V, Stratix II, Stratix II GX, Stratix III, Stratix IV, and Stratix V device families.

Depending on the clock layers activated in the selected preset, the Chip Planner displays regional and global clock regions in the device, and the connectivity between clock regions, pins, and PLLs. Clock regions appear as rectangular overlay boxes with labels indicating the clock type and index.You can select each clock network region by clicking on the clock region. The clock-shaped icon at the top-left corner indicates that the region represents a clock network region. You can change the color in which the Chip Planner displays clock regions on the **Options** dialog box of the Tools menu.

The **Layers Settings** dialog box lists layers for different clock region types; when the selected device does not contain a given clock region, the option for that category is unavailable in the dialog box. You can customize the Chip Planner's display of clock regions by creating a custom preset with selected clock layers enabled in the Layers Settings dialog box.

For more information about displaying clock regions, refer to *Displaying Resources and Information* in Quartus II Help.

Viewing Critical Paths

Critical paths are timing paths in your design that have a negative slack. These timing paths can span from device I/Os to internal registers, registers to registers, or from registers to device I/Os. The slack of a path determines its criticality; slack appears in the timing analysis report. Design analysis for timing closure is a fundamental requirement for optimal performance in highly complex designs. The analytical capability of the Chip Planner helps you close timing on complex designs.

Viewing critical paths in the Chip Planner helps you understand why a specific path is failing. You can see if any modification in the placement can reduce the negative slack. You can display details of a path (to expand/collapse the path to/from the connections in the path) by clicking **Expand Connections** in the toolbar, or by clicking on the "+/-" on the label.

You can locate failing paths from the timing report in the TimeQuest Timing Analyzer. To locate the critical paths, run the Report Timing task from the Custom Reports group in the Tasks pane of the TimeQuest Timing Analyzer. From the View pane, which lists the failing paths, right-click on any failing path or node, and select **Locate Path**. From the Locate dialog box, select **Chip Planner** to see the failing path in the Chip Planner.

To display paths in the floorplan, you must first make timing settings and perform a timing analysis.

For more information about performing static timing analysis with the Quartus II TimeQuest Timing Analyzer, refer to *The Quartus II TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

Viewing Routing Congestion

The **Report Routing Utilization** task allows you to determine the percentage of routing resources in use following a compilation. This feature can identify where there is a lack of routing resources, helping you to make design changes to meet routing congestion design requirements.

Open the Chip Planner from the Tools menu. To view the routing congestion in the Chip Planner, double-click the **Report Routing Utilization** command in the **Tasks** list. Click **Preview** in the **Report Routing Utilization** dialog box to preview the default congestion display. Change the **Routing utilization type** to display congestion for specific resources. The default display uses dark blue for 0% congestion (blue indicates zero utilization) and red for 100%. You can adjust the slider for **Threshold percentage** to change the congestion threshold level.

The routing congestion map uses the color and shading of logic resources to indicate relative resource utilization; darker shading represents a greater utilization of routing resources. Areas where routing utilization exceeds the threshold value specified in the **Report Routing Utilization** dialog box appear in red. The congestion map can help you determine whether you can modify the floorplan, or make changes to the RTL to reduce routing congestion.

To identify a lack of routing resources, it is necessary to investigate each routing interconnect type separately by selecting each interconnect type in turn in the **Routing Utilization Settings** dialog box.

The Quartus II compilation messages contain information about average and peak interconnect usage. Peak interconnect usage over 75%, or average interconnect usage over 60%, could be an indication that it might be difficult to fit your design. Similarly, peak interconnect usage over 90%, or average interconnect usage over 75%, are likely to have increased chances of not getting a valid fit.

For more information about displaying routing congestion, refer to *Displaying Resources and Information* in Quartus II Help.

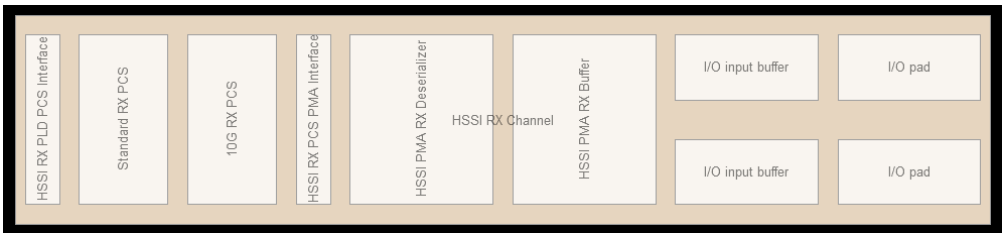
Viewing I/O Banks

The Chip Planner can show all of the I/O banks of the device. To see the I/O bank map of the device, select **Report All I/O Banks** in the Tasks pane.

Viewing High-Speed Serial Interfaces (HSSI)

For the Stratix V device family, the Chip Planner displays a detailed block view of the receiver and transmitter channels of the high-speed serial interfaces. To display the HSSI block view, select **Report HSSI Block Connectivity**. Figure 15–3 shows the blocks of a Stratix V HSSI receiver channel.

Figure 15–3. Stratix V HSSI receiver channel



Generating Fan-In and Fan-Out Connections

The ability to display fan-in and fan-out connections enables you to view the atoms that fan-in to or fan-out from the selected atom. To remove the connections displayed, use the **Clear Unselected Connections** icon in the Chip Planner toolbar.

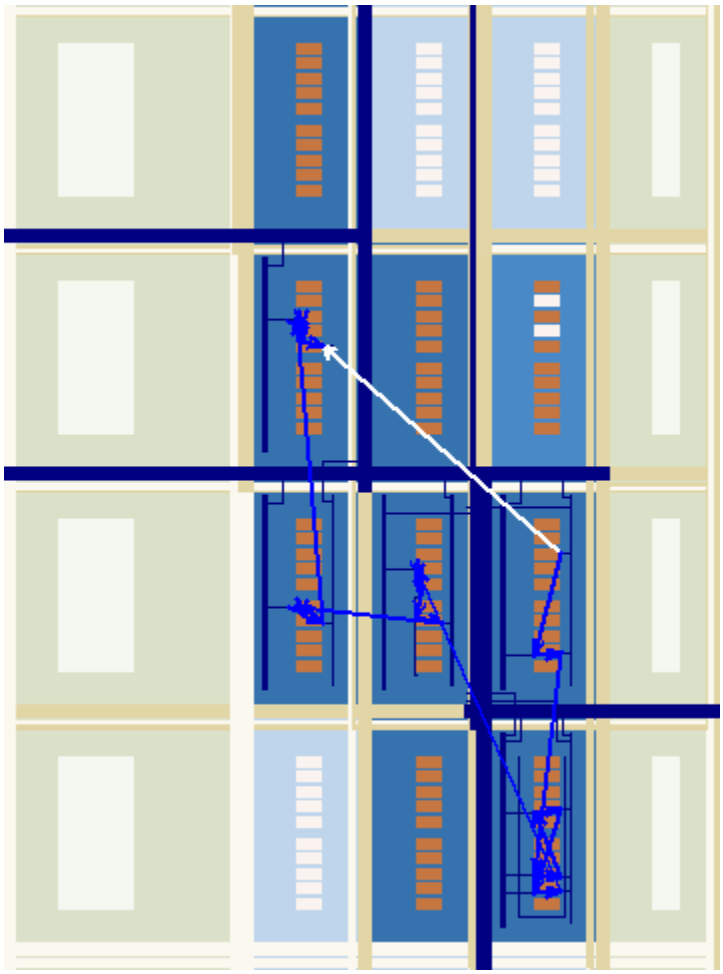
Generating Immediate Fan-In and Fan-Out Connections

The ability to display immediate fan-in and fan-out connections enables you to view the resource that is the immediate fan-in or fan-out connection for the selected atom. For example, if you select a logic resource and choose to view the immediate fan-in for that resource, you can see the routing resource that drives the logic resource. You can generate immediate fan-ins and fan-outs for all logic resources and routing resources. To remove the displayed connections from the screen, click the **Clear Unselected Connections** icon in the toolbar.

Highlight Routing

The **Show Physical Routing** command in the **Locate History** pane enables you to highlight the routing resources used by a selected path or connection. Figure 15–4 shows the routing resources in use between two logic elements.

Figure 15–4. Highlight Routing

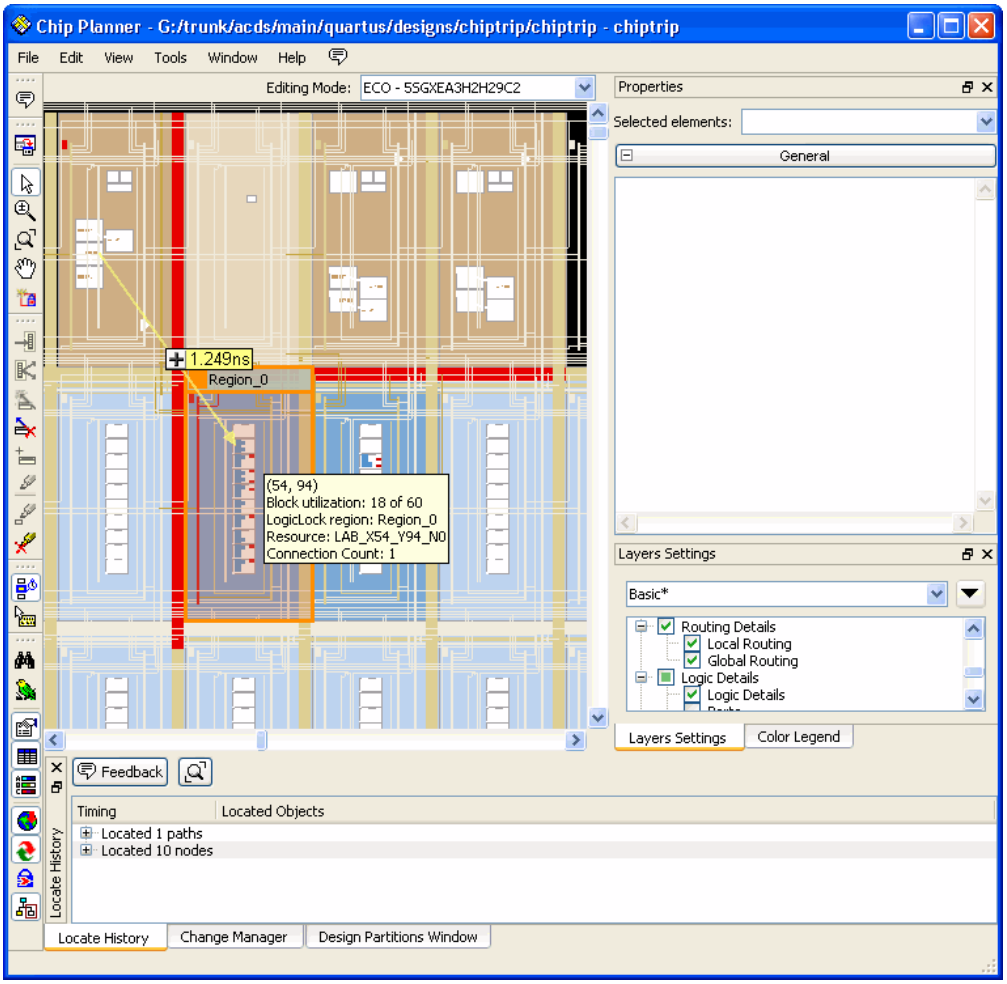


You can view and edit resources in the FPGA using the Resource Property Editor. For more information, refer to the *Engineering Change Management with the Chip Planner* chapter in volume 2 of the *Quartus II Handbook*.

Show Delays

With the Show Delays command, you can view timing delays for paths located from TimeQuest Timing Analyzer reports. For example, you can view the delay between two logic resources or between a logic resource and a routing resource. Figure 15–5 shows the delay associated with a path located from a TimeQuest Timing Analyzer report.

Figure 15–5. Show Delays



Exploring Paths in the Chip Planner

You can use the Chip Planner to explore paths between logic elements. The following example uses the Chip Planner to traverse paths from the Timing Analysis report.

Locate Path from the Timing Analysis Report to the Chip Planner

To locate a path from the Timing Analysis report to the Chip Planner, perform the following steps:

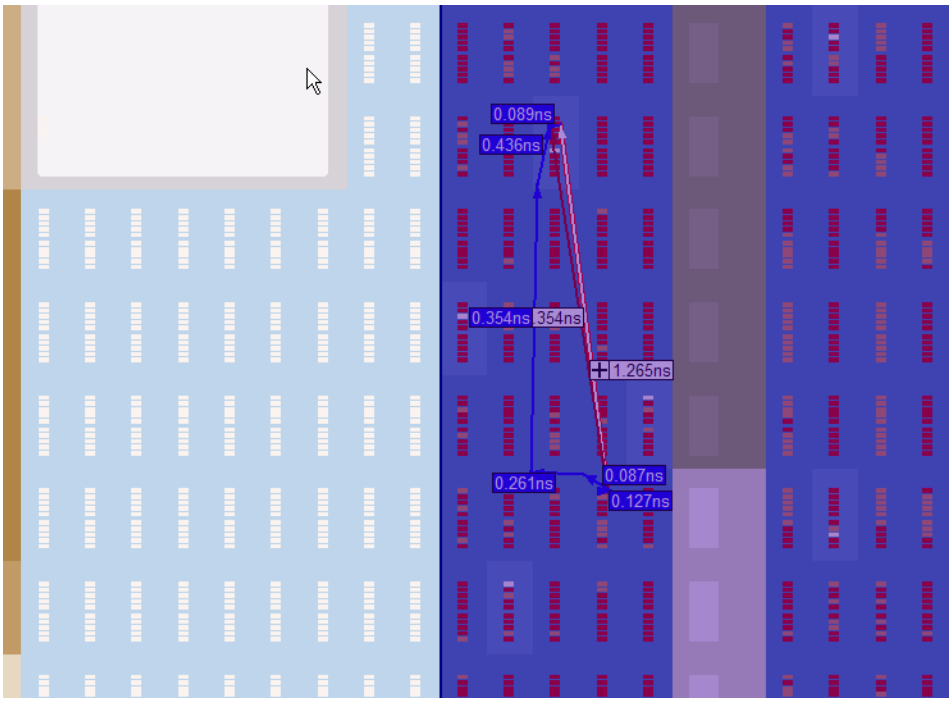
1. Select the path you want to locate.

2. Right-click the path in the Timing Analysis report, point to **Locate Path**, and click **Locate in Chip Planner**. The path is displayed with its timing data in the Chip Planner main window and is listed in the Locate History window.
3. To view the routing resources taken for a path you have located in the Chip Planner, select the path and then click the **Highlight Routing** icon in the Chip Planner toolbar, or from the View menu, click **Highlight Routing**.

Analyzing Connections for a Path

To determine the connections between items in the Chip Planner, click the **Expand Connections** icon on the toolbar. To add the timing delays for paths located from the TimeQuest Timing Analyzer, click the **Show Delays** icon on the toolbar. Figure 15–6 shows the connections for a path located from the TimeQuest Timing Analyzer that are displayed in the Chip Planner. To see the constituent delays on the selected path, click on the "+" sign next to the path delay displayed in the Chip Planner.

Figure 15–6. Path Analysis

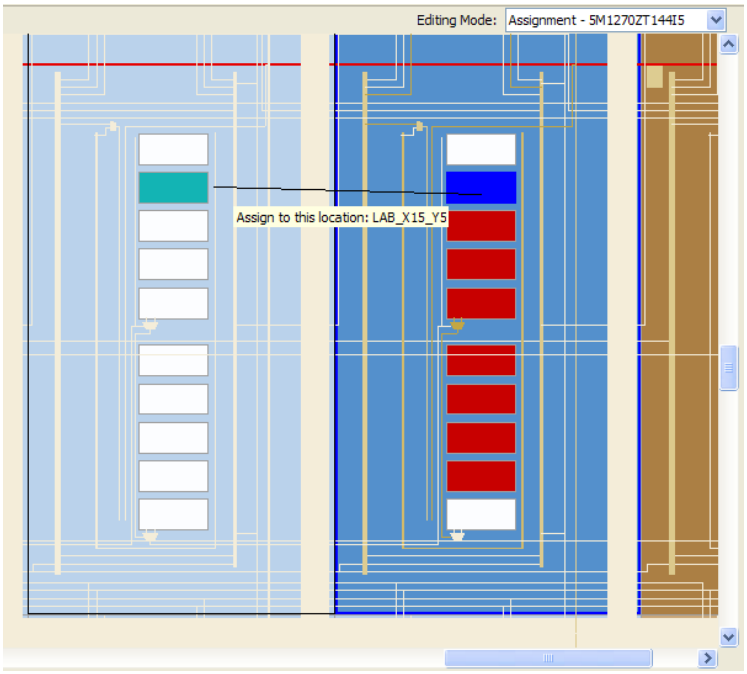


Viewing Assignments in the Chip Planner

You can view location assignments by selecting the appropriate layer set in the Chip Planner. To view location assignments, select the **Floorplan Editing** preset or any custom preset that displays block utilization, and the Assignment editing mode. See Figure 15–7.

The Chip Planner shows location assignments graphically, by displaying assigned resources in a particular color (gray, by default). You can create or move an assignment by dragging the selected resource to a new location.

Figure 15–7. Viewing Assignments in the Chip Planner



You can make node and pin location assignments to LogicLock regions and custom regions using the drag-and-drop method in the Chip Planner. The Fitter applies the assignments that you create during the next place-and-route operation.

For more information about managing assignments in the Chip Planner, refer to *Working With Assignments in the Chip Planner* in Quartus II Help.

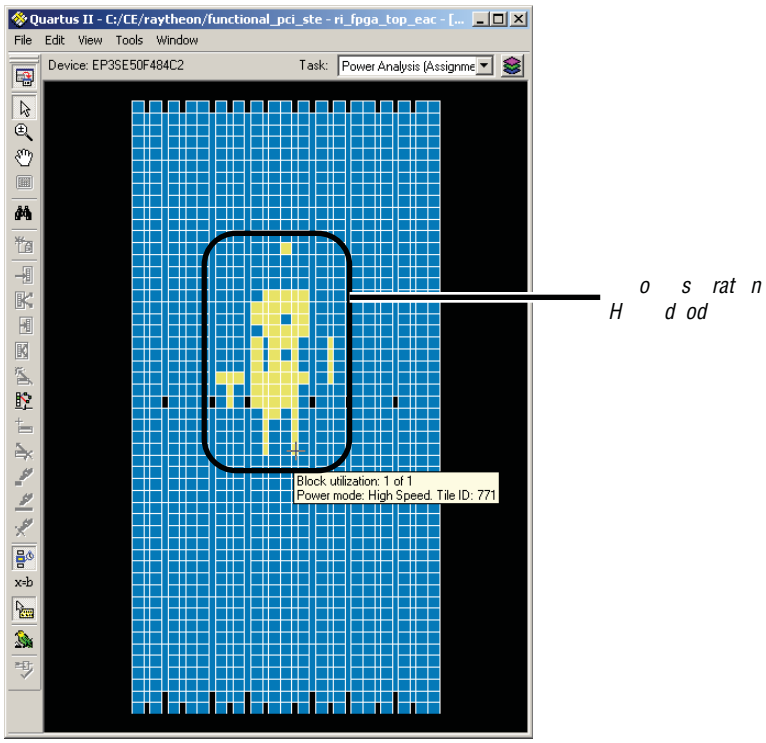
Viewing High-Speed and Low-Power Tiles in the Chip Planner

To view a power map of designs that specify Stratix III, Stratix IV, or Stratix V devices, select the **Report High-Speed/Low-Power Tiles** command in the **Tasks** menu after running the Fitter. Stratix III, Stratix IV, or Stratix V devices have ALMs that can operate in either high-speed mode or low-power mode. The power mode is set during the fitting process in the Quartus II software. These ALMs are grouped together to form larger blocks, called "tiles."

To learn more about power analyses and optimizations in Stratix III devices, refer to *AN 437: Power Optimization in Stratix III FPGAs*. To learn more about power analyses and optimizations in Stratix IV devices, refer to *AN 514: Power Optimization in Stratix IV FPGAs*.

When you select the **Report High-Speed/Low-Power Tiles** command for Stratix III, Stratix IV, or Stratix V devices, the Chip Planner displays low-power and high-speed tiles in contrasting colors; yellow tiles operate in a high-speed mode, while blue tiles operate in a low-power mode (see Figure 15–8). When you select the **Power** task, you can perform all floorplanner-related functions for this task; however, you cannot edit tiles to change the power mode.

Figure 15–8. Viewing High-Speed and Low Power Tiles in a Stratix III Device



Scripting Support

You can run procedures and specify the settings described in this chapter in a Tcl script. You can also run some procedures at a command prompt. For detailed information about scripting command options, refer to the Quartus II command-line and Tcl API Help browser. To run the Help browser, type the following command at the command prompt:

```
quartus_sh --qhelp ↵
```

Information about scripting command options is also available in *API Functions for Tcl* in Quartus II Help.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*. For more information about command-line scripting, refer to the *Command-Line Scripting* chapter in volume 2 of the *Quartus II Handbook*. For information about all settings and constraints in the Quartus II software, refer to the *Quartus II Settings File Manual*.

Initializing and Uninitializing a LogicLock Region

You must initialize the LogicLock data structures before creating or modifying any LogicLock regions and before executing any of the Tcl commands listed below.

Use the following Tcl command to initialize the LogicLock data structures:

```
initialize_logiclock
```

Use the following Tcl command to uninitialize the LogicLock data structures before closing your project:

```
uninitialize_logiclock
```

Creating or Modifying LogicLock Regions

Use the following Tcl command to create or modify a LogicLock region:

```
set_logiclock -auto_size true -floating true -region <my_region-name>
```

The command in the above example sets the size of the region to auto and the state to floating.

If you specify a region name that does not exist in the design, the command creates the region with the specified properties. If you specify the name of an existing region, the command changes all properties you specify and leaves unspecified properties unchanged.

For more information about creating LogicLock regions, refer to "Creating LogicLock Regions" on page 15–4.

Obtaining LogicLock Region Properties

Use the following Tcl command to obtain LogicLock region properties. This example returns the height of the region named `my_region`:

```
get_logiclock -region my_region -height
```

Assigning LogicLock Region Content

Use the following Tcl commands to assign or change nodes and entities in a LogicLock region. This example assigns all nodes with names matching `fifo*` to the region named `my_region`.

```
set_logiclock_contents -region my_region -to fifo*
```

You can also make path-based assignments with the following Tcl command:

```
set_logiclock_contents -region my_region -from fifo -to ram*
```

Save a Node-Level Netlist for the Entire Design into a Persistent Source File

Make the following assignments to cause the Quartus II Fitter to save a node-level netlist for the entire design into a **.vqm** file:

```
set_global_assignment-name LOGICLOCK_INCREMENTAL_COMPILE_ASSIGNMENT ON
set_global_assignment-name LOGICLOCK_INCREMENTAL_COMPILE_FILE <file
name>
```

Any path specified in the file name is relative to the project directory. For example, specifying **atom_netlists/top.vqm** places **top.vqm** in the **atom_netlists** subdirectory of your project directory.

A **.vqm** file is saved in the directory specified at the completion of a full compilation.

The saving of a node-level netlist to a persistent source file is not supported for designs targeting newer devices such as Arria GX, Arria II, Cyclone III, MAX V, Stratix III, Stratix IV, or Stratix V.

Setting LogicLock Assignment Priority

Use the following Tcl code to set the priority for a LogicLock region's members. This example reverses the priorities of the LogicLock region in your design.

```
set reverse [list]
for each member [get_logiclock_member_priority] {
    set reverse [insert $reverse 0 $member]
{
set_logiclock_member_priority $reverse
```

Assigning Virtual Pins

Use the following Tcl command to turn on the virtual pin setting for a pin called `my_pin`:

```
set_instance_assignment -name VIRTUAL_PIN ON -to my_pin
```

For more information about assigning virtual pins, refer to "Virtual Pins" on page 15–10.

For more information about Tcl scripting, refer to the *Tcl Scripting* chapter in volume 2 of the *Quartus II Handbook*.

Document Revision History

Table 15–2 shows the revision history for this chapter.

Table 15–2. Document Revision History (Part 1 of 2)

Date	Version	Changes
November 2013	13.1.0	Removed HardCopy device information.
May 2013	13.0.0	Updated "Viewing Routing Congestion" section Updated references to Quartus UI controls for the Chip Planner
June 2012	12.0.0	Removed survey link.
November 2011	11.0.1	Template update.
May 2011	11.0.0	■ Updated for the 11.0 release. ■ Edited "LogicLock Regions" ■ Updated "Viewing Routing Congestion" ■ Updated "Locate History" ■ Updated Figures 15-4, 15-9, 15-10, and 15-13 ■ Added Figure 15-6

Table 15–2. Document Revision History (Part 2 of 2)

Date	Version	Changes
December 2010	10.1.0	■ Updated for the 10.1 release.
July 2010	10.0.0	■ Updated device support information ■ Removed references to Timing Closure Floorplan; removed "Design Analysis Using the Timing Closure Floorplan" section ■ Added links to online Help topics ■ Added "Using LogicLock Regions with the Design Partition Planner" section ■ Updated "Viewing Critical Paths" section ■ Updated several graphics ■ Updated format of Document revision History table
November 2009	9.1.0	■ Updated supported device information throughout ■ Removed deprecated sections related to the Timing Closure Floorplan for older device families. (For information on using the Timing Closure Floorplan with older device families, refer to previous versions of the *Quartus II Handbook*, available in the Quartus II Handbook Archive.) ■ Updated "Creating Nonrectangular LogicLock Regions" section ■ Added "Selected Elements Window" section ■ Updated table 12-1

May 2008	8.0.0	■ Updated the following sections:
		  ■ "Chip Planner Tasks and Layers"
		  ■ "LogicLock Regions"
		  ■ "Back-Annotating LogicLock Regions"
		  ■ "LogicLock Regions in the Timing Closure Floorplan"
		■ Added the following sections:
		  ■ "Reserve LogicLock Region"
		  ■ "Creating Nonrectangular LogicLock Regions"
		  ■ "Viewing Available Clock Networks in the Device"
		■ Updated Table 10–1
		■ Removed the following sections:
		  ■ Reserve LogicLock Region Design Analysis Using the Timing Closure Floorplan

For previous versions of the *Quartus II Handbook*, refer to the Quartus II Handbook Archive.