White Paper

Using the Assignment Editor in the Quartus II Software

Introduction

As a result of the increasing complexity of today's FPGA designs and the demand for higher performance, designers must make a larger number of complex timing and logic constraints to meet their performance requirements. This complexity is compounded by the increasing density and associated pin counts of current FPGAs. To successfully implement a complex design in the latest generation of FPGAs, designers must make a large number of pin assignments that include the location, I/O standards, and on-chip termination settings.

To make the process of entering these assignments easier, Altera has developed an easy and intuitive, spreadsheet-like interface called the Assignment Editor. The Assignment Editor is designed to make the process of making, changing, and managing a large number of assignments as easy as possible.

This white paper discusses the following topics:

- Using the Assignment Editor
- The New Assignment Editor Interface
- Category, Node, Information, Edit Bars & Entry Field
- Enhanced Spreadsheet-like Interface
- Dynamic Assignment Checker
- Node Filter Bar
- Customizable Columns
- Tcl Commands Displayed

Assignment Editor Overview

With the Quartus® II software version 3.0, the Assignment Editor replaces the Assignment Organizer. In previous versions of the Quartus II software, the Assignment Organizer was used to make project assignments and constraints with limitations. These limitations have been addressed and improved by the development of the Assignment Editor.

With its spreadsheet-like entry method and Category and Node Filter bars, the Quartus II Assignment Editor makes the creation and viewing of timing, logic option, and pin assignments quicker and easier.

To provide more flexibility, the Assignment Editor can be launched from various locations in the Quartus II software, including the Quartus II compilation report, Timing Closure Floorplan Editor, and the Messages window.

Using the Assignment Editor

You can use the Assignment Editor to make any location assignments, timing assignments, or logic options. The Assignment Editor is one of the preferred methods for setting assignments. Other methods include using the tool command language (Tcl) scripting interface, making location assignments with the Floorplan Editor, and creating LogicLock™ assignments with the LogicLock regions window.

For more information on making TCL assignments, see *AN 309: Command-Line Scripting in the Quartus II Software*.

You can use the Assignment Editor throughout the design cycle to assign pins for board layout, for making timing assignments for design requirements, and for making logic assignments to control logic optimization.

The project defaults and compiler settings (i.e., non-node-specific settings) are made in the **Settings** dialog box (Assignments menu).

Another change in the Quartus II software version 3.0 is the **Import MAX+PLUS II acf file** option that you can select from the **Import MAX+PLUS II Assignments** dialog box (Assignment menu).

The New Assignment Editor Interface

Similar to the design file editor or the compilation report, the Assignment Editor is resizable. This scalability makes it ideal to view and/or edit your assignments along with your design files. You can launch the Assignment Editor from the Assignments menu or by clicking on the Assignment Editor Icon, as shown in Figure 1.

Figure 1. Assignment Editor Icon

Additionally, the Assignment Editor allows you to collapse and hide three of the four bars (Category, Node, and Information) which helps control desktop real estate. The Edit bar can be hidden, but not collapsed.

Category, Node, Information, Edit Bars & Entry Field

The Assignment Editor is separated into into four bars and the spreadsheet-like entry area (see Figure 2).

Figure 2. The Assignment Editor Window

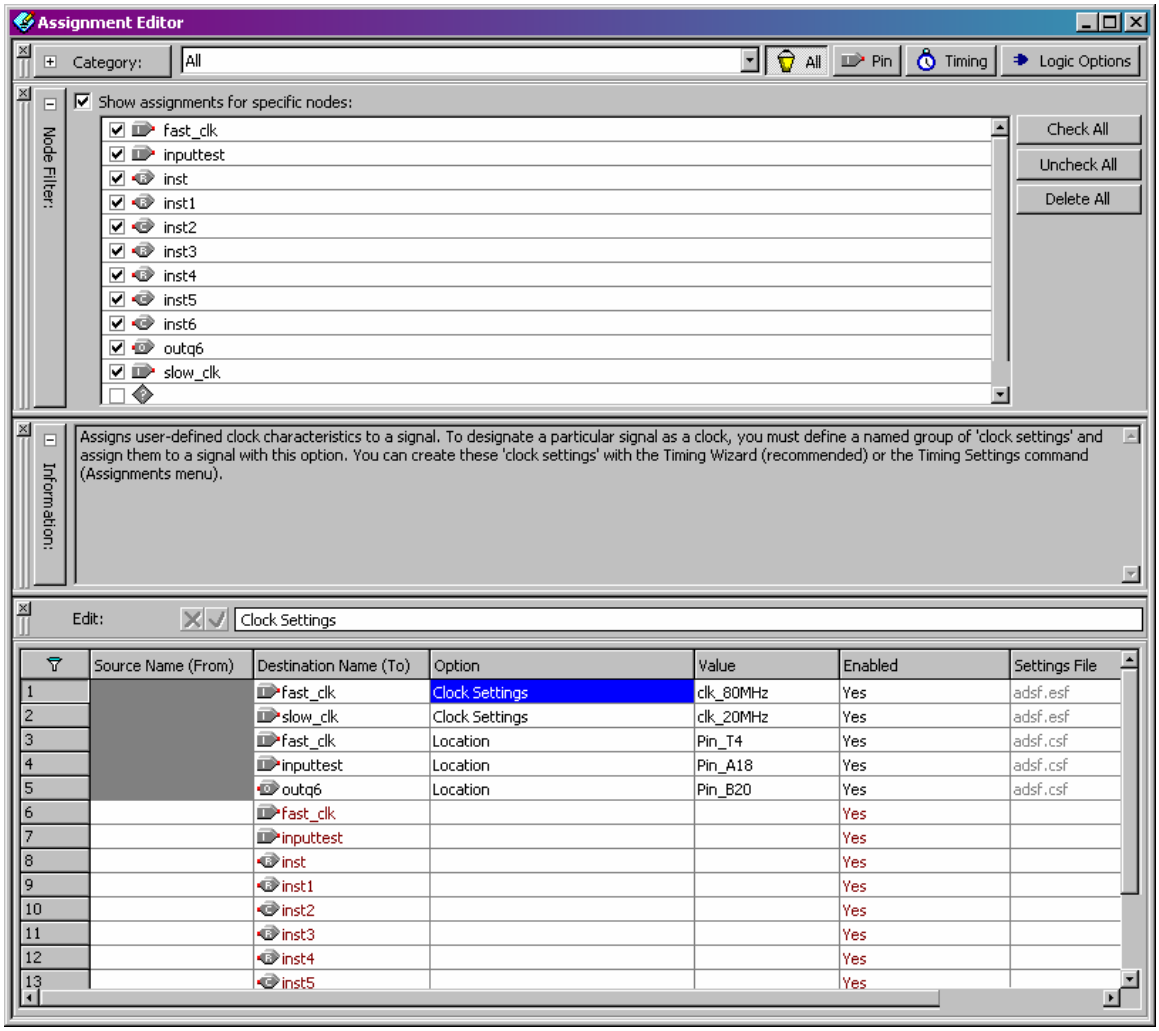


Table 1 describes the four bars of the Assignment Editor: the Category, Node Filter, Information, and Edit bars.

Table 1. Assignment Editor Bar Descriptions

Bar Name	Description
Category	Filters the types of assignment being made
Node Filter	Filters a selection of nodes to be viewed and assigned
Information	Displays a description of the cell currently selected
Edit	Allows the text in the currently selected cell to be edited

The Category bar is very useful when you are trying to make a large number of similar assignments. For example, select the timing/t_{SU} category when entering set-up time values for your input pins. With the category selected, you can view all your previous t_{SU} assignments as well as make new t_{SU} assignments.

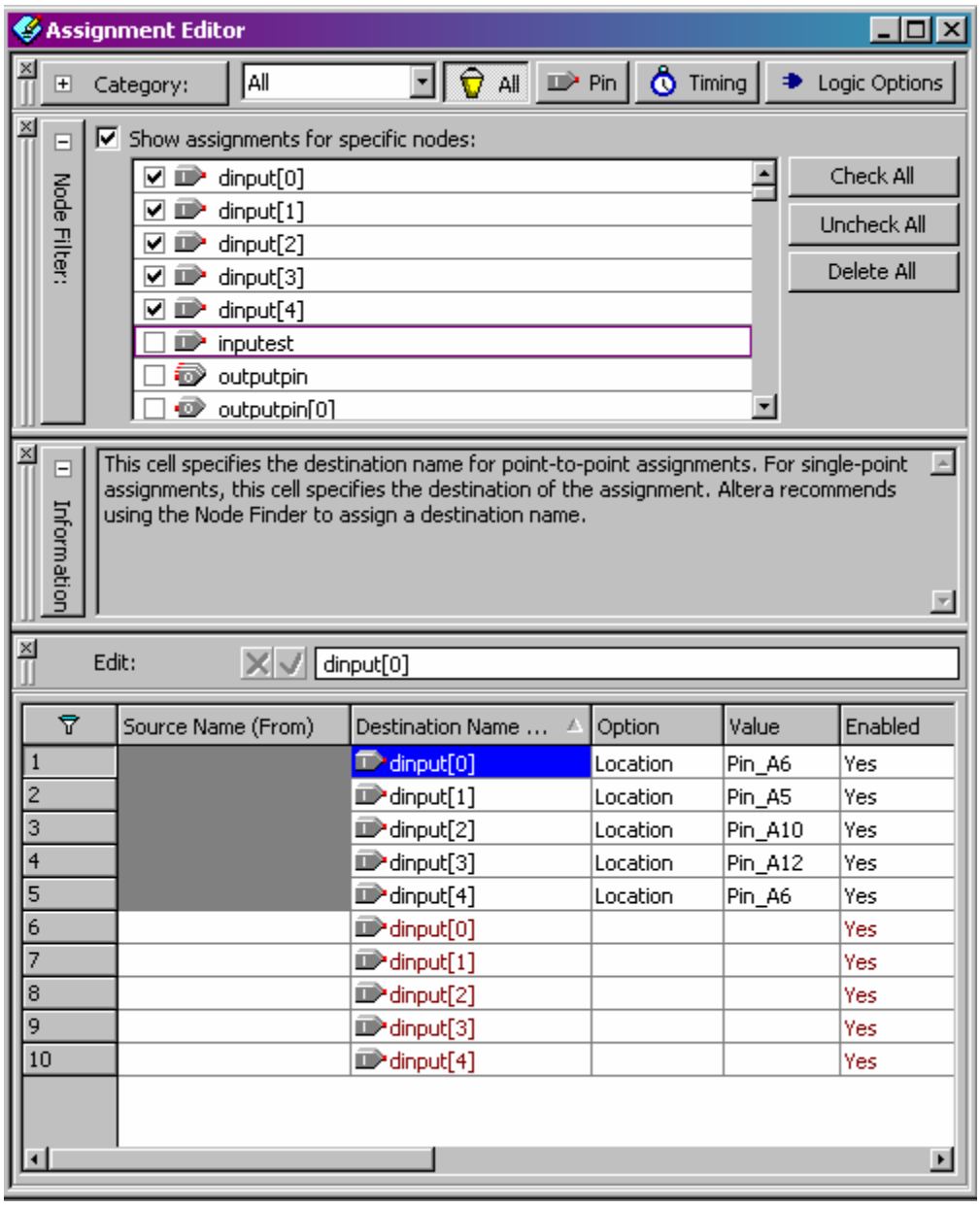
When you collapse the Category bar, there is a set of four commonly used shortcut buttons available for you to toggle between various preset category selections (see Figure 3).

Figure 3. Category Bar

The Node Filter bar stores a list of nodes which have previously been searched. This feature makes entering assignments easier because you can reselect the nodes to create a new assignment. You can use the Node Filter bar as a simple filter to view all assignments made to a particular set of nodes.

In Figure 4, you can check or uncheck the different entries to enable or disable each filter. In this case, each bit of the `dinput` bus is selected.

Figure 4. Using the Node Filter in the Assignment Editor



The Information bar provides a brief description of the currently selected cell. If you select a particular logic option, the Information bar shows a description of how that option impacts the design. The Information bar is similar to the Description box in the Assignment Organizer.

The Edit bar is another way to edit the field of the currently selected cell (which can be a node or an option). You can directly enter the value for a currently selected cell(s).

One of the key features of the Edit bar is its ability to simultaneously change the value of multiple cells. For example, to change the I/O standards of a number of pins, you can select the cells below the I/O standard column and change the value with the Edit bar.

Associated Files

The Assignment Editor loads the assignments that exist in two of the Quartus II settings files: Entity Settings File (**.esf**) and Compiler Settings File (**.csf**).

As assignments are made, modified, and removed within the Assignment Editor, they are not saved or applied to your current design until the settings are saved. When you save the assignment settings made in the Assignment Editor, the Quartus II software writes the assignments to the appropriate settings files.

Assignment Editor Features

The Assignment Editor has many new and enhanced features.

Enhanced Spreadsheet-Like Interface

One of the key features of the Assignment Editor is the spreadsheet-based entry field. With the spreadsheet-like interface, you can sort the assignments, use the pull down entry boxes, or use the clipboard support. It is easy to copy and paste multiple cells within the Assignment Editor spreadsheet, making pin assignments and project documentation significantly easier.

There are many ways to enter nodes into the spreadsheet, including: the Node Finder, the Node Filter bar, the Edit bar, or by directly typing the node name into the cell within the spreadsheet. Wildcards are supported for the source and destination nodes for certain types of entries.

In the Quartus II software version 3.0, node names support wildcards in the following types of assignments:

- All timing assignments
- Point-to-point global signal assignments (applicable for Stratix™ devices)
- Point-to-point, or pad-to-core delay chain assignments

The spreadsheet-like interface also supports customizable columns, allowing you to show, hide, and arrange the columns.

When making pin location assignments, the background color of the cells will mirror the color of the I/O bank. These colors will match the color in the Floorplan Editor (see Figure 5).

Figure 5. Spreadsheet-Like Interface

	Name	Location	I/O Bank	I/O Standard	General Function	Special Function
1	clk	Pin_R26	6	LVTTL	Dedicated Clock	CLK9p
2	dinput[0]	Pin_D22	4	LVTTL	Column I/O	DQ0T2
3	dinput[1]	Pin_F24	5	LVTTL	Row I/O	DIFFIO_TX24p
4	dinput[2]	Pin_AA4	1	LVTTL	Row I/O	DIFFIO_TX2p
5	dinput[3]	Pin_E3	2	LVTTL	Row I/O	DIFFIO_TX21p
6	dinput[4]	Pin_F3	2	LVTTL	Row I/O	DIFFIO_TX20p
7	outputpin[0]	Pin_D24	5	LVTTL	Row I/O	DIFFIO_TX22n
8	outputpin[1]	Pin_F23	5	LVTTL	Row I/O	DIFFIO_TX24n
9	outputpin[2]	Pin_AA2	1	LVTTL	Row I/O	DIFFIO_RX2p
10	outputpin[3]	Pin_B3	3	LVTTL	Column I/O	DQ9T4
11	outputpin[4]	Pin_K3	2	LVTTL	Row I/O	DIFFIO_RX20n/RDN2
12	rx_in[0]	Pin_AC2	1	LVTTL	Row I/O	DIFFIO_RX0p
13	rx_inclock	Pin_R1	1	LVTTL	Dedicated Clock	CLK2p
14	rx_locked	Pin_P6	1	LVTTL	Row I/O	DIFFIO_TX10p
15	rx_out[0]	Pin_AE2	8	LVDS	Column I/O	DQ9B5
16	rx_out[1]	Pin_AA3	1	LVDS	Row I/O	DIFFIO_TX2n
17	rx_out[2]	Pin_AD2	8	LVDS	Column I/O	DQ9B6
18	rx_out[3]	Pin_AD4	8	LVDS	Column I/O	DQS9B
19	rx_outclock	Pin_T7	1	LVTTL	Row I/O	DIFFIO_TX6p

The color of the font in each row shows the status of the assignment providing instant feedback. The colors will indicate if the assignment is incomplete, incorrect, or disabled. Quartus II Help describes the color of the font and the status of the assignment in more detail.

Dynamic Assignment Checker

The Assignment Editor performs simple legality checks on your assignment. As each assignment is entered, the Assignment Editor dynamically checks your assignment and does not accept illegal assignments. Dynamic checking is not as thorough as the checks done during a full compilation, but it can report general incorrect settings.

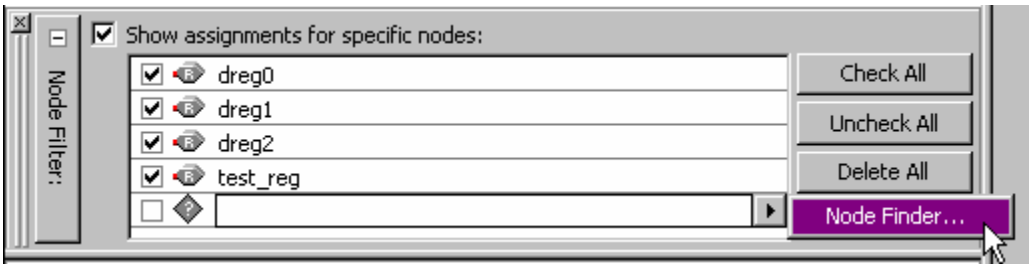
For example, the Assignment Editor does not allow a pin to be assigned to a no-connect pin. In this case, the assignment is not accepted and another pin location must be entered.

Node Filter Bar

In the Assignment Organizer, from previous versions of the Quartus II software, it was difficult to view an additional set of nodes. The Assignment Editor's Node Filter bar provides much more flexibility in how you view and make your settings.

The Node Filter bar consists of a list of node filter entries. To create a new entry, you can use the Node Finder or manually type the node name. Double clicking in an empty entry of the Node Filter bar, and then clicking on the scroll arrow brings up the Node Finder option (see Figure 6).

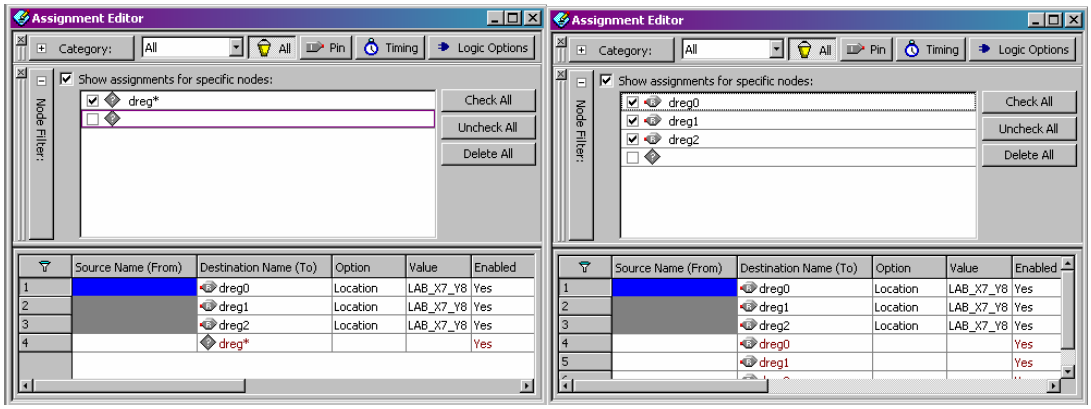
Figure 6. Node Finder Option



You can enable or disable each filter by clicking on the checkbox next to it, or all filters by clicking the **Show assignments for specific nodes** check box.

The Node Filter bar supports the use of the wildcard symbols "*" and "?". You can use wildcards to filter a selection of all the design nodes with one entry in the Node Filter. For example, you can enter three registers in the Node Filter bar for signals called `dreg0`, `dreg1`, and `dreg2`. With the use of wildcards, only one entry is necessary, `dreg*` (see Figure 7).

Figure 7. Using the Node Filter Bar with or without Wildcards



The Node Filter bar is a very effective feature, providing a simple and quick method of creating and viewing selected nodes.

Customizable Columns

To provide more control, the Assignment Editor supports customizable columns. The Assignment Organizer was not as flexible and did not allow any customization.

By default, a selection from all of the available columns is shown. However, additional columns can be shown/hidden (e.g., the Comments or Enable fields). The Comments field is a great way to document the purpose of a particular I/O pin or to explain why a particular constraint was assigned to the node.

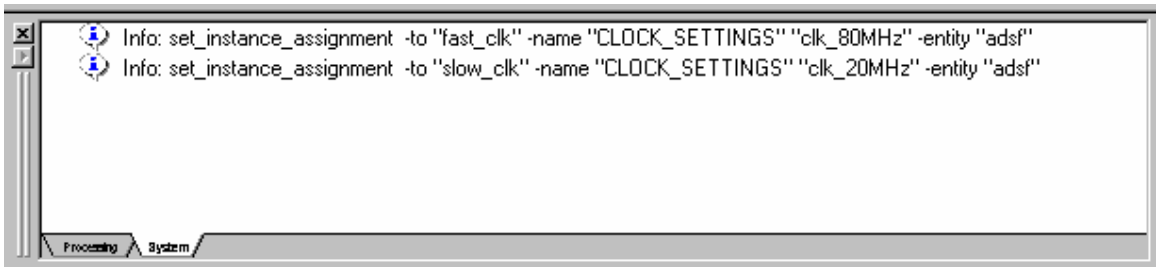
The Enable field option allows you to enable or disable a particular logic assignment without the assignment being deleted. This feature is useful when performing various compilations with different timing constraints or logic optimizations.

Tcl Commands Displayed

The Assignment Editor can easily convert the assignments to a Tcl script. After creating all assignments with the Assignment Editor, you can take advantage of the Tcl exporter by selecting **Export** (File menu).

Additionally, as assignments are entered through the Assignment Editor, the equivalent Tcl command is echoed in the system message window. To view the Messages window, select **Messages** (View, Utility Windows menu). You can copy these commands to create customized Tcl scripts (see Figure 8).

Figure 8. Equivalent Tcl Commands Displayed in the Messages Window



Conclusion

As FPGAs continue to increase in density and pin count, it is essential to quickly create and view design assignments. The new Assignment Editor facilitates an intuitive and effective way of making assignments. With the spreadsheet-like interface and the Category and Node Filters, the Assignment Editor provides an efficient assignment entry solution for FPGA designers.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com