Developing on Xilinx Zynq using C to RTL automatic conversion

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Accelerating Your Success™

Objectives

- **Introduce Avnet Silica**
- **Understand the Zynq-7000 All Programmable SoC architecture**
- **Introduce the Vivado High Level Synthesis**
  - Automatic conversion from C/C++ to VHDL/Verilog

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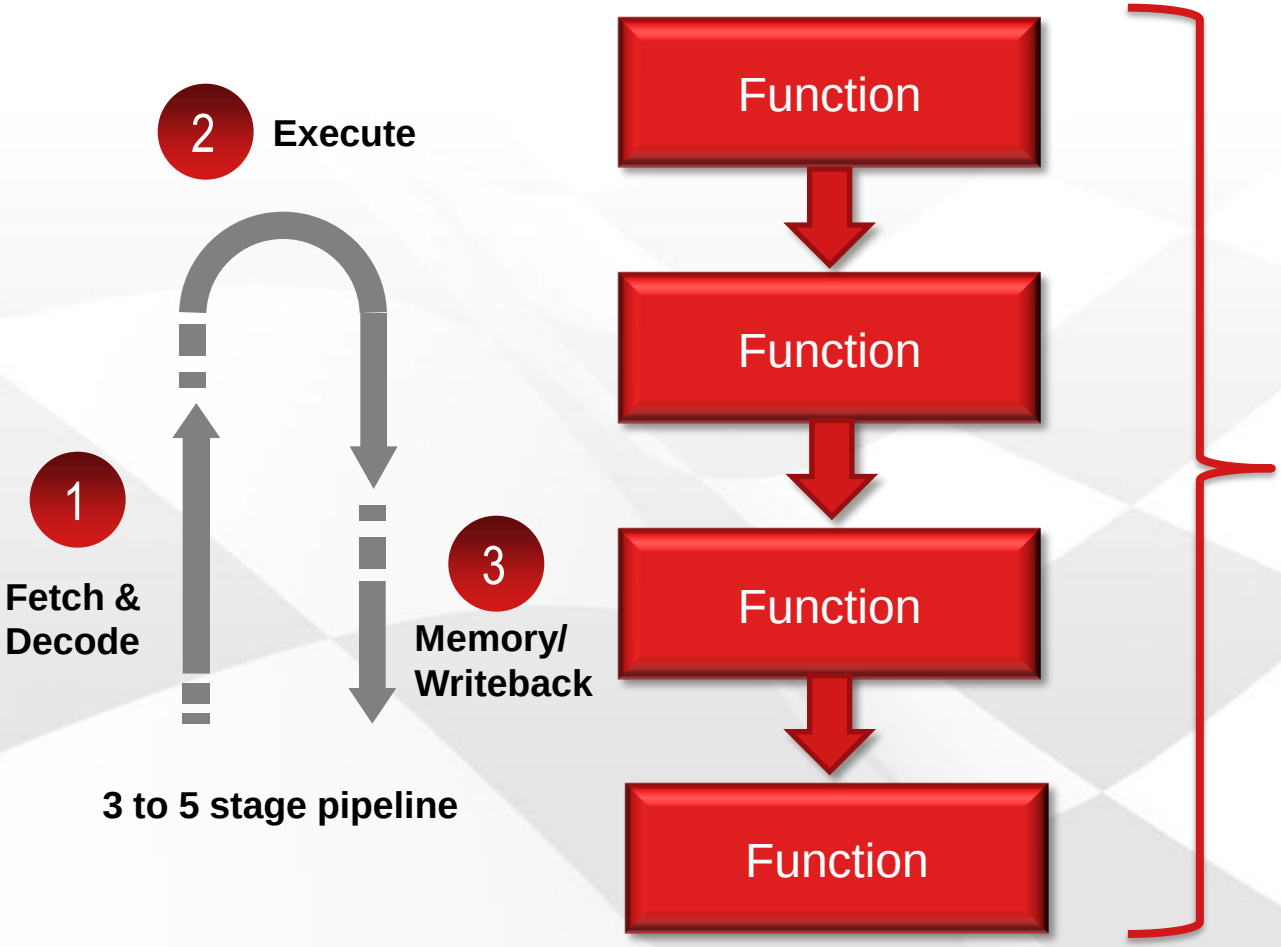
System Bottlenecked?

- **Profiling indicates processor activity**
  - Is processor utilization exceeding 90%?
  - Processor Queue Length > 2?
  - If multiprocessor system, processor time > 50%?
  - Intensive reoccurring tasks?

- **Effects of overburdened Processors include:**
  - Increased Data Latency
  - Delayed Interrupt Handling
  - Lowered Data Throughput

Software Engineers: Stuck in a Sequential World



Sequential Processing limits performance

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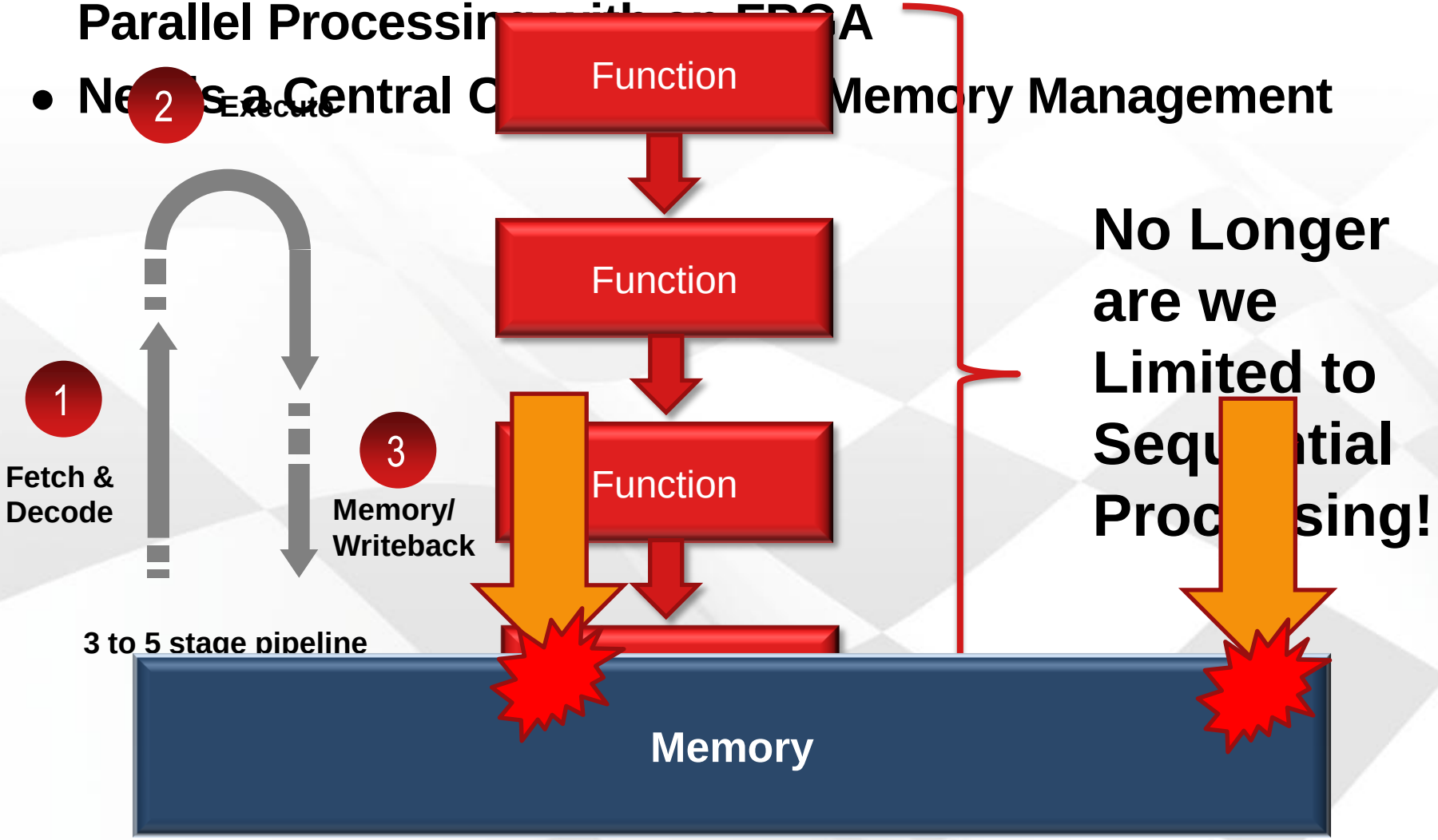
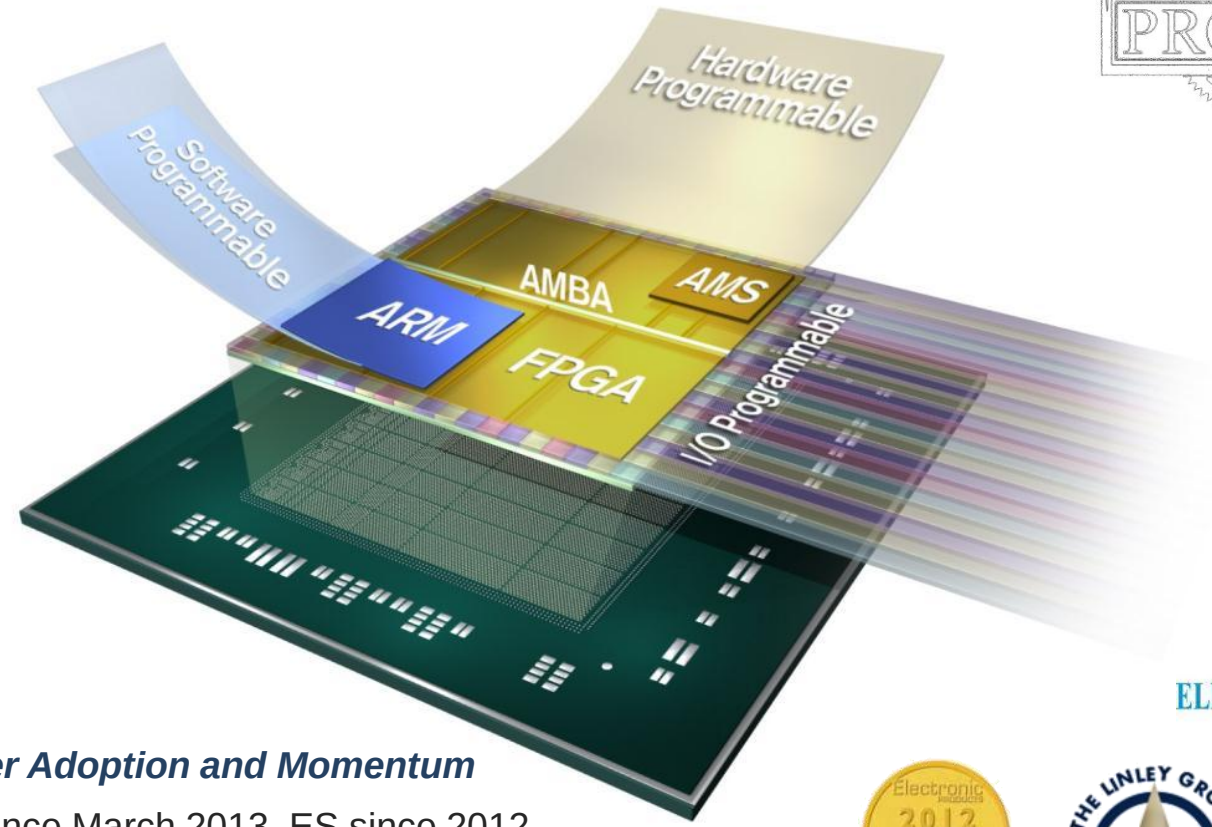
Parallel Processing is Efficient…

- **For critical systems and performance, Engineers utilize Parallel Processin[illegible]A**
- **Ne[illegible]s a Central C[illegible]Memory Management**



The First All Programmable SoC



ZYNQ

Significant Customer Adoption and Momentum

- ✓ In full production since March 2013, ES since 2012
- ✓ 500+ unique customers actively designing
- ✓ 100+ Zynq specific partners
- ✓ All major OSs supported and in use
- ✓ 20+ different development boards and SOMs

PROVEN

ELECTRON D'OR

Electronic Products 2012 Product of the Year Award

The Linley Group 2012 Analysts' Choice

ACE AWARDS EETimes EDN

EDN China Innovation Award 创新奖 2011 优秀产品奖

Best of Show Award ESC 2010 San Jose

Elektra 2011 European Electronics Industry Awards WINNER

IET Awards The Institution of Engineering and Technology

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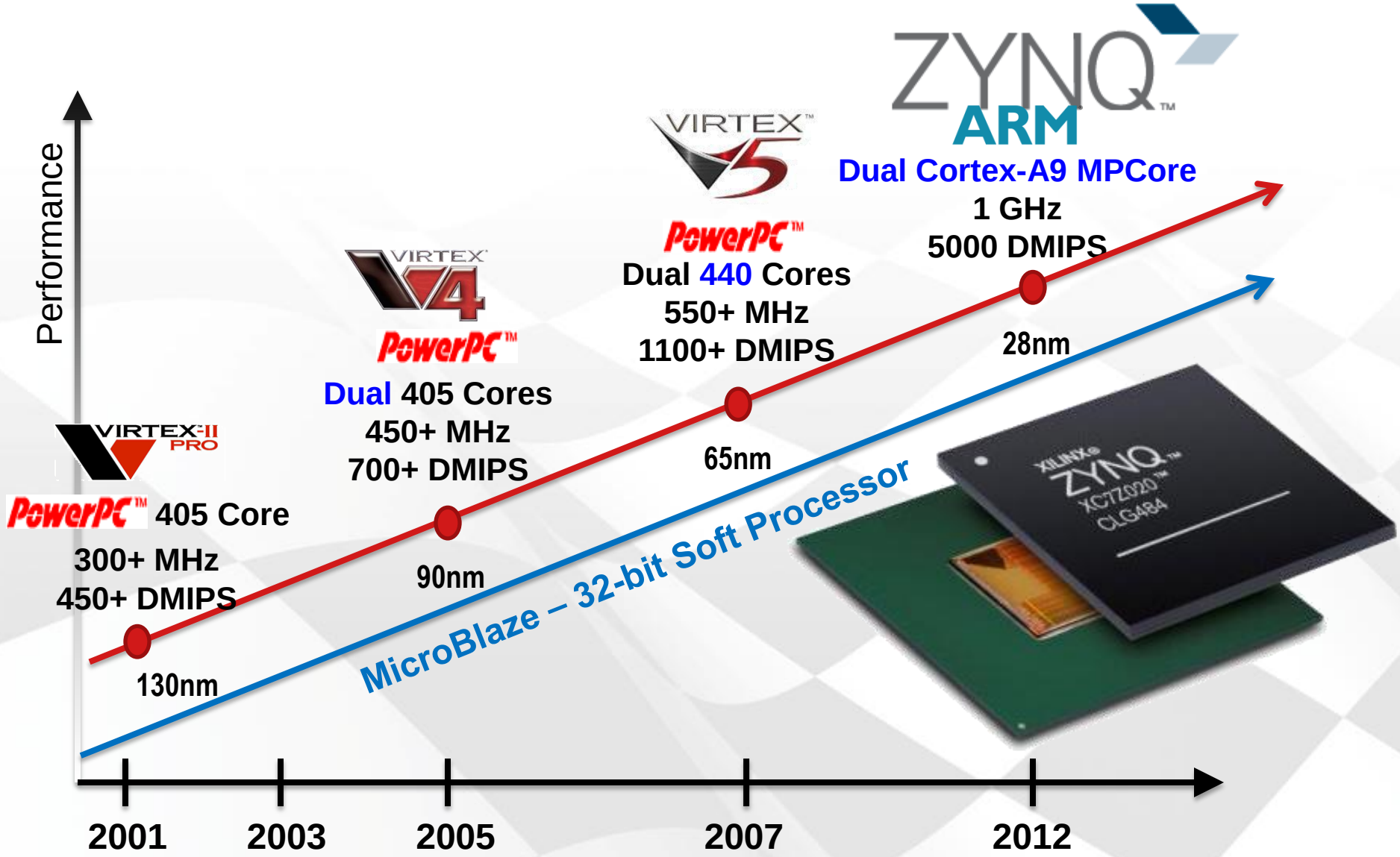
Xilinx Processing Heritage



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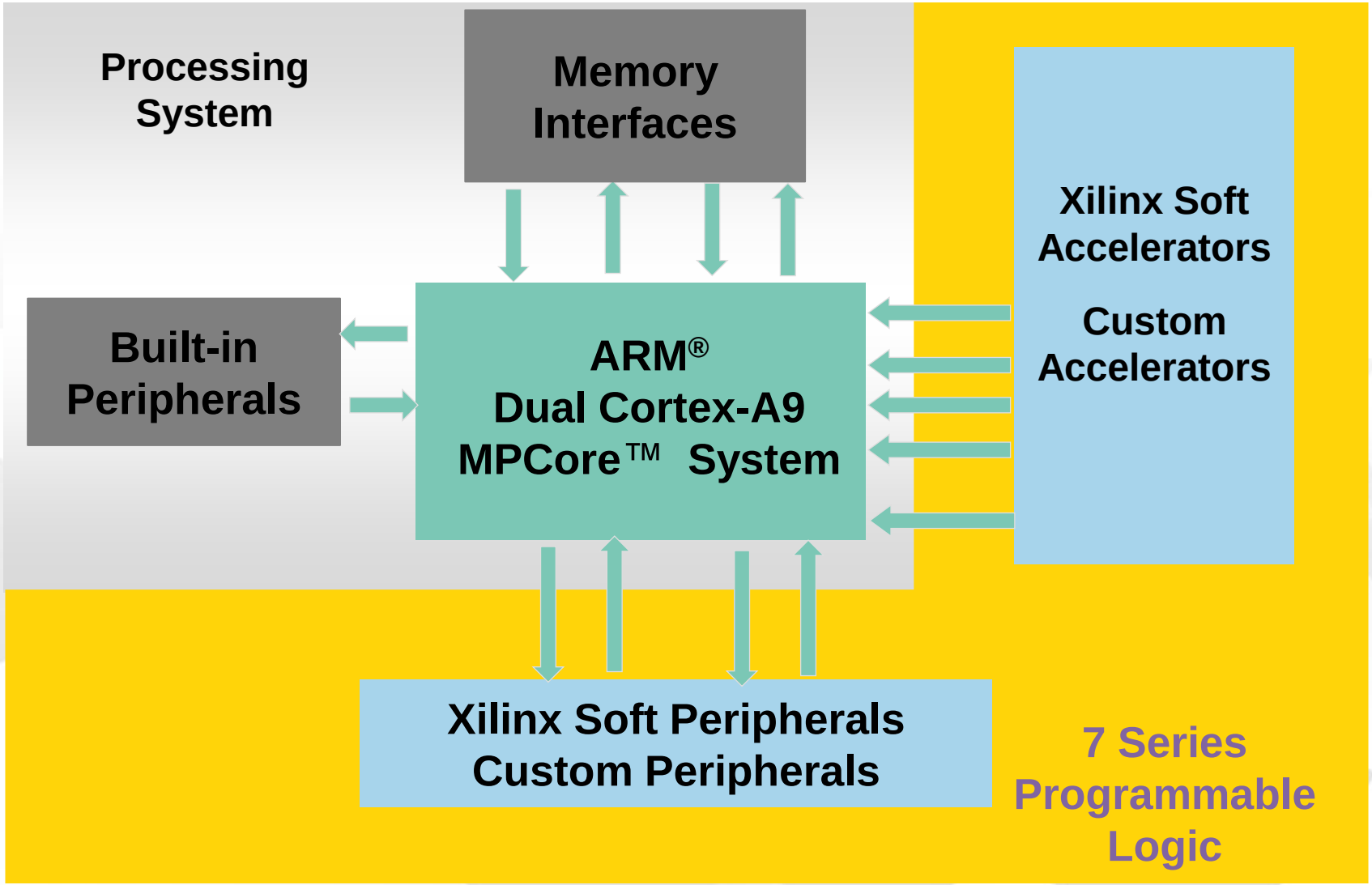
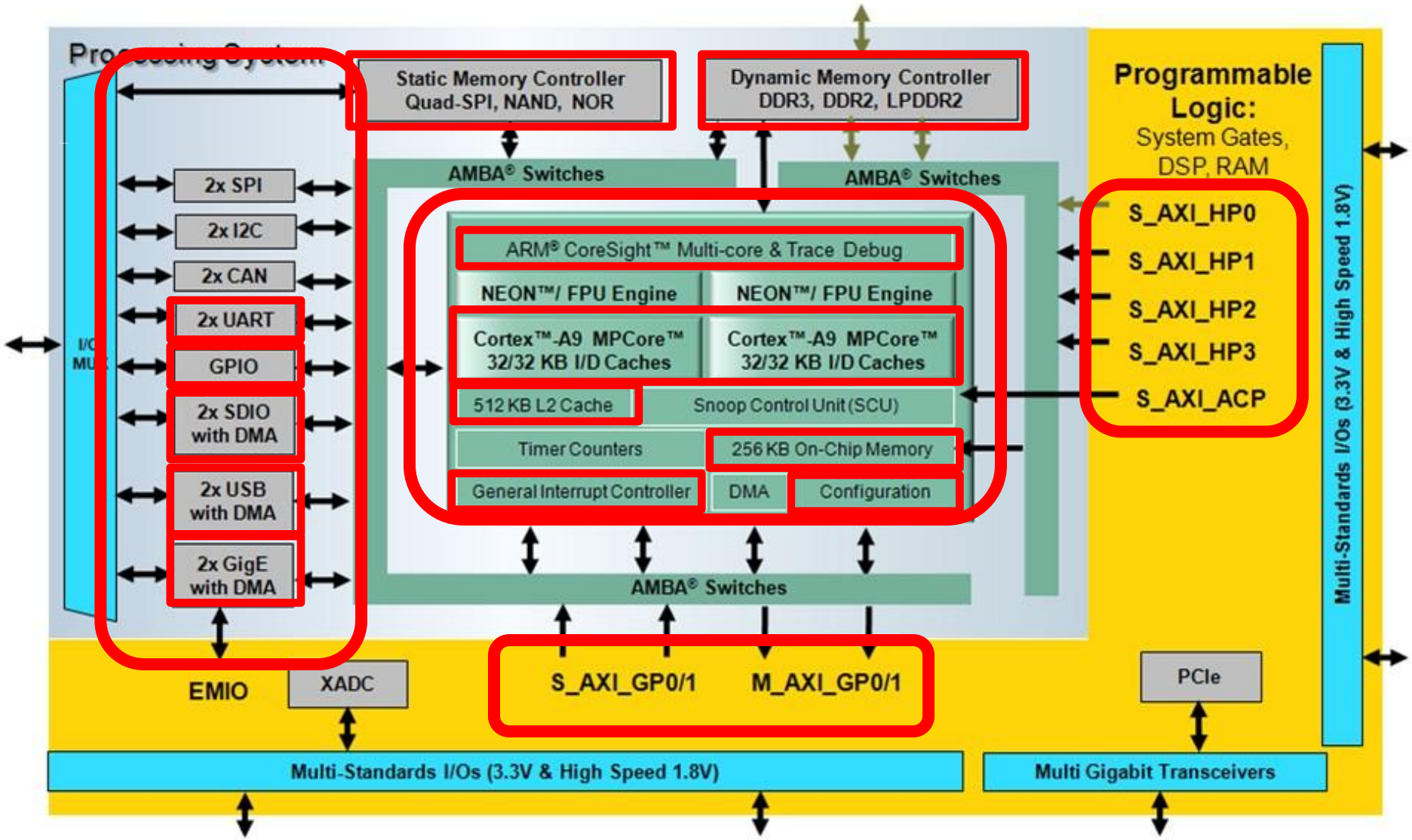
10+ years, 4 Generations

Zynq-7000 AP SoC Basic Architecture



Zynq-7000 AP SoC Block Diagram



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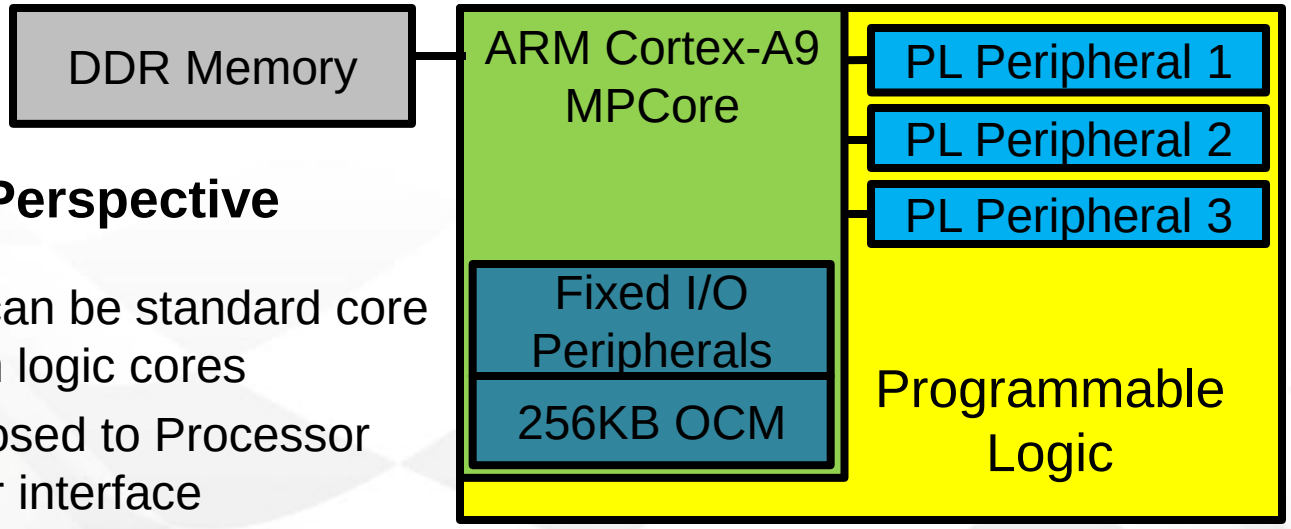
Connecting HW and SW

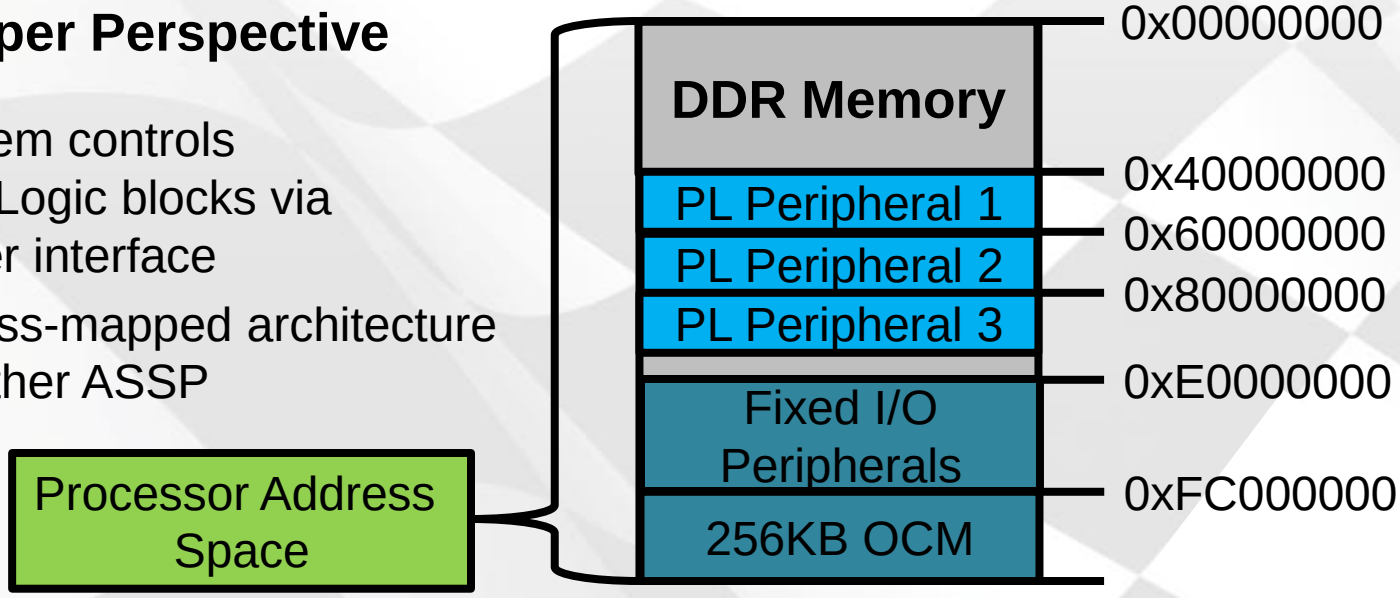


Hardware Designer Perspective

- Peripheral blocks can be standard core offerings or custom logic cores
- Logic controls exposed to Processor System via register interface

Software Developer Perspective

- Processor System controls Programmable Logic blocks via exposed register interface
- Standard address-mapped architecture similar to any other ASSP



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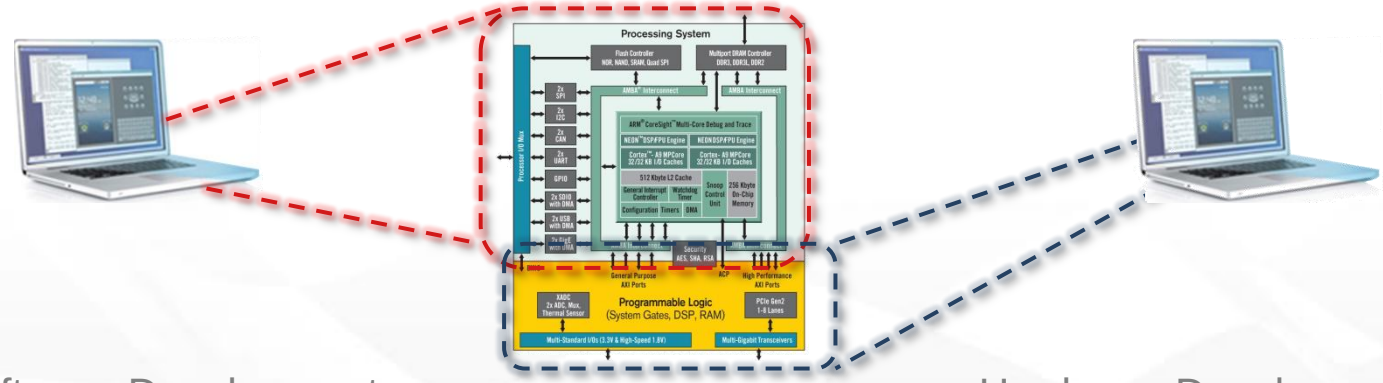
Parallel Developments of your AP SoC Based Application



Software Development

- **Processor boots first like any ARM based SoC.**
- **SW developers can use their favorite SW tool to load / debug SW code over JTAG**
- **Programmable Logic can be left unconfigured while developing on real hardware**

Hardware Development

- **Reference SW boots processor first leaving PL up and ready to be programmed through JTAG**
- **Vivado Probe connects to Programmable Logic like to any other FPGA**
- **FPGA developer can start loading / debug like for any FPGA**

SW developments like any other ARM based SoC

HW developments like any other Xilinx FPGA

Extensive OS, Middleware & Stack Ecosystem

Middleware and Stacks

mentor embedded
The MathWorks
QNX
iVeia
ENEA
Microsoft
Micrium
Green Hills SOFTWARE
WIND RIVER
timesys
logicBRICKS Designed by XYLON
expresslogic
Discretix trust • embedded
eSOL
montavista

Operating Systems

THREADX
NUCLEUS
ENEA
Linux and OSE
RTXC RTOS
WIND RIVER
Linux and VxWorks
QNX
T-Kernel
INTEGRITY
XILINX
Open Source Linux & Commercial Linux
freeRTOS
ecos
Microsoft Windows Embedded
android
µC/OS-II The Real-Time Kernel

Hypervisors

Open Kernel Labs
WIND RIVER
sierraware
open virtualization
Green Hills SOFTWARE
SYSGO EMBEDDING INNOVATIONS

Zynq-7000 Device Portfolio Summary

Scalable platform offers easy migration between devices

	Zynq-7000 AP SoC Devices	Z-7010	Z-7015	Z-7020	Z-7030	Z-7045	Z-7100
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™					
	Processor Extensions	NEON™ & Single / Double Precision Floating Point					
	Max Frequency	866 MHz			Up to 1 GHz		
	Memory	L1 Cache 32KB I / D, L2 Cache 512KB, on-chip Memory 256KB					
	External Memory Support	DDR3, DDR3L, DDR2, LPDDR2,2x QSPI, NAND, NOR					
	Peripherals	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO					
Programmable Logic	Approximate ASIC Gates	~430K (28k LC)	~1.1M (74k LC)	~1.3M (85k LC)	~1.9M (125k LC)	~5.2M (350k LC)	~6.6M (444kLC)
	Block RAM	240KB	380KB	560KB	1,060KB	2,180KB	3,020KB
	Peak DSP Performance (Symmetric FIR)	100 GMACS	200GMACS	276 GMACS	593 GMACS	1334 GMACS	2662 GMACS
	PCI Express® (Root Complex or Endpoint)	-	Gen2 x4	-	Gen2 x4	Gen2 x8	
	Agile Mixed Signal (XADC)	2x 12bit 1Msps A/D Converter					
I/O	Processor System IO	130					
	Multi Standards 3.3V IO	100	150	200	100	212	250
	Multi Standards High Performance 1.8V IO	-	-	-	150	150	150
	Multi Gigabit Transceivers	-	4	-	4	16	16

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MicroZed

ZedBoard

Zynq Prototyping and Production Solutions

We've got you covered!

- **ZedBoard**
- **ZC702**
- **ZC706**
- **MicroZed**
- **Zynq MMP**
- **Zynq Mini-ITX**

- **IVK**
- **SDR**

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Xilinx Embedded Tool Flow

- **Vivado Design Suite WebPACK Edition**
  - **FREE!**
  - Supports **four** Zynq devices: 7010, 7015, 7020 and 7030

Pillars of Productivity	Features	WebPACK	Design Edition	System Edition	Free 30-day Eval
IP Integration and Implementation	Integrated Design Environment	√	√	√	√
	Software Development Kit (SDK)	√	√	√	√
Verification and Debug	Vivado Simulator	√	√	√	√
	Vivado Logic Analyzer		√	√	√
	Vivado Serial Analyzer		√	√	√
Design Exploration and IP Generation	High-Level Synthesis			√	√
	System Generator for DSP			√	√

- **MicroZed and ZedBoard include license for Vivado Analyzer**

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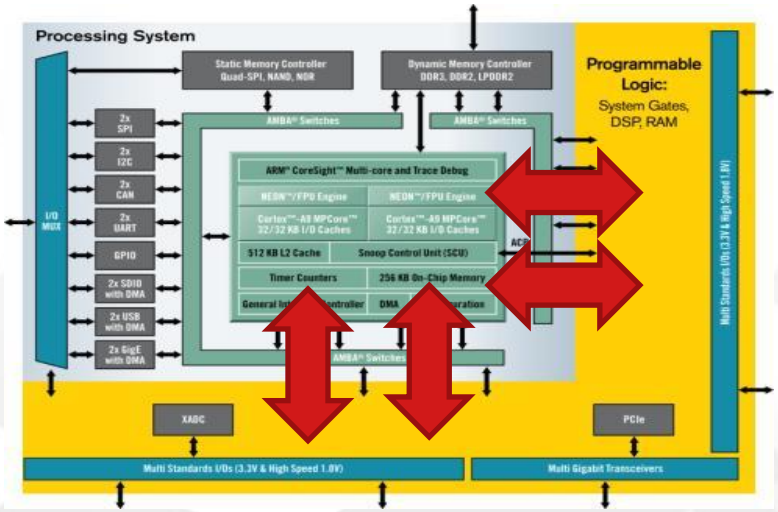
Increased System Performance

- **Increasing SW Processing Performance with:**
  - Programmable Logic
  - Massive DSP processing
  - High throughput AXI
    - Over 3000 PS to PL direct connections
  - High performance I/Os
  - Gigabit transceivers



Elements	Performance (up to)
Processors (each)	1 GHz
PL Fabric/ DSP Fmax	741 MHz
DSP (aggregate)	1080 GMACs
Transceivers (each)	12.5Gbps

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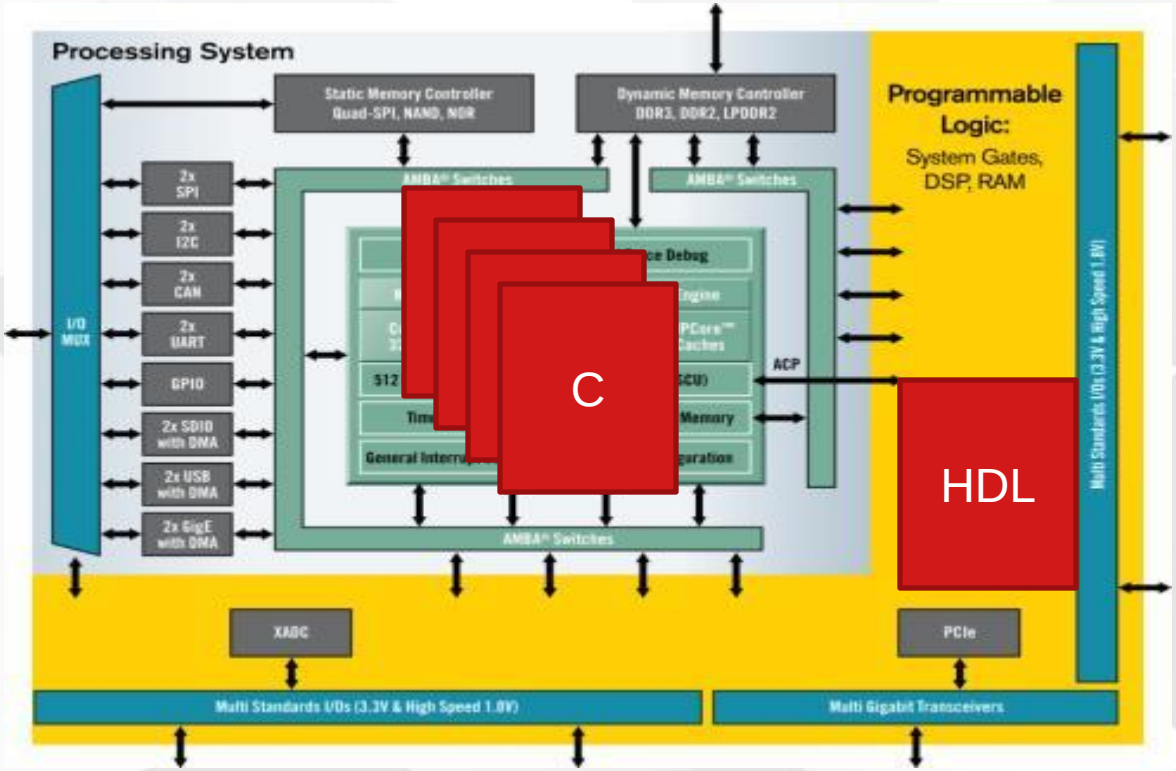
Increased System Performance

- **Optimized & Simplified HW/SW Partitioning**
  - HW acceleration enables scaling SW performance to address many applications
  - Low latency interfacing for efficient co-processor implementation and high throughput data transfers



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