Radiation Hardness of Silicon Detectors

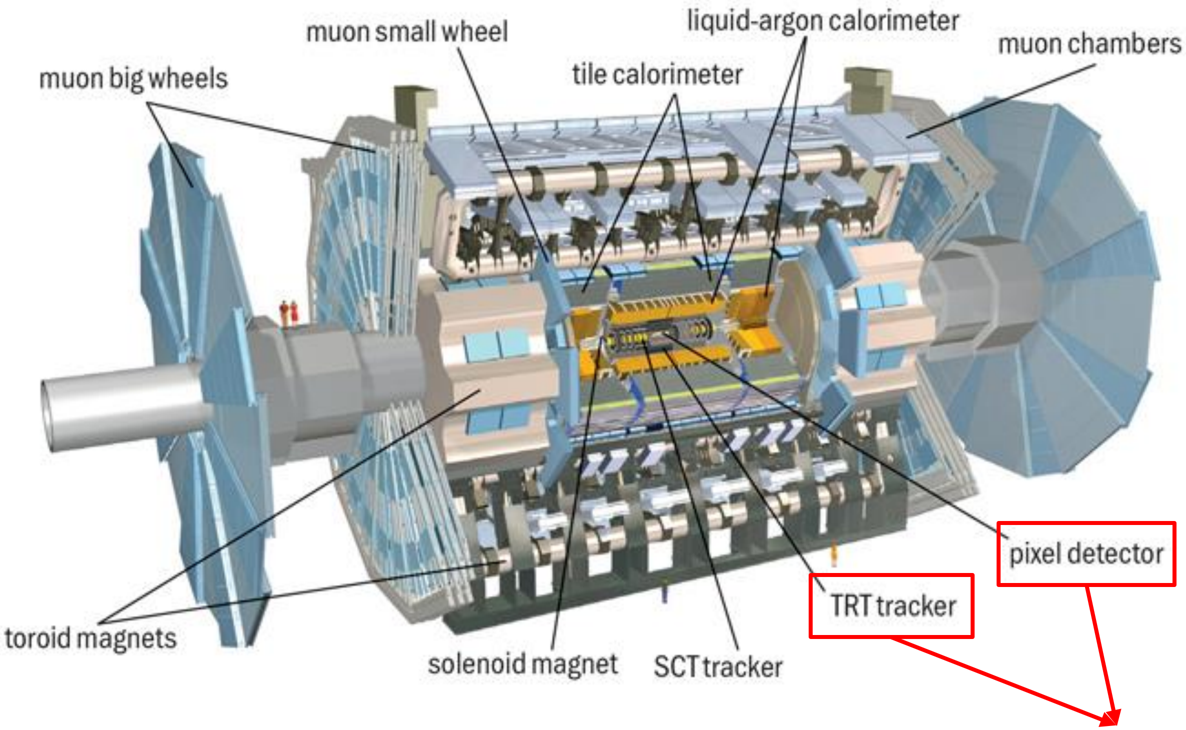
Prof. Laura Gonella

Outline

- **Silicon detectors in HEP**
- Radiation environment at collider experiments
- Surface damage to electronics
- Examples of radiation hard detectors
    - ATLAS IBL
    - ATLAS ITk strip detector
- Conclusion

HEP experiments at colliders

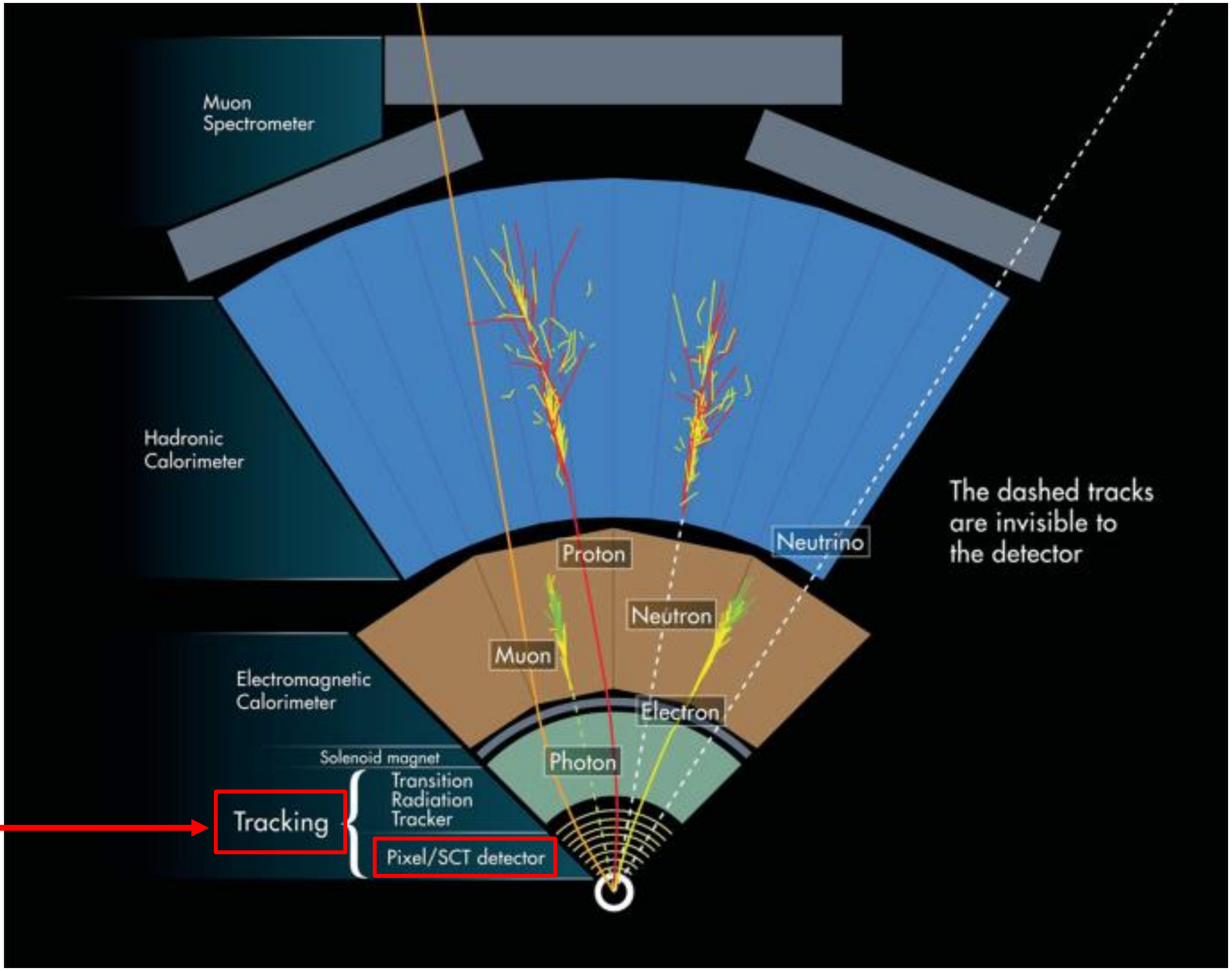
Example: The ATLAS detector



Silicon detectors

HEP experiments at colliders

Particles in the ATLAS detector



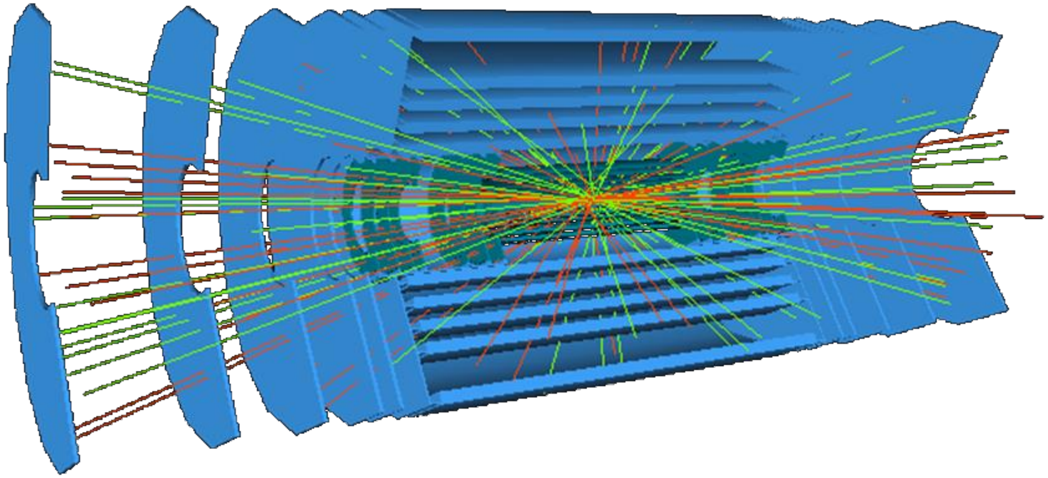
Silicon detectors

Silicon detectors in HEP

- Highly segmented semiconductor detectors have been used in particle and nuclear physics experiments for over 40 years

- Silicon detectors are the technology of choice for the detectors that operate close to the interaction point at collider experiments

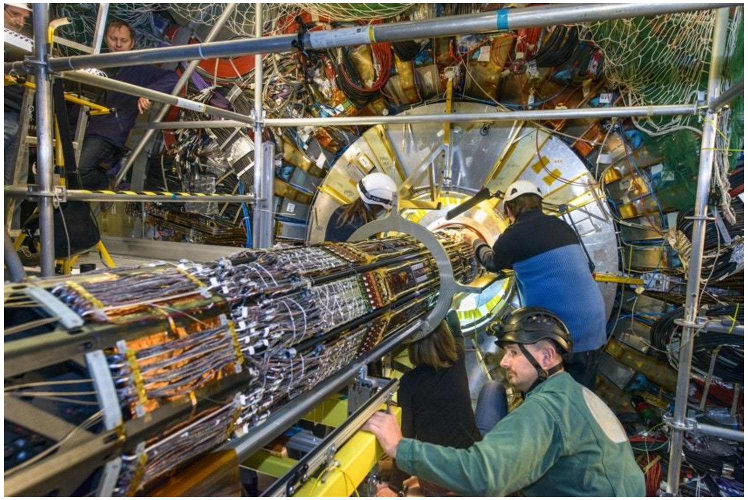
- They measure and reconstruct the trajectories of all charged particles produced in the collision with high spatial resolution and efficiency



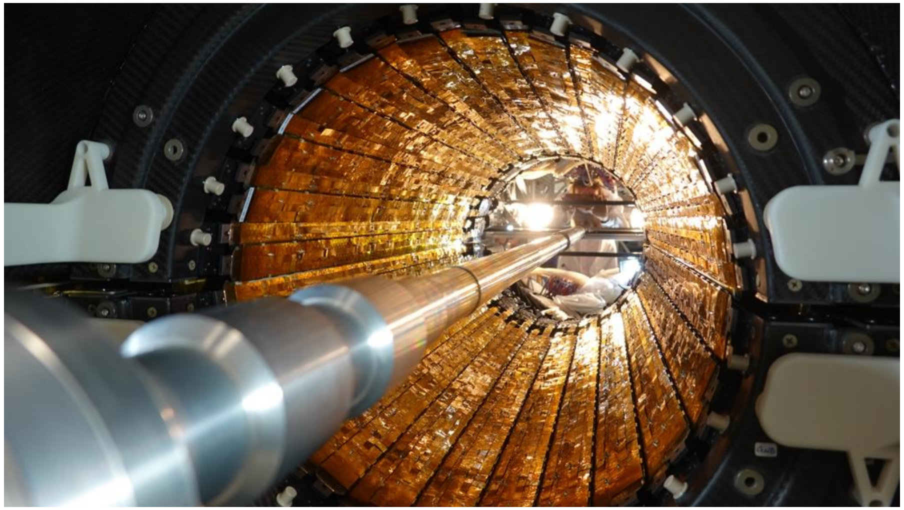
Simulation of the ATLAS Inner Detector at the LHC

Silicon detectors at the LHC

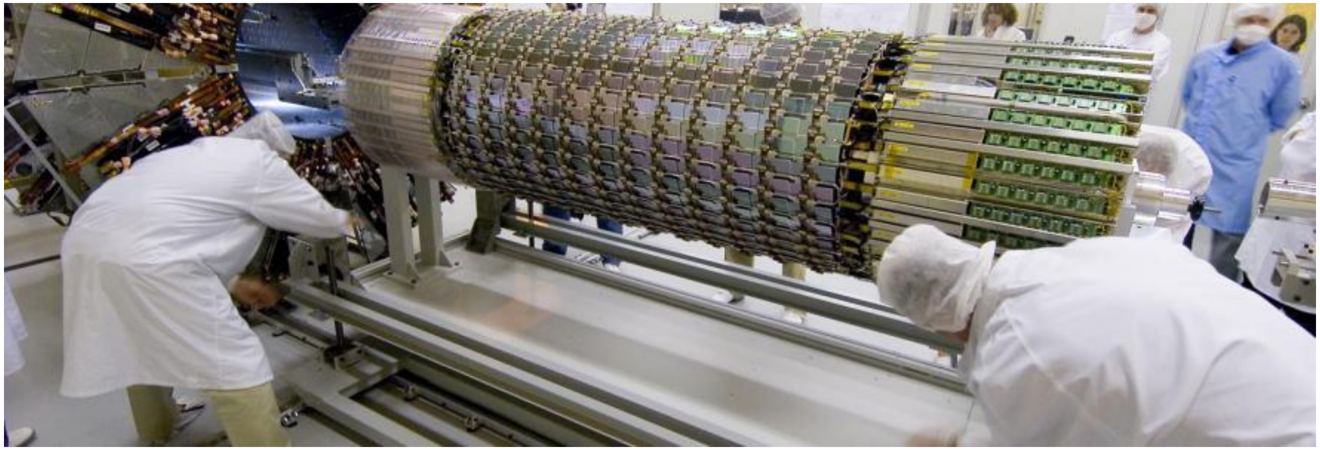
ATLAS pixels



ALICE ITS2

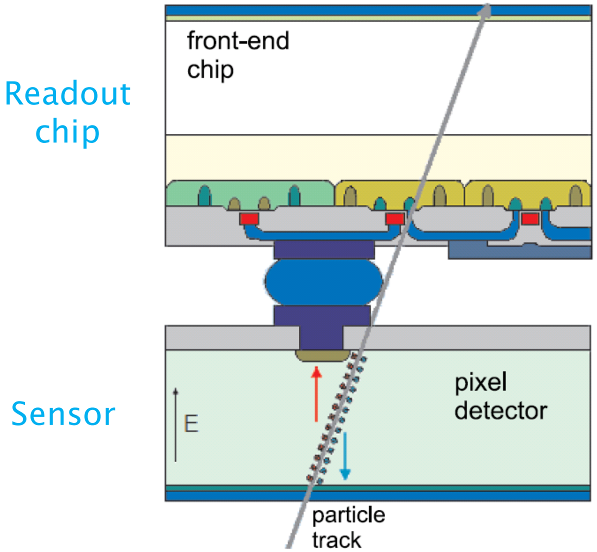


ATLAS SCT

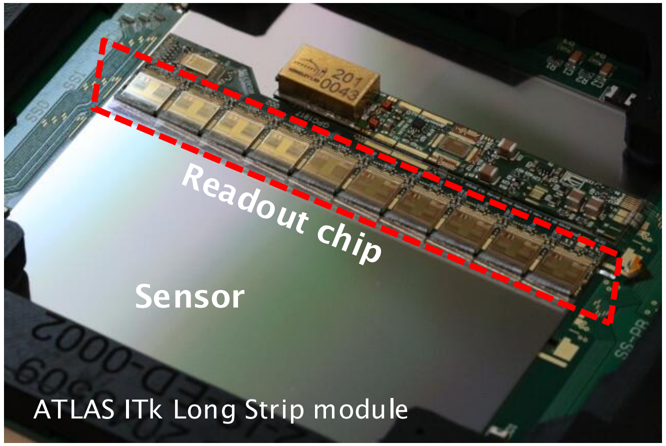


Silicon detectors: Configurations

Pixels - Hybrid

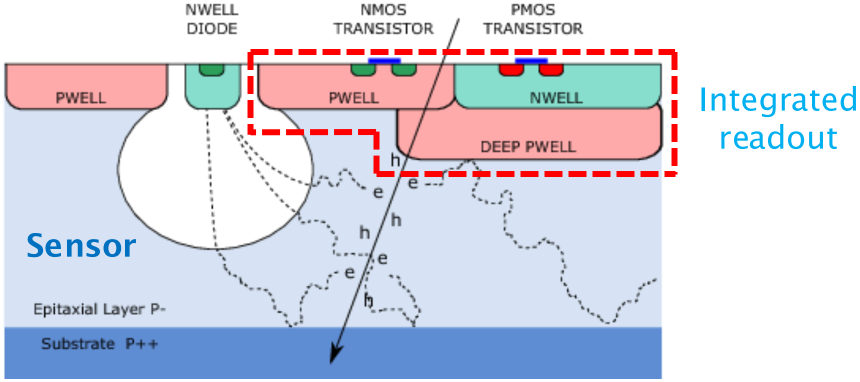


Strips



ATLAS ITk Long Strip module

Pixels - Monolithic



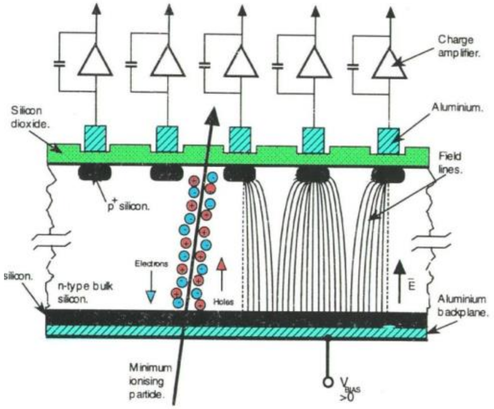
ALICE ITS2 ALPIDE detector, sketch of the cross-section of one pixel

Different flavours, basic elements: sensor + readout electronics.

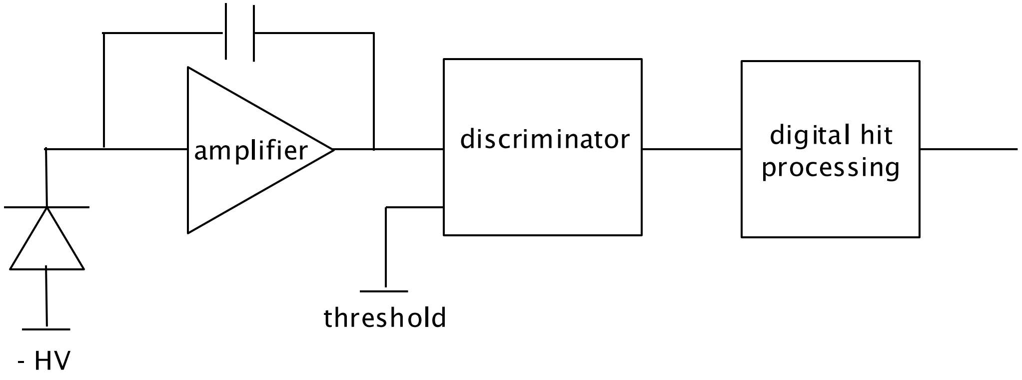
Both sensor are electronics are implemented in silicon.

Silicon detectors: Technology

- Sensor for charge collection
  - Reverse biased pn-junction
  - Charge collection in depleted sensor volume
  - Pixel or strip electrode segmentation



- Readout electronics for signal processing
  - Application Specific Integrated Circuits (ASIC) in deep submicron CMOS technologies
  - Amplification, analogue to digital conversion, digital signal processing



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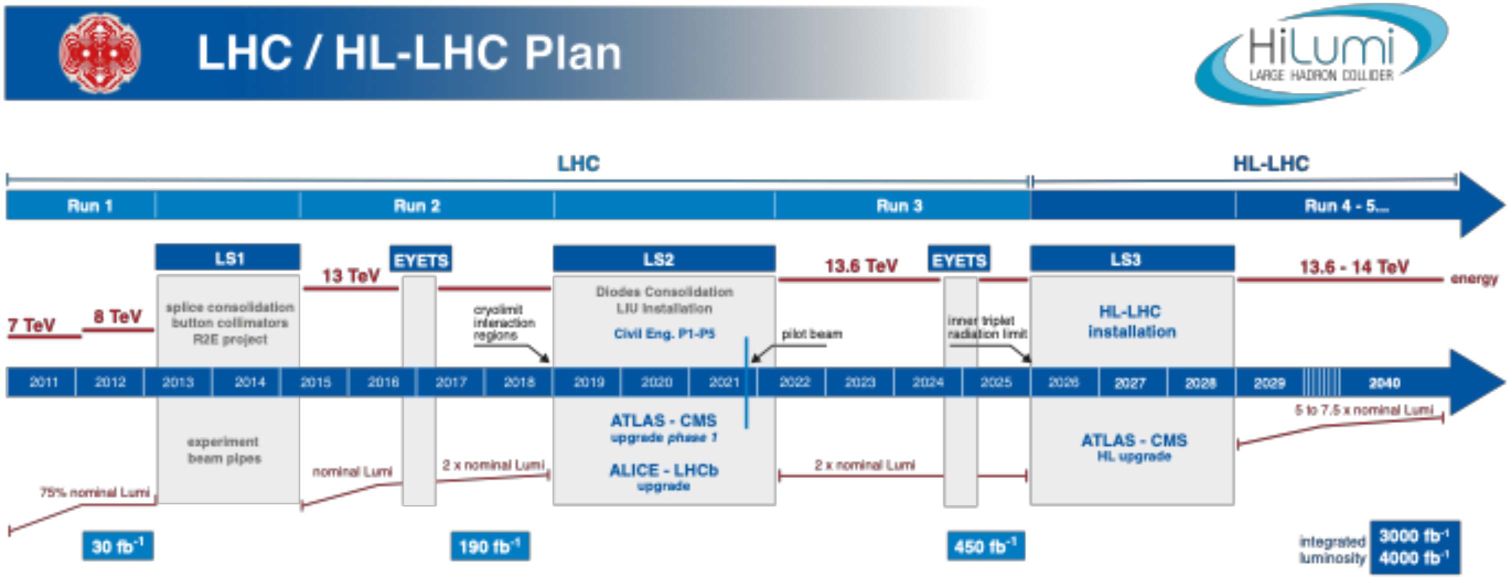
Radiation damage: Units

- Displacement damage
  - Due to non-ionizing energy loss (NIEL)
  - Fluence = number of particles per cm^2 traversing a material over a certain amount of time (typ. the lifetime of the experiment).
  - For silicon sensors the displacement damage is normalised to the damage level caused by 1 MeV neutrons.
  - Unit for fluence: 1 MeV neutron equivalents per cm^2 [n_{eq}/cm^2].

- Surface damage
  - Total Ionising Dose = energy deposited per unit mass of material as a result of ionisation.
  - Unit for TID:
    - Gy = J/Kg
    - 1 Gy = 100 rad

Why are we concerned about radiation?

- HEP detectors at collider experiments operate in a high particle flux environment.
- High luminosity is required to obtain large statistical samples to characterize rare processes.



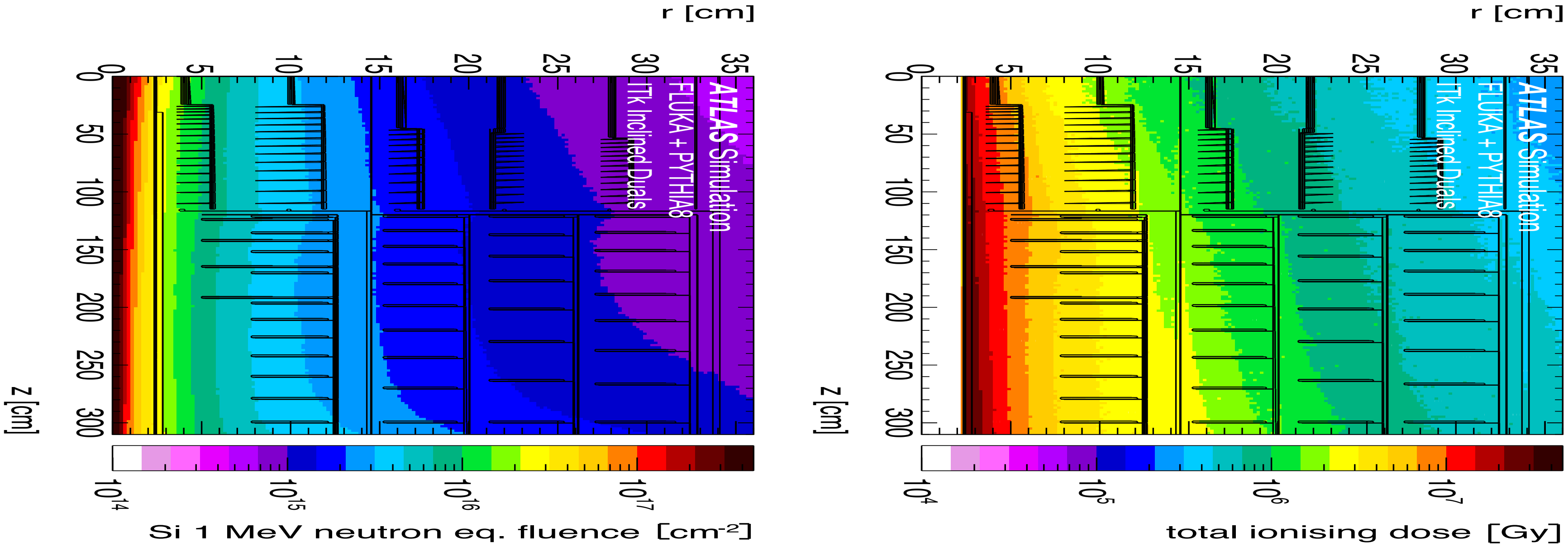
https://hilumilhc.web.cern.ch/content/hl-lhc-project

	Instantaneous peak luminosity	**Integrated luminosity**
LHC	2×10^{34} cm^{-2}s^{-1}	450 fb^{-1}
HL-LHC	$5 - 7.5 \times 10^{34}$ cm^{-2}s^{-1}	4000 fb^{-1}

Radiation levels

- Silicon detectors are used for vertexing and tracking close to the interaction point and are exposed to highest particle fluxes.

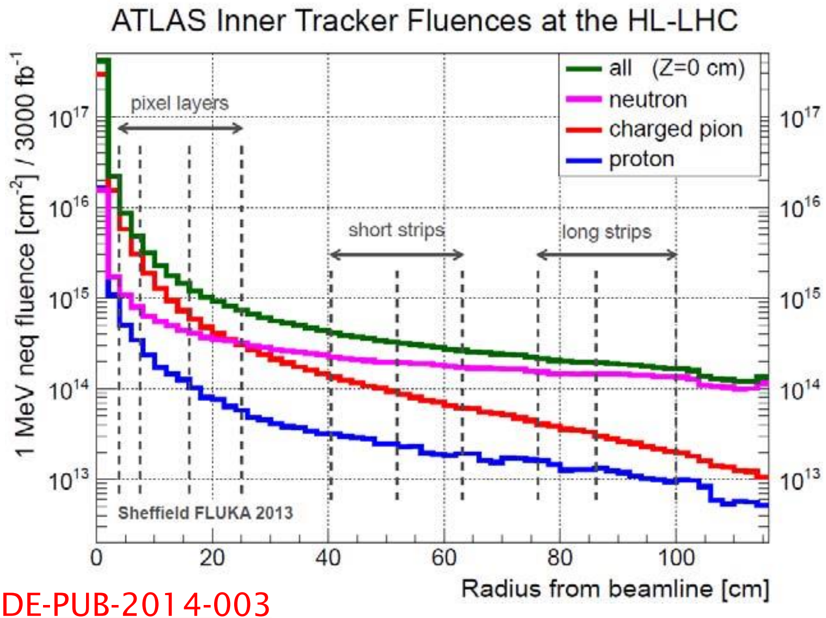
	Example: ATLAS innermost pixel layers	
	Fluence	**Total Ionising Dose**
@ LHC (300 fb^{-1})	2 x 10^{15} n_{eq}/cm^2	300 kGy
@ HL-LHC (4000 fb^{-1})	2 x 10^{16} n_{eq}/cm^2	10 MGy



The fluence and dose distributions for the ATLAS Pixel Detector at the HL-LHC. Left: 1 MeV neutron equivalent fluence. Right: Total ionising dose. The two plots are normalised to 4000 fb^{-1}. No safety factors are taken into account for this Figure. http://cdsweb.cern.ch/record/2285585

Radiation fields

- The particle flux at (HL-)LHC is made of charged and neutral particles, gamma and x-rays, neutrons.
- Close to the interaction point the charged hadron component dominates.
  - At 5 cm distance from the LHC IP 90:10 pions to neutrons ratio.
- Further out, the neutron component dominates.
  - Neutrons occur from backscattering in dense materials in the calorimeter.
  - At 30 cm distance from the LHC IP 50:50 pions to neutrons ratio.



ATL-UPGRADE-PUB-2014-003

Radiation damage: Cumulative effects

- Cumulative effects leading to a gradual degradation taking place through the experiment lifetime: displacement damage and surface damage.

- Displacement damage.
  - Damage to the silicon crystal by particles impinging on the lattice.
  - Caused by collisions with the nuclei in the lattice atoms → Non-Ionizing Energy Loss (NIEL).
  - Creates dislocations of the lattice atoms or more complex distortions of the crystal lattice.
- Surface damage.
  - Damage to silicon surfaces and interfaces, esp. $Si\text{-}SiO_2$.
  - Ionisation energy loss of impinging radiation.

A device sensitive to bulk or surface damage will exhibit failure in a radiation environment when the accumulated fluence or Total Ionising Dose (TID) has reached its tolerance limit.

Radiation damage: Single Event Effects

- Single Events Effects (SEE) are due to the energy deposited by one single particle in a circuit's sensitive node, and they can happen in any moment.

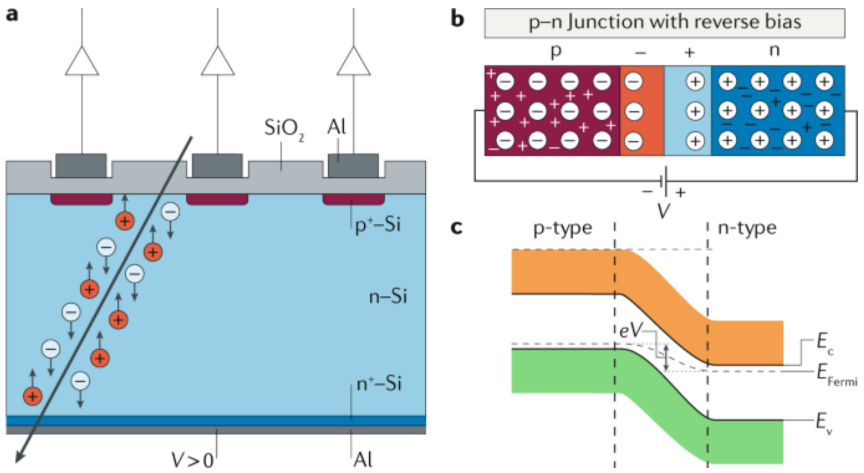
A device sensitive to SEE can exhibit failure at every moment since the beginning of its operation in a radiation environment.

In this lecture we discuss surface damage

Radiation damage to silicon detectors

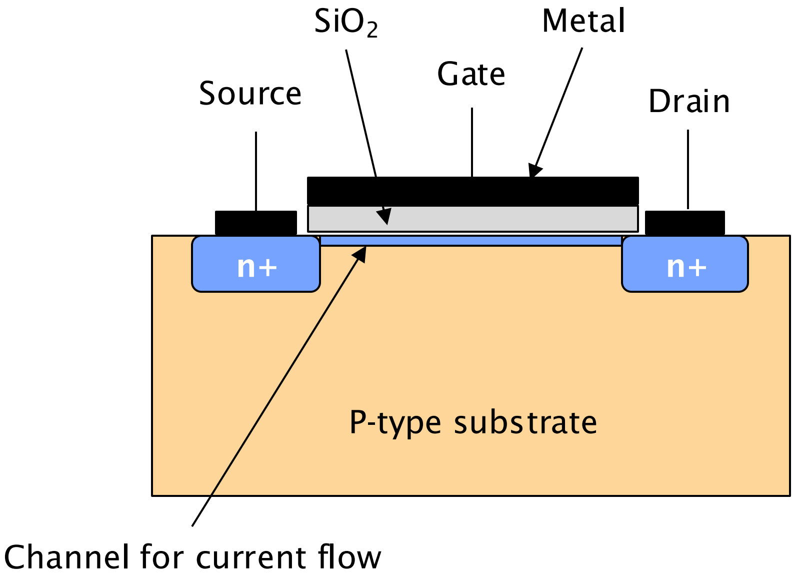
- Sensor:
  - Reverse biased pn-junction.
  - Charge collection in the sensor volume.

→Mostly affected by displacement damage but also by surface effects.



- Electronics:
  - Design and fabrication in deep-submicron CMOS technology.
  - Basic building element MOSFET transistor.
  - Current flowing in conduction channel a few nm below the Si-SiO$_2$ interface.

→ Affected by surface effects and SEE.



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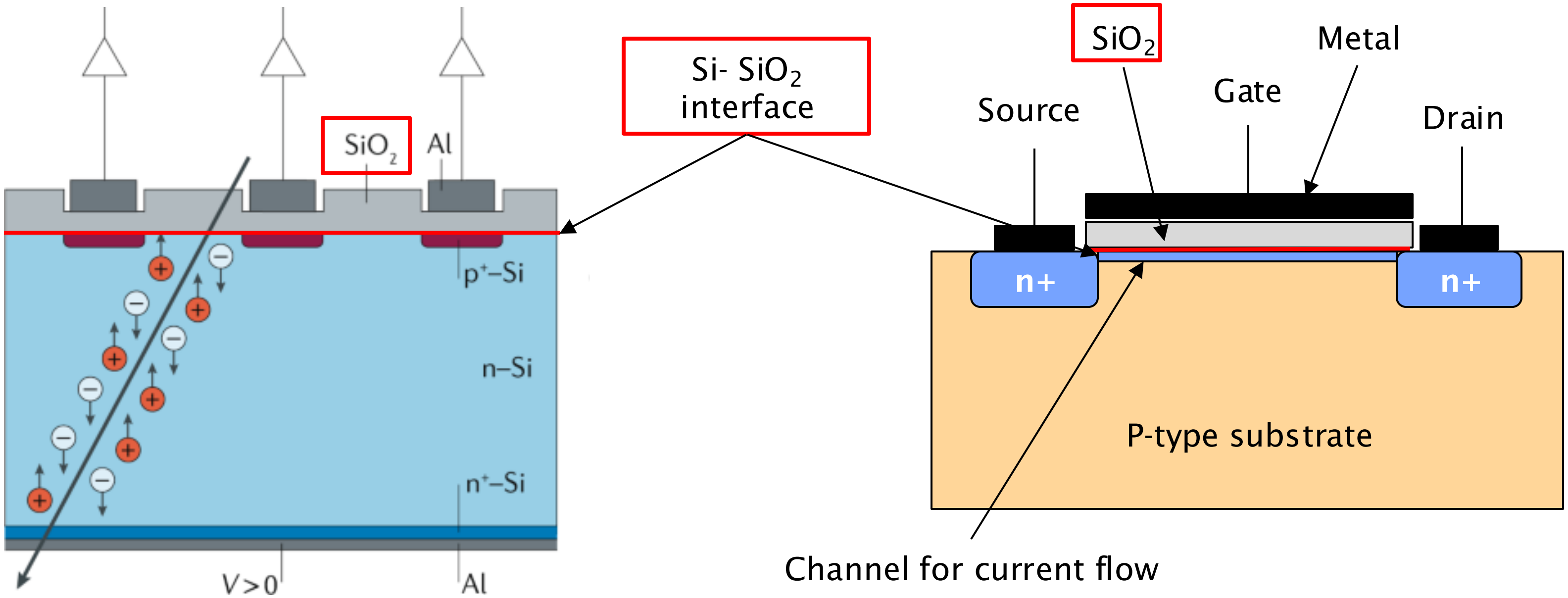
Surface damage

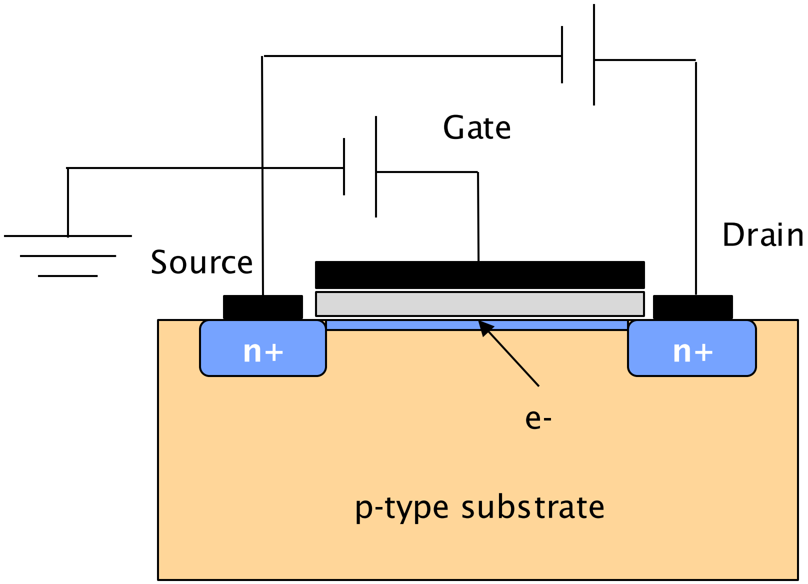
- Damage to the surface of silicon sensors and electronics, especially in the SiO_2 layer and at the Si-SiO_2 interface.
- SiO_2 is used as:
  - Passivation layer on silicon sensor.
  - Gate Oxide in MOSFET transistors.
  - Shallow Trench Isolation (STI) between transistors.
- Surface damage affects mostly electronics.



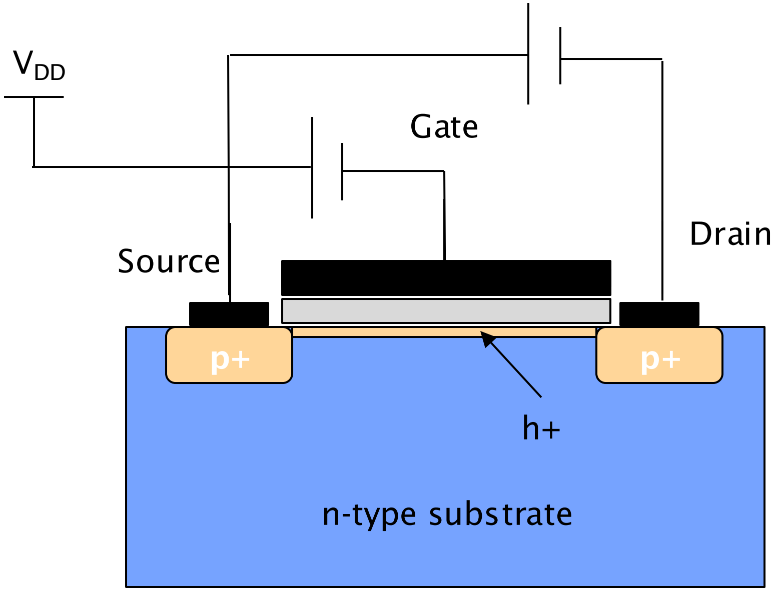
MOSFET transistors basics

1. A voltage is applied to the gate to induce a channel of free charge carriers below the Si-SiO_2 interface.
2. By applying a voltage on the drain, carriers can move → current.

- NMOS transistor:
  - $V_{GS} > 0$.
  - Electrons in the conduction channel.



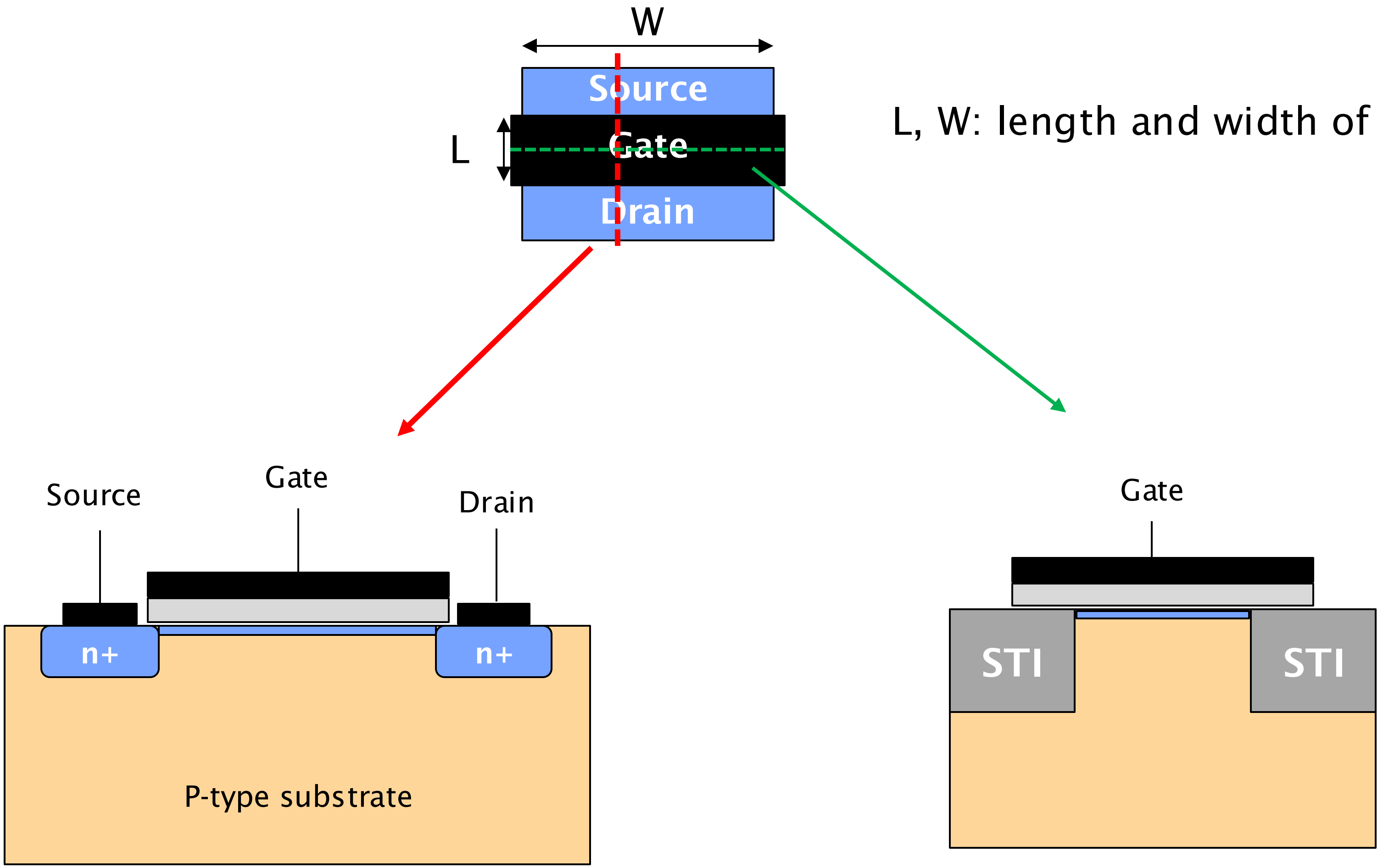
- PMOS transistor:
  - $V_{GS} < 0$.
  - Holes in the conduction channel.



Other transistor views

View from the top

L, W: length and width of the channel



Shallow Trench Isolation (STI)

Damage to SiO_2

- Radiation causes ionisation and/or dislocation of lattice atoms in SiO_2.

- Damage impact from ionisation is more severe in SiO_2 → it creates charged defect states in the oxide and at the interface with the silicon that impact transistor's operational parameters.
  - High electric fields can exist in the oxide of MOS transistors.
  - Charge carriers generated by ionisation are separated.
  - Holes have a mobility 10^6 times lower than electron mobility in SiO_2 (large hole capture cross section by shallow levels in the silicon oxide).

- NIEL damage does not get electrically active in the SiO_2.
  - Also, the substrate of integrated circuits is highly doped (i.e. low resistivity) which reduces the sensitivity to displacement damage.

Defects in SiO_2 and Si-SiO_2 interface

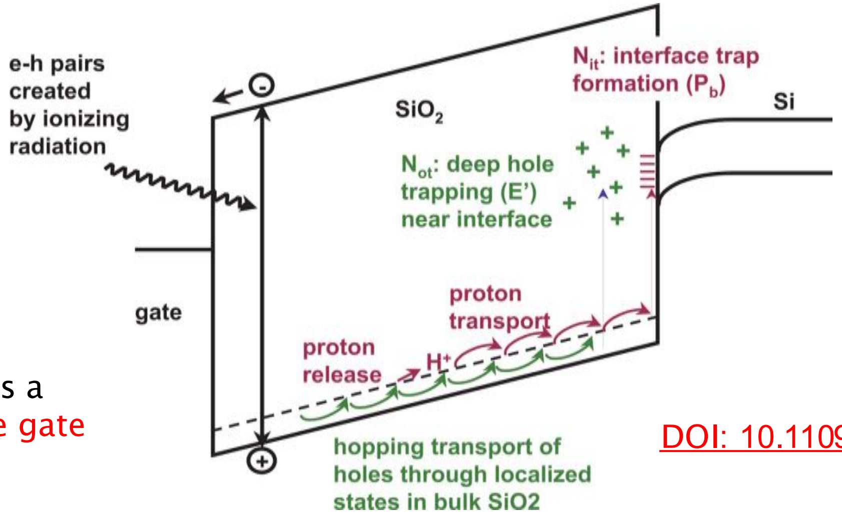
- Defects are present in the SiO_2 and at the Si-SiO_2 interface that introduce localised energy states in the bandgap of the material and act as traps for charge carriers.

- In the SiO_2 defects are due to a precursor that is not active in its normal condition but is activated by radiation and becomes a trap for positive charges.
  - This precursor is the physical origin of oxide traps.
  - Oxide traps are donor like, i.e. positive.

- At the Si-SiO_2 interface defects are due to the abrupt transition between a crystalline material (Si) and an amorphous one (SiO_2) that interrupts the crystalline structure of silicon.
  - Interface states are located at the interface or a few angstrom from it.
  - Responsible for interface traps.
  - Interface traps can be both donor or acceptor like, i.e. their net charge will positive or negative according their position wrt. the Fermi level.

Oxide charges

- The incoming radiation generates e-/h+ pairs.
- After a few ps a fraction of the e-/h+ pair has recombined, the other pairs are separated by the E-field and start to drift in opposite directions.
  - The fraction of non-recombined pairs depends on the type of incident radiation, material, and applied electric field.
- Assuming a positive voltage on the gate.
  - The e- drift to the gate and exit the oxide in a few ps (higher mobility).
  - The h+ will drift (slowly) towards the Si-SiO_2 interface.

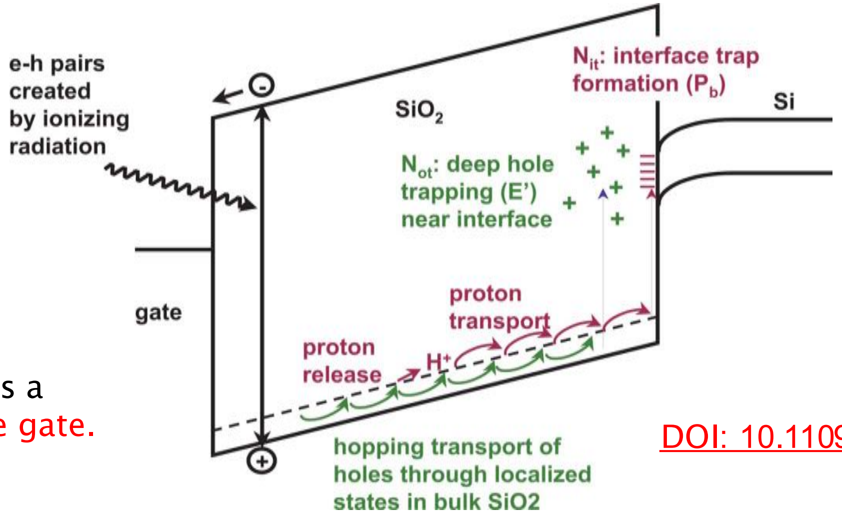


This figure assumes a positive bias on the gate (worse condition).

DOI: 10.1109/TNS.2008.2001040

Oxide charges

- The h+ move with a dispersive transport phenomena called “polaron hopping”.
  - Being slow h+ are self-trapped, i.e. they are localised in the lattice distortion that they generate → polaron.
  - The polaron moves by hopping from one lattice location to the next → increased holes effective mass, lower mobility.
  - Higher T and E field = faster transport.
  - Dependent on oxide thickness.
  - Long time scales compared to the charge injection.



This figure assumes a positive bias on the gate.

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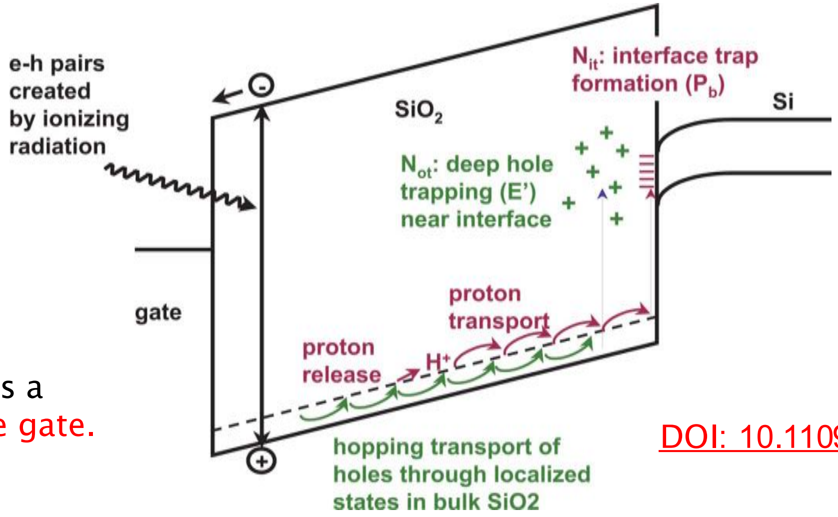
Oxide charges

- The h+ can be trapped in defects presents in the SiO_2 and in oxygen vacancies close to the interface (deep hole trapping) giving origin to a fixed positive charge.
  - The fraction of trapped holes depends on the mean trap density, their hole capture cross-section, and the width of their distribution.



This figure assumes a positive bias on the gate.

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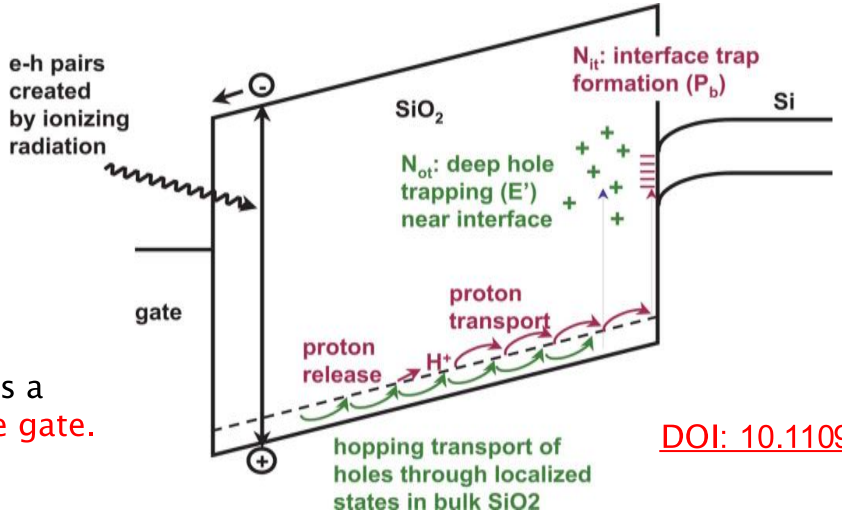
Interface states

- Because of irradiation, the density of interface traps increases by orders of magnitude.
- Impurity hydrogen ions are released from the lattice by hole hopping.
- These ions move toward the Si-SiO$_2$ interface where they give origin to new interface states that serve as traps.
- Creation of interface states is a slower process than oxide charge formation due to the lower mobility of the hydrogen ions.



This figure assumes a positive bias on the gate.

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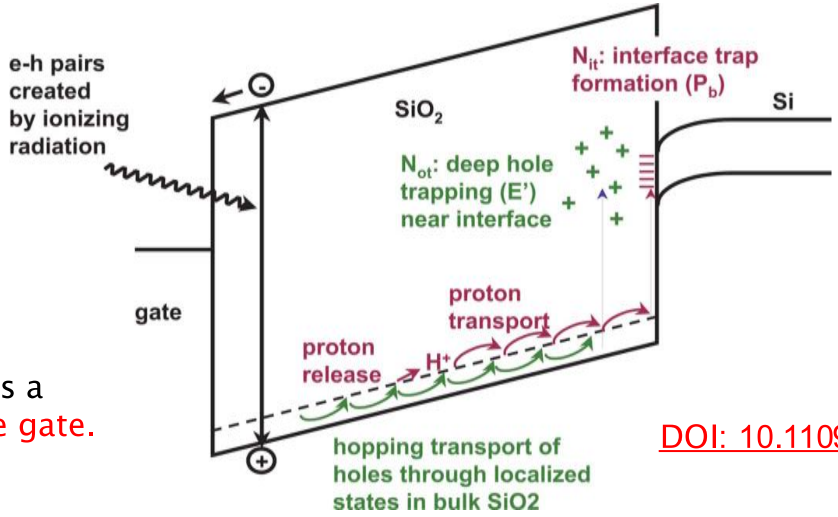
Interface states

- The radiation-induced traps have energy levels in the bandgap.
    - Traps above midgap = acceptors.
    - Traps below midgap = donors.

- For NMOS under positive bias, interface traps are negatively charged.
- For PMOS under negative bias, interface traps are positively charged.



This figure assumes a positive bias on the gate.

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Annealing

- Annealing happens through two mechanisms whereby electrons recombine with the trapped holes.

- Electron tunnelling from the silicon to the oxide traps.
  - Strongly dependent on the E-field in the oxide and on the spatial distribution of traps, which in turn depends on the fabrication process.

- Thermal emission of electrons from the oxide valence band into the trap levels.
  - Strong dependence on temperature.
  - Traps need to be close to the valence band.

- Annealing can start already during irradiation depending on dose rate, temperature during irradiation, and the electric field in the oxide, but it is a slow process.
  - Complete annealing can take many months.

TID technology dependence

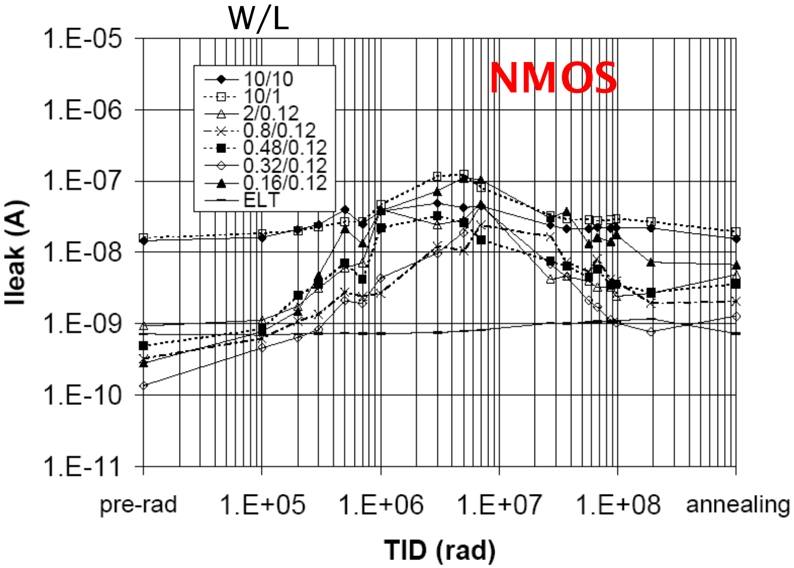
- The scaling of CMOS technologies and reduction of MOSFET gate oxide thickness has greatly improved the radiation hardness of integrated circuits for use at high luminosity experiments.
  - Thick oxides however still exists, e.g shallow trench isolation oxides, field oxides.

- TID damage is greatly influenced by the oxide growth process and the level of initial impurities.
  - Some technologies are more affected than others, even within the same node, i.e. same gate oxide thickness.
  - Even the technology from a specific foundry can have different radiation performance depending on the production sites.

In the following, I will discuss TID effects on the 130 nm CMOS technology used for various ATLAS and CMS upgrades.

Leakage current

- Leakage current in MOSFET transistors is defined as the current that flows through the device for $V_{GS} = 0$.
- A change in leakage current is observed for NMOS transistors.
  - Increase in current up to a TID of a few Mrad, followed by a decrease towards the pre-irradiation value.
  - Peak at a few Mrad.
- No change is observed in PMOS transistors.



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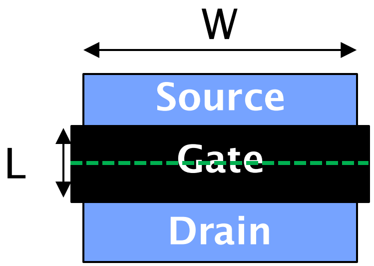
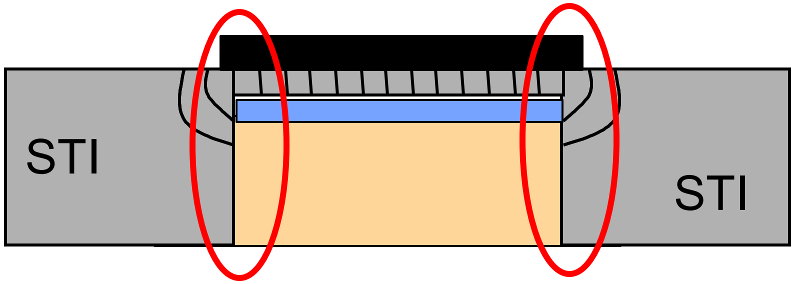
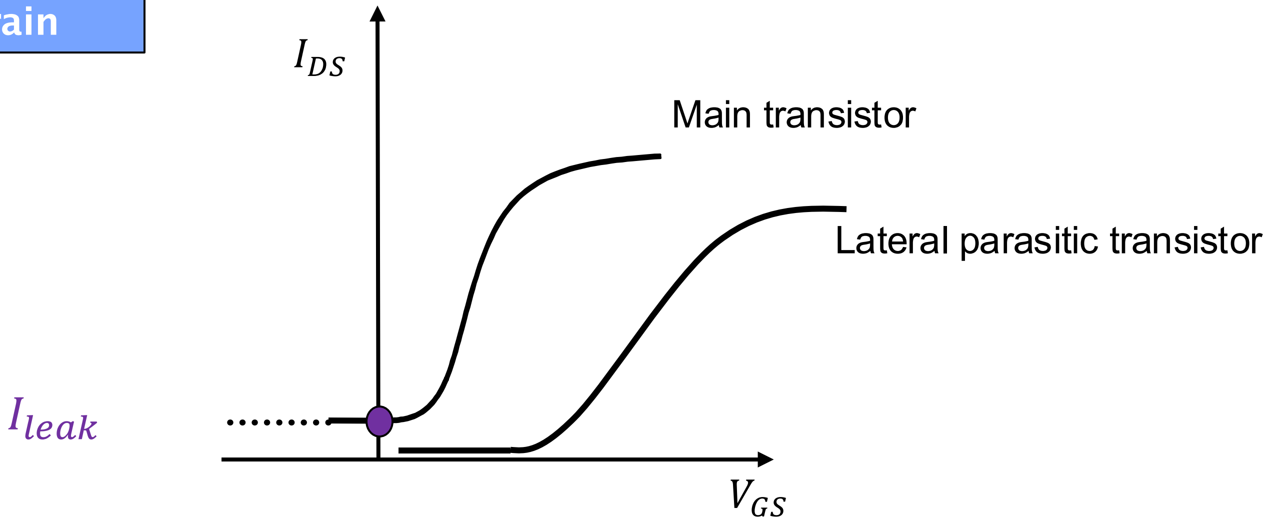
Edge effects: NMOS

- Parasitic transistors exist at the edges of the transistor.
- Their gate oxide is the STI.

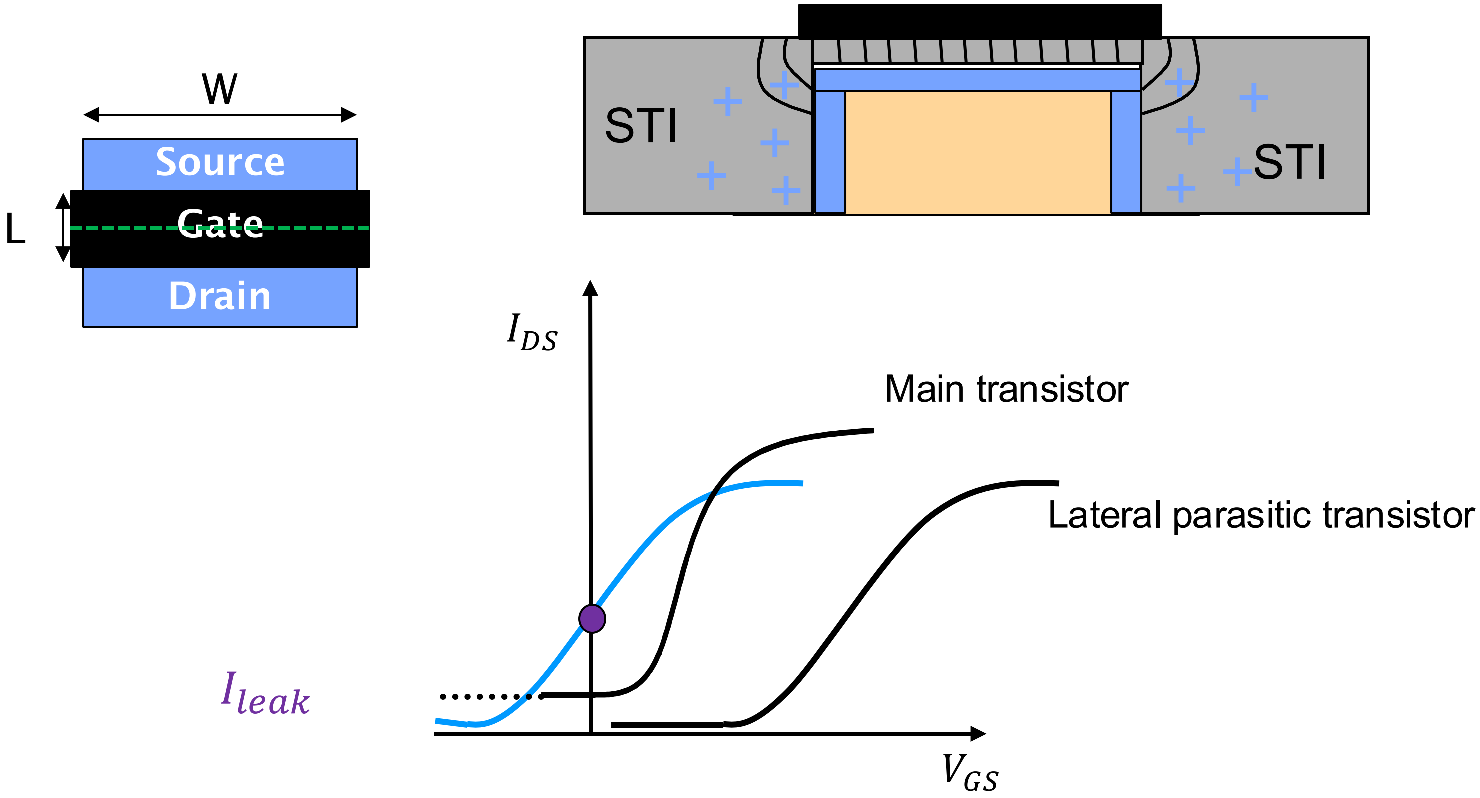






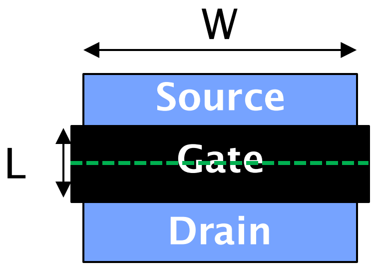
Edge effects: NMOS

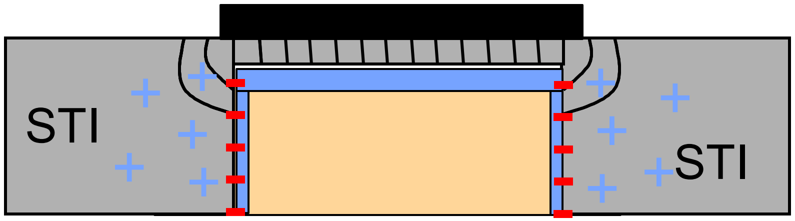
- Positive trapped charges quickly build up in the STI at the edge of the transistor.
- These open a conductive channel through which current can flow between drain and source → parasitic lateral transistor switches on.
- The leakage current increases.

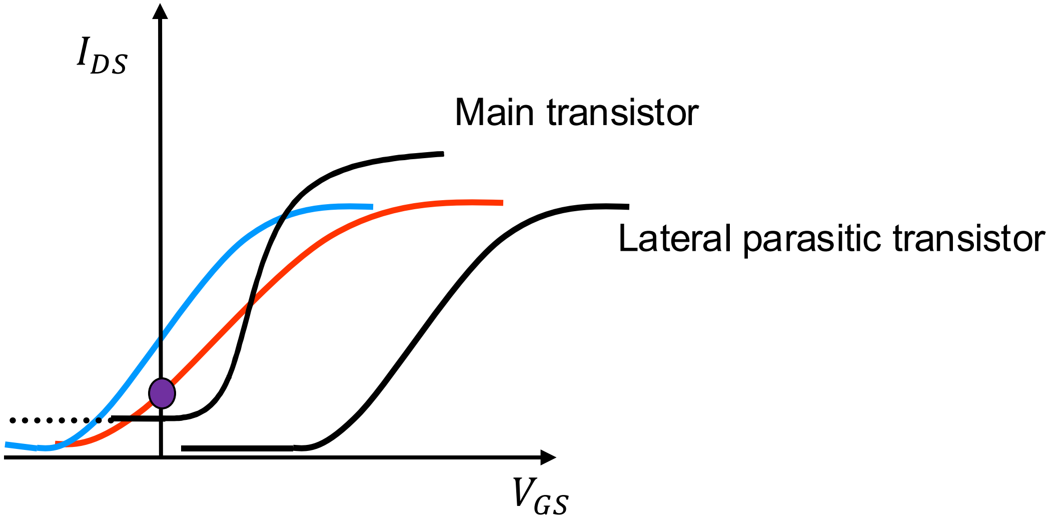


Edge effects: NMOS

- At higher TID, due to the slower formation process, interface states start to build up.
- These are negatively charged for NMOS transistor and counteract the effect of positive charges trapped in the STI.
- The leakage current decreases.

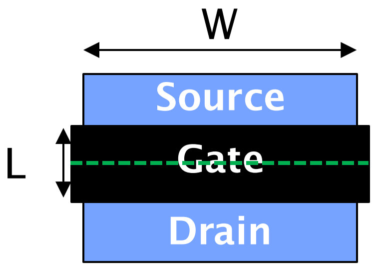


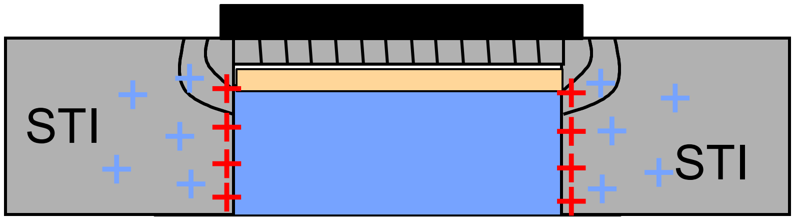


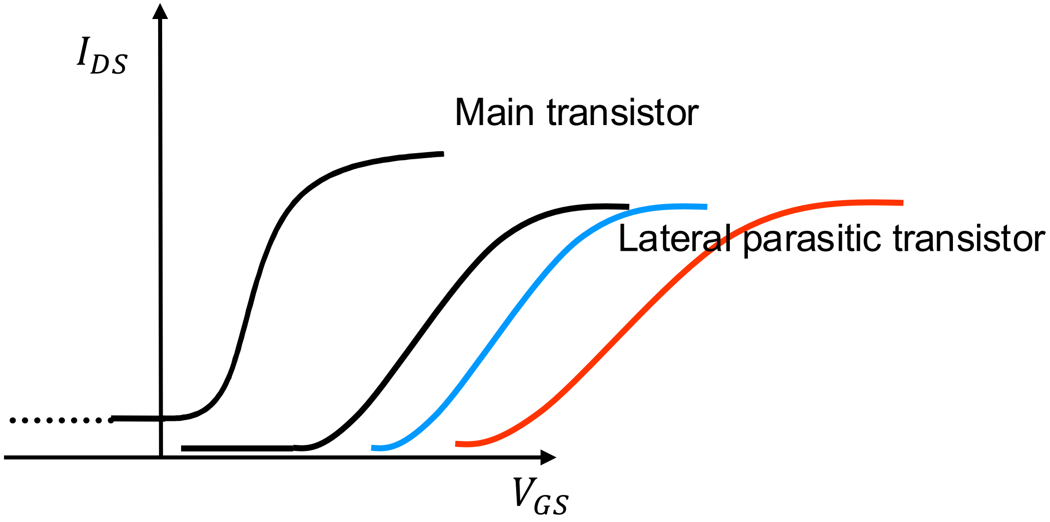


Edge effects: PMOS

- In PMOS transistors, both oxide charges and interface states are positively charged.
- They repel further the holes from the side of the transistor → the parasitic transistors do not switch on.
- The leakage current does not change.



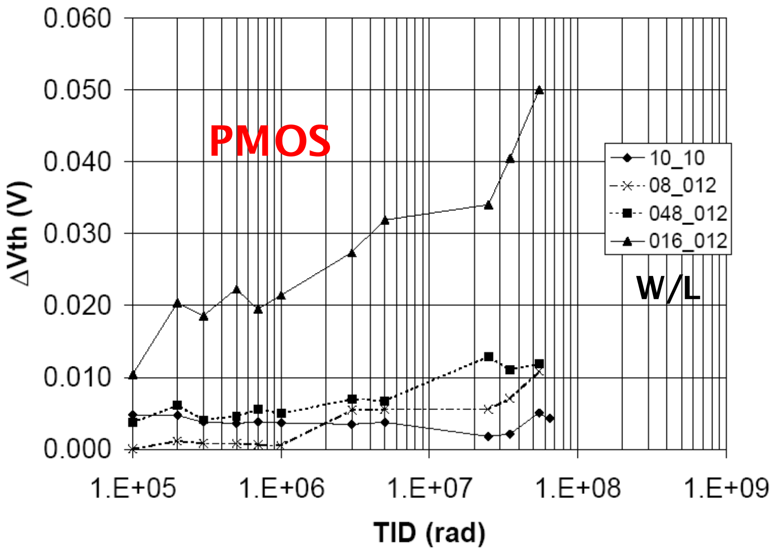


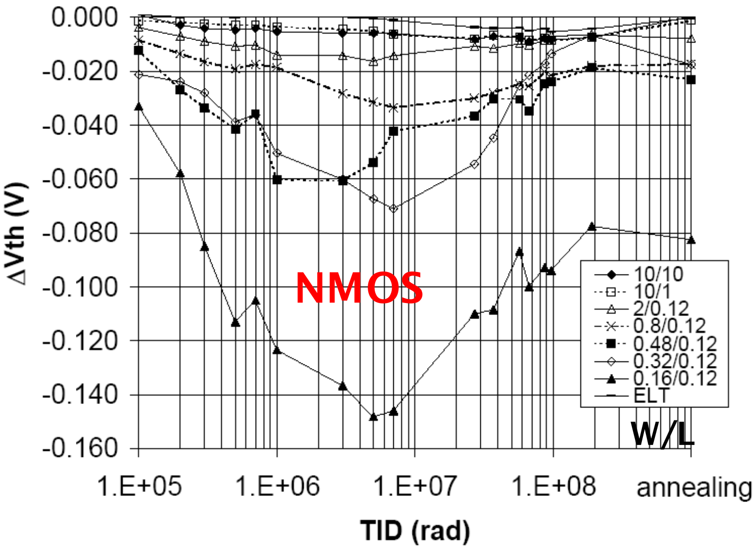


Threshold voltage shift

- A threshold shift is observed for narrow transistors both NMOS and PMOS.

- For narrow transistors, i.e. small W, the net charge at the transistor edges influences the electric field in the main device → narrow channel effect.
  - Observed in deep-submicron CMOS technologies as a decrease of V_{th} with transistor width.





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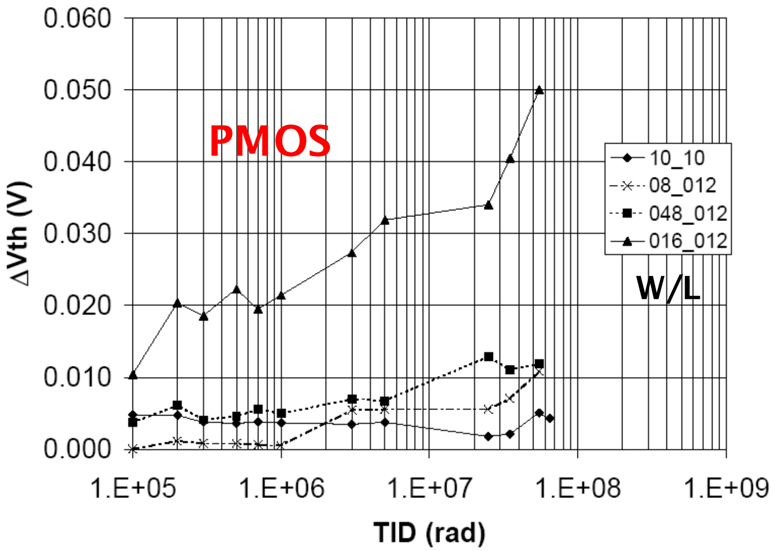
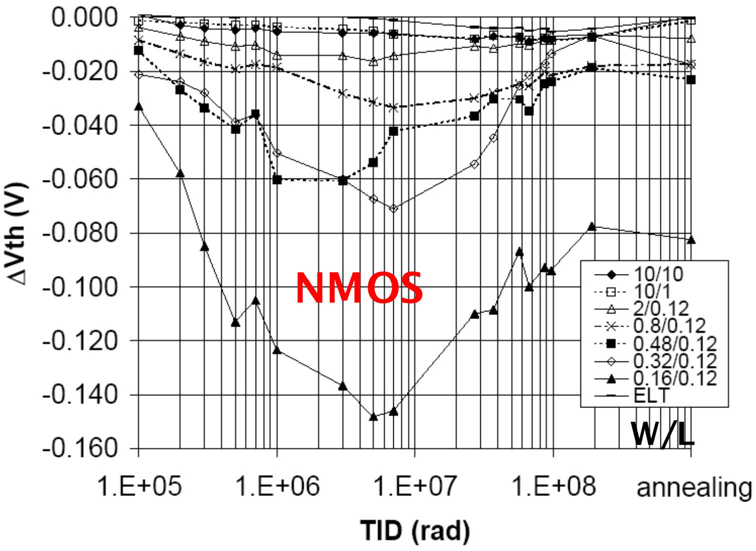
RINCE

- Due to the positive oxide charge trapped in the STI oxide, the narrow channel effect decreases/increases the V_{th} of NMOS/PMOS transistors.
- For NMOS, the negatively charged interface states counteract the effect of the positive oxide charge → rebound with peak at a few Mrad.
- For PMOS, the positively charged interface states add to the effect of the positive oxide charge → increase of the V_{th} slope.

Radiation Induced Narrow Channel Effect (RINCE)

10.1109/TNS.2005.860698





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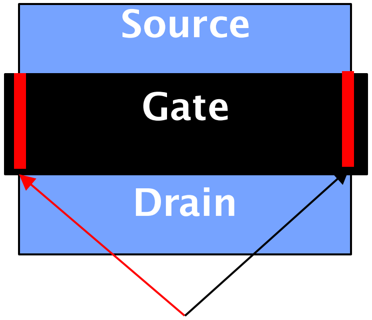
Hardening by layout techniques

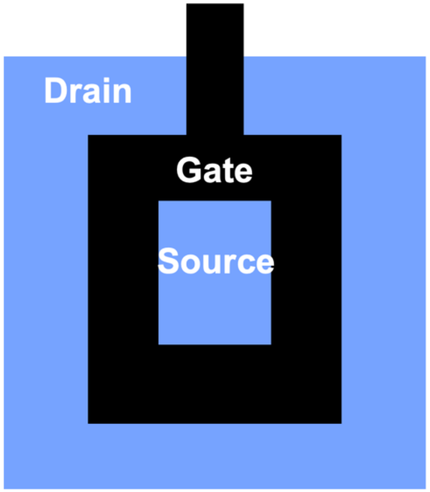
- Enclosed layout transistor can be used to cut leakage current paths at the edge of the transistors.
  - For the same W/L, ELT use more space → Loss of logic density.
  - Only really feasible for the analogue part of the circuit.
  - Lack of a commercial digital library for digital design.

Linear transistor layout



Leakage current paths

Enclosed transistor layout (ELT)



Outline

- Silicon detectors in HEP

- Radiation environment at collider experiments

- Surface damage to electronics

- **Examples of radiation hard detectors**
  - **ATLAS IBL**
  - ATLAS ITk strip detector

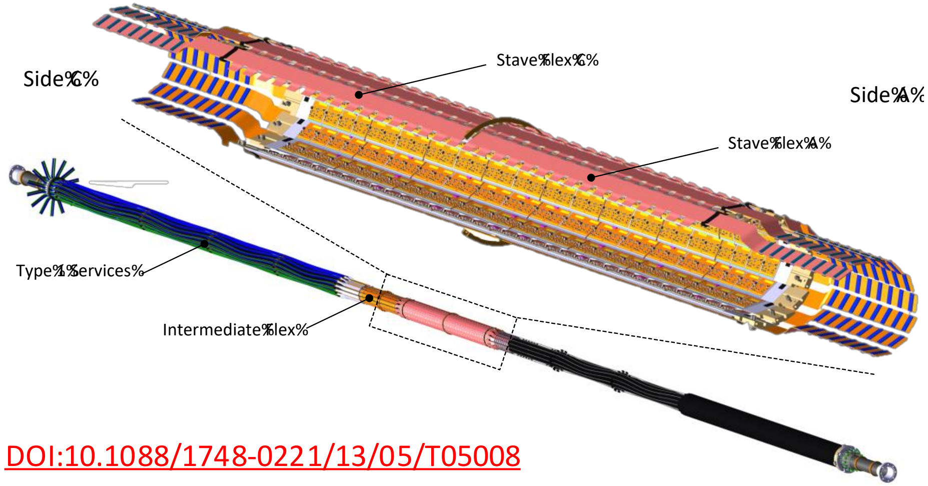
- Conclusion

TID effects on ATLAS IBL operation

- The ATLAS Insertable B-Layer is the innermost layer of the ATLAS tracking system at the LHC.
  - New layer inserted in the ATLAS Inner Detector during the LHS LS1 (2013-14).
  - Closest layer to IP, radius = 33.5 mm (beam pipe r = 23.5 mm).

- The IBL sensors and front-end electronics must cope with radiation doses of $5\times10^{15}\ n_{eq}/cm^2$ NIEL and 250 MRad TID during the LHC Phase-I.

- New front-end chip in 130 nm CMOS technology → FE-I4.



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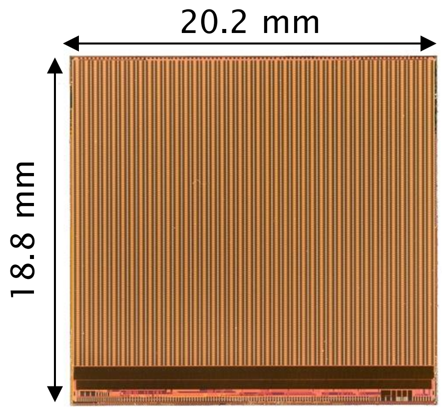
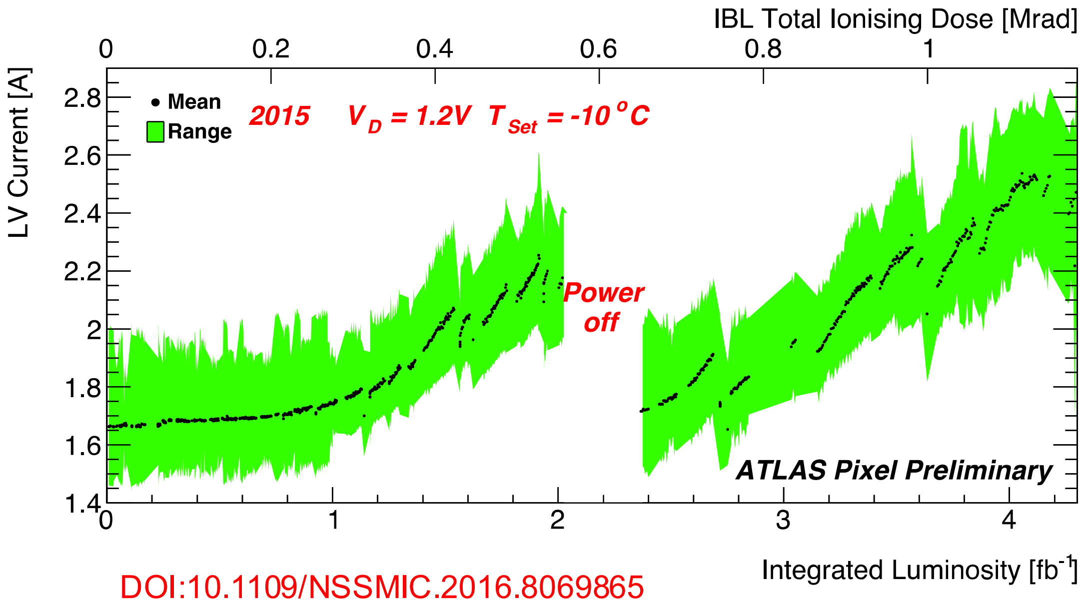


TID effects on ATLAS IBL operation

- The current of the FE-I4 chip (LV current) was stable at a value of 1.6–1.7A (for a four-chip unit) until the middle of September 2015.
- The current then started to rise up significantly → consequence of I_{leak} increase in transistors.
    - Between September to November 2015 the current increase was more than 0.2 A even within a single LHC fill, depending on the luminosity and the duration of the fill.
- This led to a temperature increase of the modules.
    - Increased IBL distortion.
    - Drifting module calibration.



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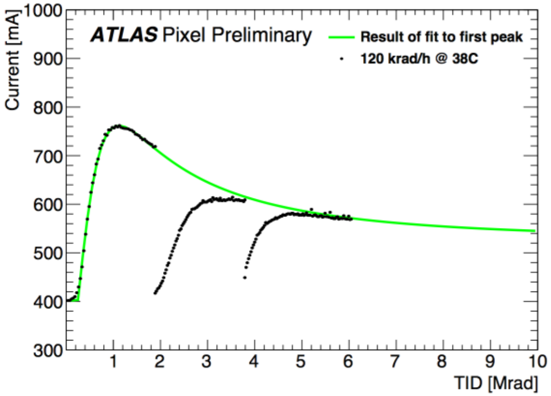
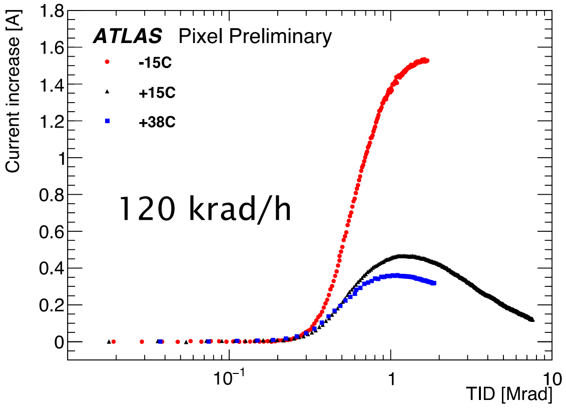
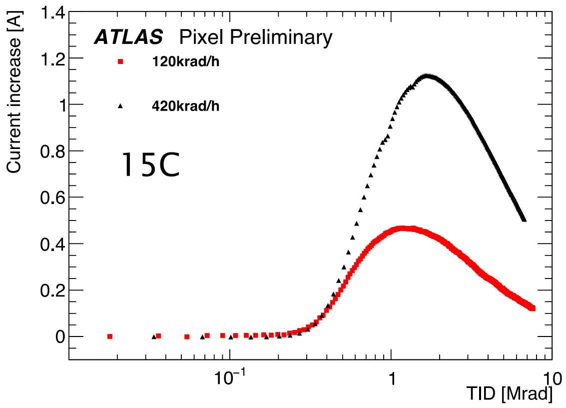
Studies of IBL current increase

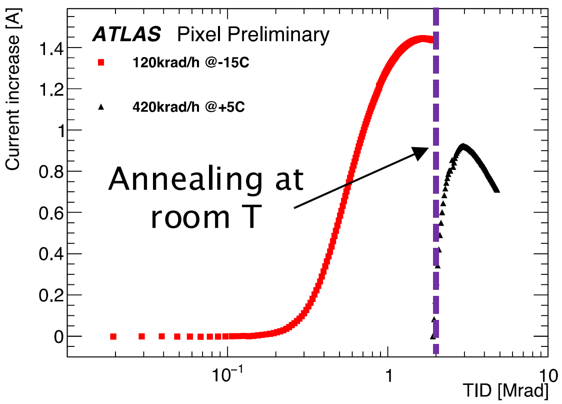
- X-rays irradiation were performed on IBL modules in the lab at different dose rates and temperatures.



- Important findings:
  - At a given temperature and dose rate, the current always approaches a boundary after annealing periods and re-irradiation.
  - At a given dose rate, the LV current increase is stronger at lower temperatures.
  - At a given temperature, the LV current increase is stronger at higher dose rates.
  - By increasing the operational temperature of the chip during irradiation the increase of the LV current can be kept below the boundary.







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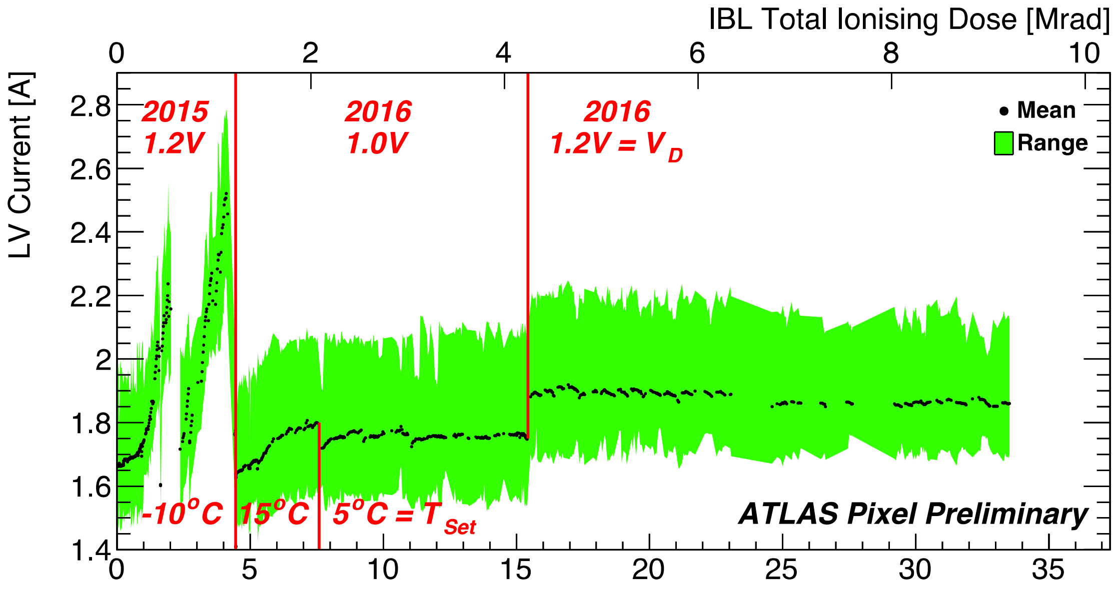
IBL mitigation strategy

- Based on experience in 2015 and lab measurements, the IBL was run at higher temperatures and lower digital voltage for part of 2016.
- The digital voltage was increased back to 1.2V after 5 Mrad, well beyond the peak of current increase.



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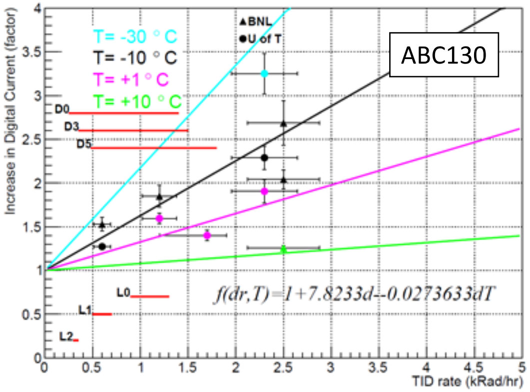
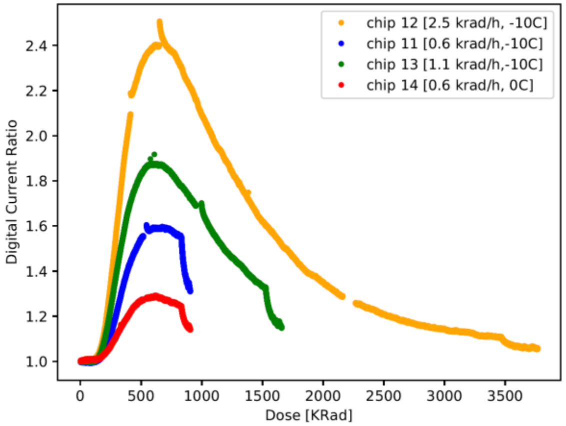
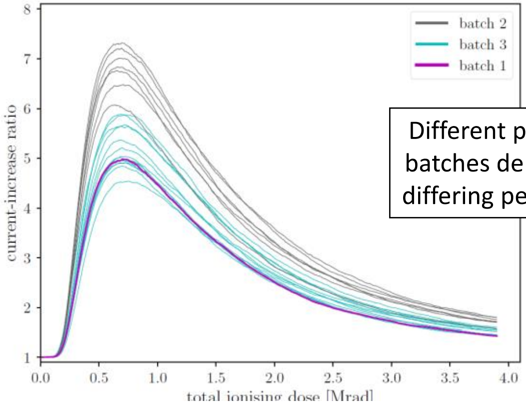
TID mitigation measures for the ATLAS ITk

- The ITk is the new ATLAS Inner Tracker system for the HL-LHC.
  - All-silicon detector made of pixels and strips layers.

- The readout chip for the strips detector, the ABCStar, is designed in the same 130 nm CMOS process as the FE-I4.
  - Max TID at ITk for the ABCStar = 60-70 Mrad.
  - Enclosed layout transistors are used in the analogue part of the chip.
  - Extensive irradiation campaigns to study current increase versus temperature and dose rate.
    - Slow dose rate to estimate current increase during operation, high dose rate studies to gather information on larger samples of chips.



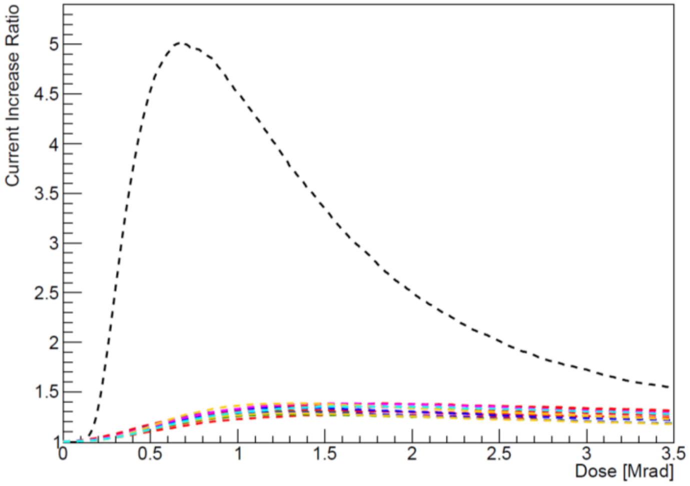


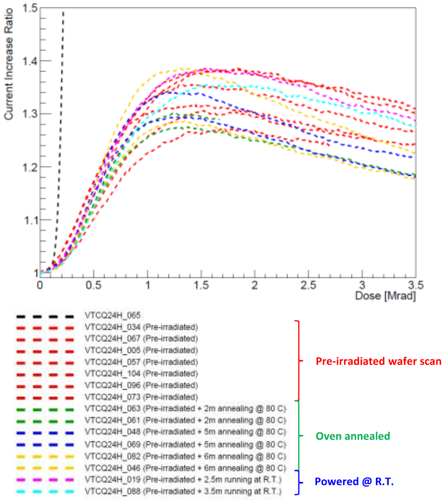


Different production batches demonstrate differing peak heights

ATLAS ITk TID consequences and mitigations

- Consequences of higher current for the operation:
  - Cable plant and cooling system requirements need to be adapted.
  - Implications on system stability/alignment during runs.
  - Voltage regulators cannot support more voltage drop on cables.
  - Higher transients from module switch off.
  - Un-predictable wafer-by-wafer and batch-by-batch variations.
  - Thermo-electric models based on very low statistics.
- Mitigation: pre-irradiation of all ABCStar chips to be used in the experiment.
  - After pre-irradiation and annealing, current peak is lower.





TID effects in CMOS 65 nm and 28 nm

- TID effects become more complex in smaller technology nodes.
- Thinner gate oxide is beneficial however…
  - Thick oxides still present.
  - Effect from other structures, such as gate spacers (nitride).
  - Radiation Induced Short Channel Effect (RISCE).

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Summary and final considerations

- Radiation hardness is one of the most important requirements for operation of silicon tracking systems at high luminosity collider experiments.

- Development of radiation hard sensors and electronics is carried out by large experimental collaborations and takes many years of development.

- Work on the silicon technologies is supported by modelling and simulations.

- Silicon detectors exist that will be able to cope with the HL-LHC environment, i.e. up to $2 \times 10^{16}\ n_{eq}/cm^2$ and 1 Grad.

- For future hadron colliders (e.g. FCC hh), radiation levels will increase to $6 \times 10^{17}\ n_{eq}/cm^2$ and 40 Grad → Completely new challenge; Will silicon still work? Will we need new materials? Which ones? …