Rivelatori e Apparati

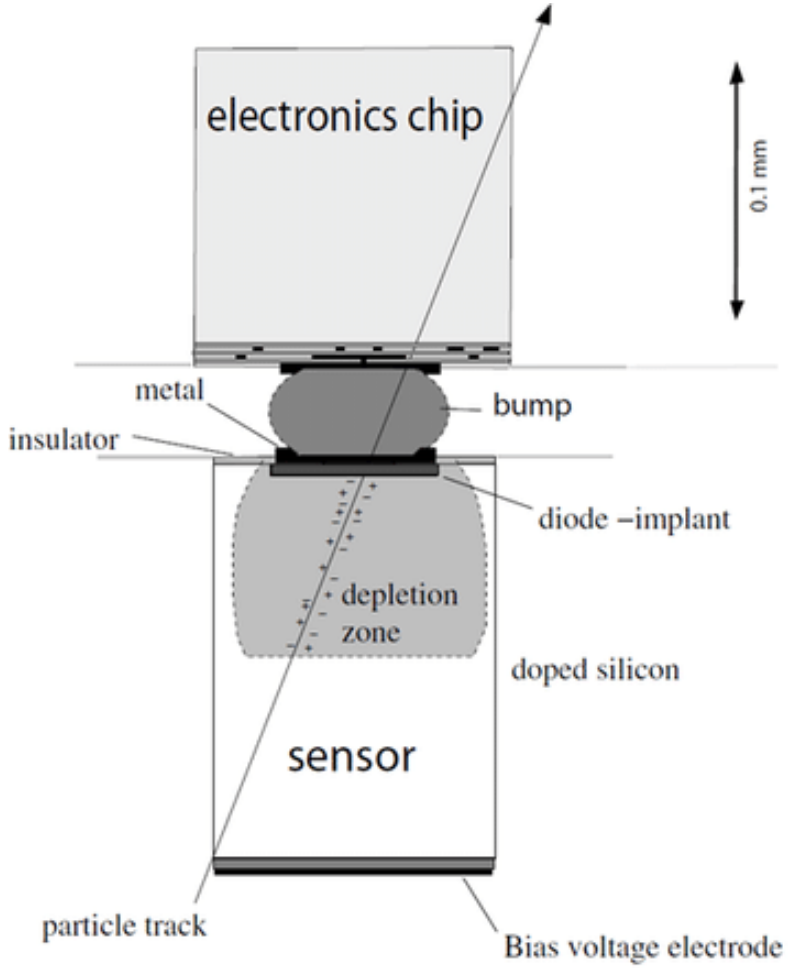
Slides_8 – MAPS, LGAD, SiPM, Calorimetri

Differenze tra silicio di chip e di sensore

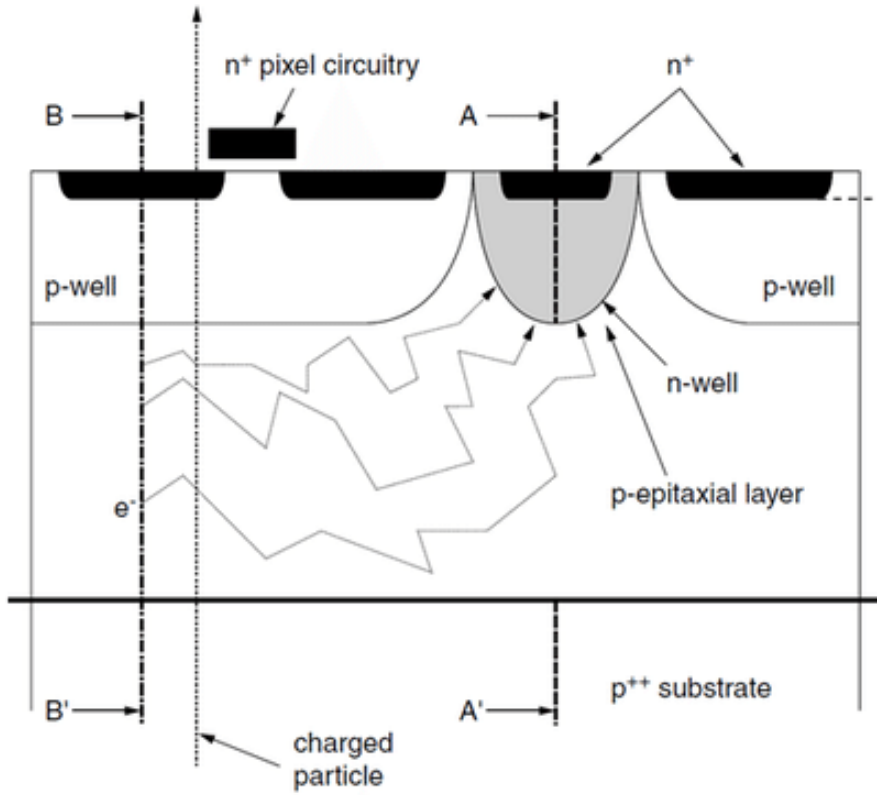
- Il silicio del sensore deve essere ad alta resistività per favorire lo svuotamento e la raccolta veloce delle cariche (kOhm x cm)
- Il silicio del chip di readout deve essere a bassa resistività (Ohm x cm), perché' tutta la tecnologia CMOS commerciale è stata sviluppata in silicio a bassa resistività per ridurre i costi

- Sono stati però esplorati due approcci per unire le funzionalità:
  1. Privilegiare il sensore (come DEPFET project) applicando semplici funzioni logiche (amplificatore e indirizzamento) su alta resistività.
     - Segnale ottimale – pochissima elaborazione
  2. L'elettronica guida lo sviluppo del sensore: sottile strato epitassiale a bassa resistivita'
     - Ottimale per una logica CMOS commerciale ma non si puo' svuotare piu' di tanto – raccolta in piu' di 100 ns

Monolithic Active Pixel Sensors (MAPS)

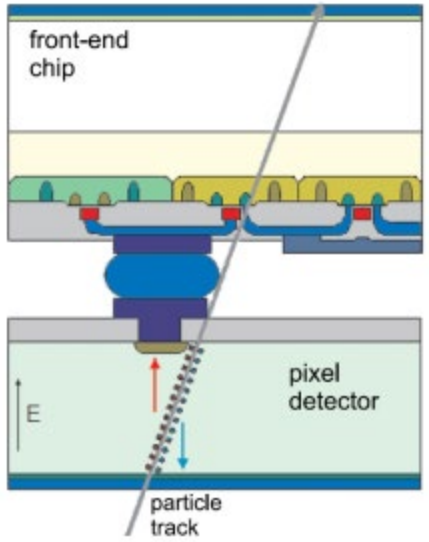


(a)

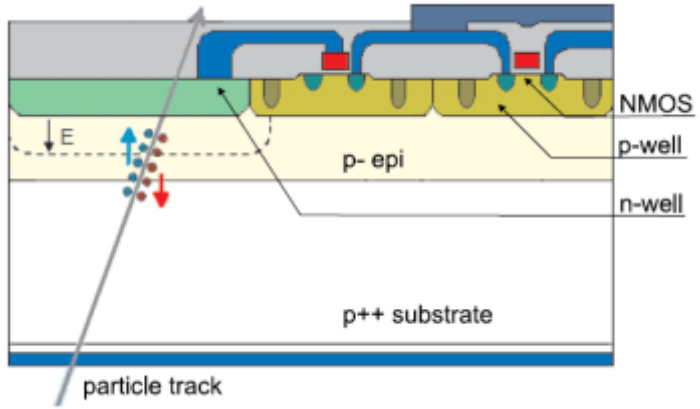


(b)

Hybrid Pixel Detectors



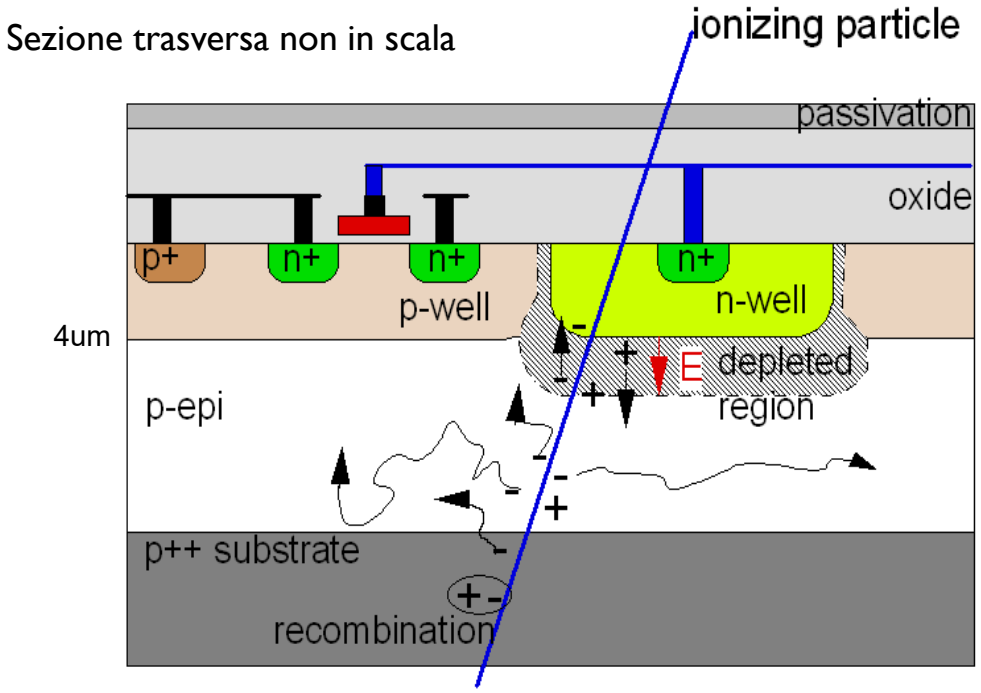
Monolithic Pixels



La tecnologia MAPS

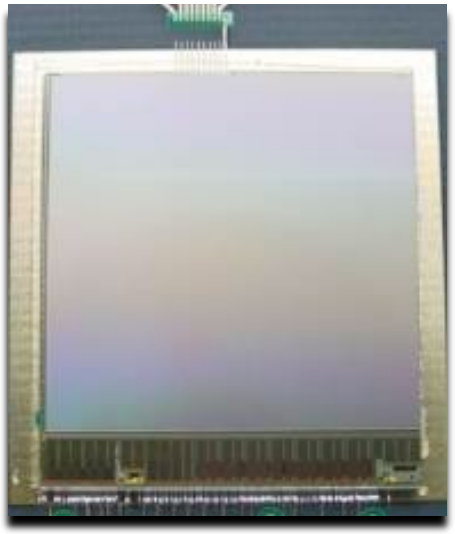
Volume sensibile e logica CMOS di prima elaborazione del segnale nello stesso cristallo di silicio

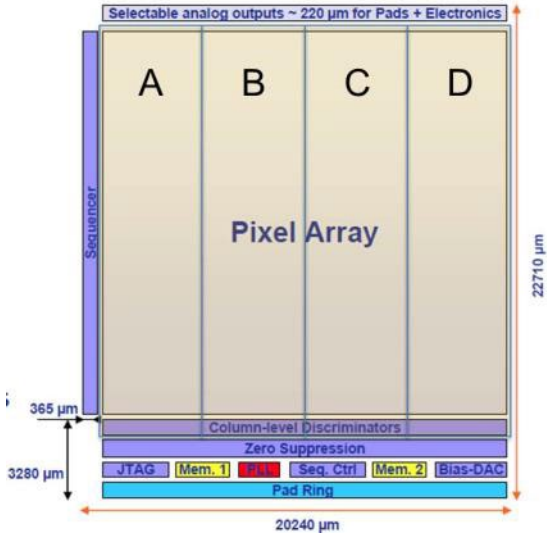
Sezione trasversa non in scala

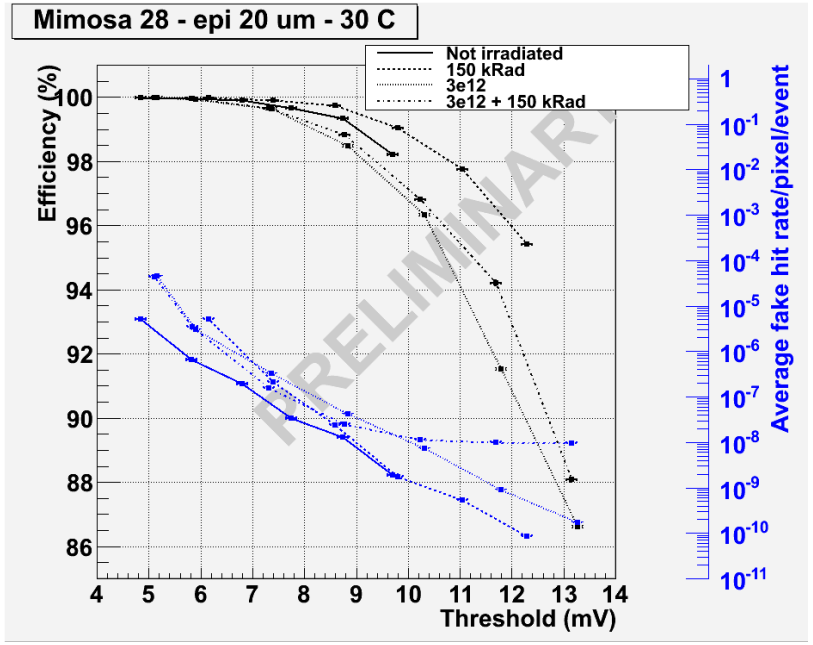


- Monolithic Active Pixel Sensor
- Tecnologia industriale standard CMOS (ma inizialmente solo nmos)
- **Room temperature** operation
- Sensore e processazione del segnale integrati nello stesso silicio
- Il segnale e' creato nell'epitassiale (tipicamente ~10-15 µm) a basso drogaggio → segnale di un MIP limitato a <1000 elettroni
- La raccolta di carica avviene soprattutto per diffusione termica (lenta, ~100 ns), anche grazie ai confini "riflettenti reflective boundaries at p-well and substrate.
- Epitassiali ad alta resistivita' per ottenere zone svuotate piu' spesse → raccolta della carica piu' efficiente, piu' tollerante alle radiazioni
- 100% fill-factor

MAPS *Ultimate-2* Sensor (2013)







3rd generation sensor developed for the PXL detector by the PICSEL group of IPHC,Strasbourg, optimized for the STAR environment

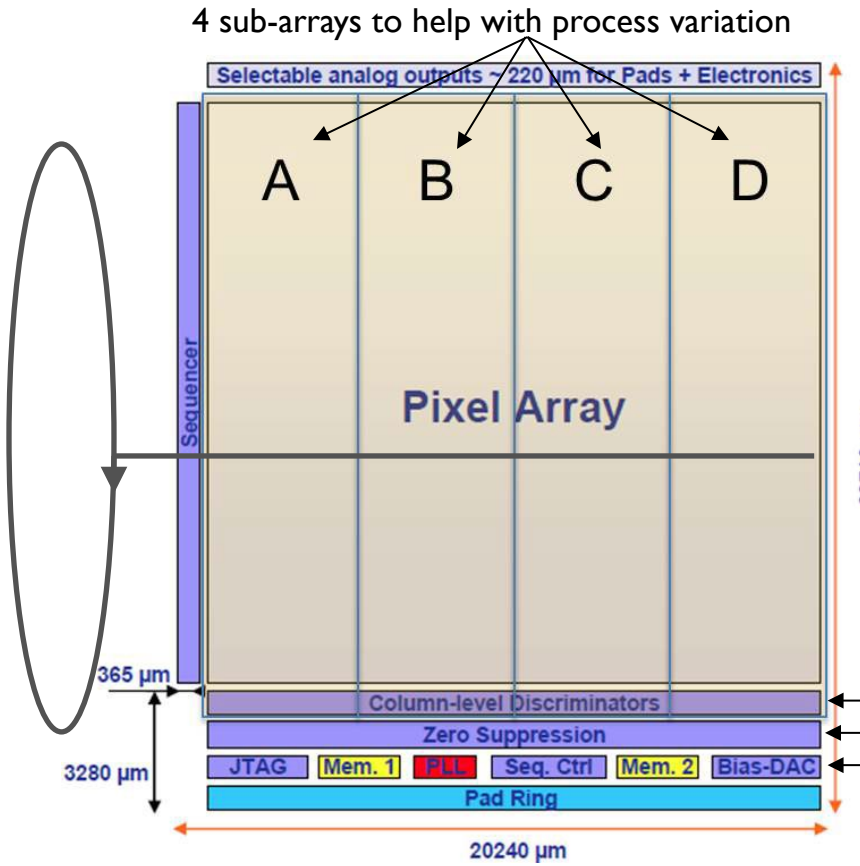
- Monolithic Active Pixel Sensors
- Reticle size (~ 4 cm²)
  - Pixel pitch 20.7 µm
  - 928 x 960 array
- Power dissipation ~170 mW/cm² @ 3.3V (air cooling)
- Short integration time 185.6 µs
- Sensors thinned to 50 µm

- In pixel **Correlated Double Sampling**
- **Discriminators** at the end of each column
- Column-parallel readout
- 2 **LVDS** data outputs @ 160 MHz
- Integrated zero suppression (up to 9 hits/row)
- Ping-pong memory for frame readout (~1500 words)
- 4 tunable sub-arrays to help with process variation
- JTAG configuration of many internal parameters

STAR HFT PXL sensor: Ultimate-2

- *Ultimate-2:* third generation sensor developed for PXL by the PICSEL group of IPHC, Strasbourg
- *Monolithic Active Pixel Sensor* technology, MIMOSA series

- High resistivity p-epi layer
  - Reduced charge collection time
  - Improved radiation hardness
- S/N ~ 30
- MIP Signal ~ 1000 e-
- **Rolling-shutter readout**
  - A row is selected
  - For each column, a pixel is connected to discriminator
  - Discriminator detects possible hit
  - Move to next row
- 185.6 μs integration time
- ~170 mW/cm² power dissipation



Pixel matrix

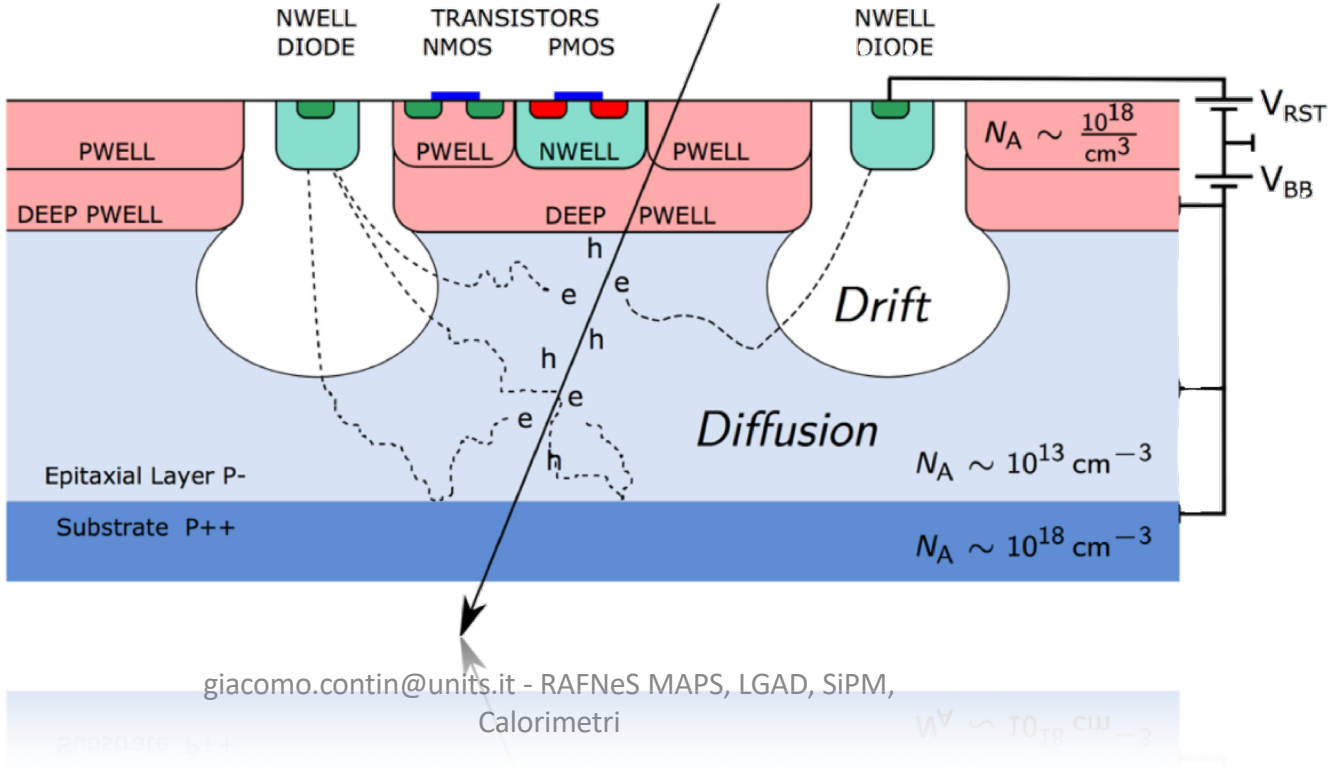
- 928 rows * 960 columns = ~1M pixel
- In-pixel amplifier
- In-pixel Correlated Double Sampling (CDS)

Digital section

- End-of-column discriminators
- Integrated zero suppression (up to 9 hits/row)
- Ping-pong memory for frame readout (~1500 w)
- 2 LVDS data outputs @ 160 MHz

Introduzione deep p-well → CMOS

- Un secondo impianto profondo (deep p-well) permette di implementare transistor pmos schermandolo, evitando che il suo n-well entri in competizione con i diodi di raccolta.
- E' difficile svuotare l'epitassiale perche' deve essere a **bassa resistivita'** per permettere di utilizzare tecniche industriali di design e produzione della logica CMOS.
- La raccolta di carica e' lenta perche' parzialmente per diffusione



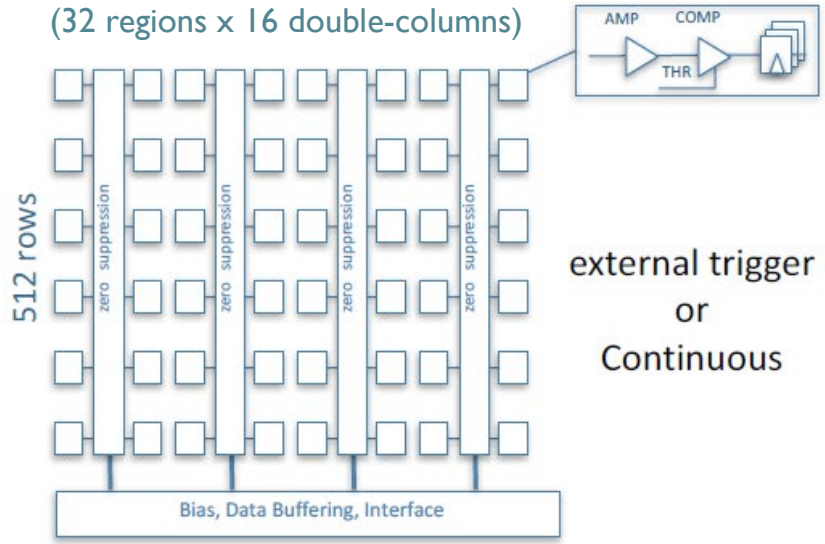
MAPS – ALPIDE sensor (2017)

Priority Encoder (AE-RD)

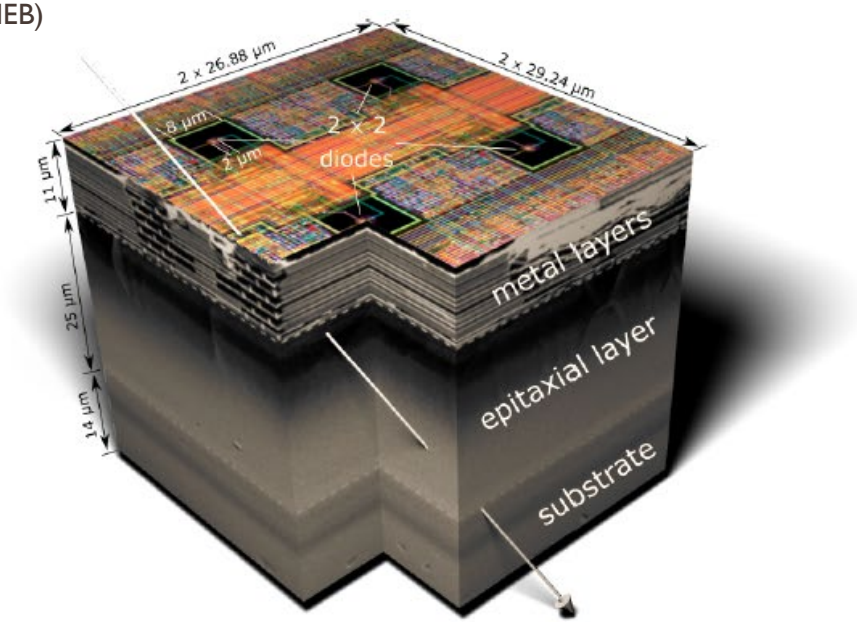
1024 pixel columns

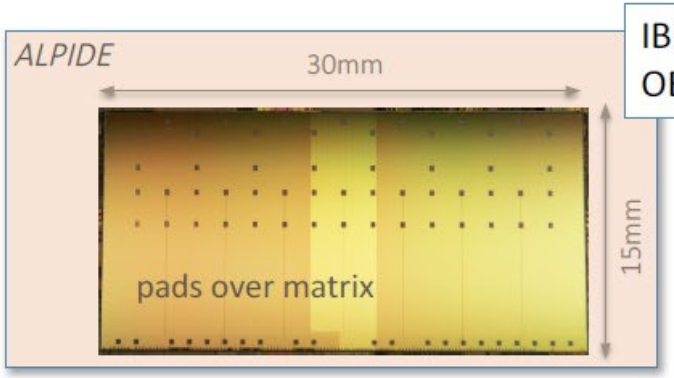
(32 regions x 16 double-columns)

In pixel:
- Amplification
- Discrimination
- 3 hit storage registers (MEB)



external trigger
or
Continuous





IB: 50µm thick
OB: 100µm thick

Power: 40 mW/cm^2
Trigger rate: 100 kHz
Integration time: < 20 µs
Read out up to 1.2 Gbit/s.

130,000 pixels / cm^2 27x29x25 µm^3

spatial resolution: ~ 5 µm (3-D)

Max particle rate: 100 MHz / cm^2

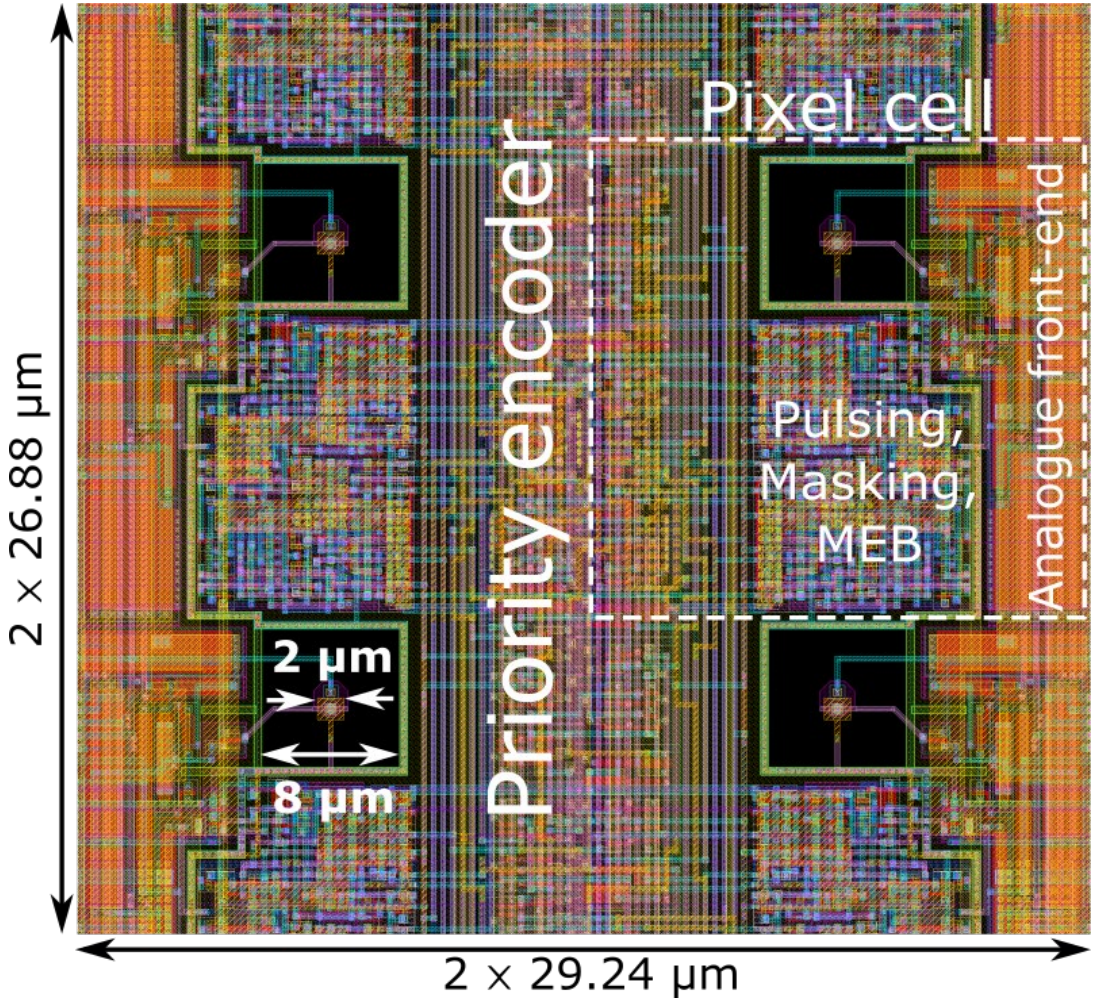
fake-hit rate: ~ 10^{-10} pixel / event

power : ~ 300 nW /pixel

MAPS working principle (3)

example: ALPIDE pixel

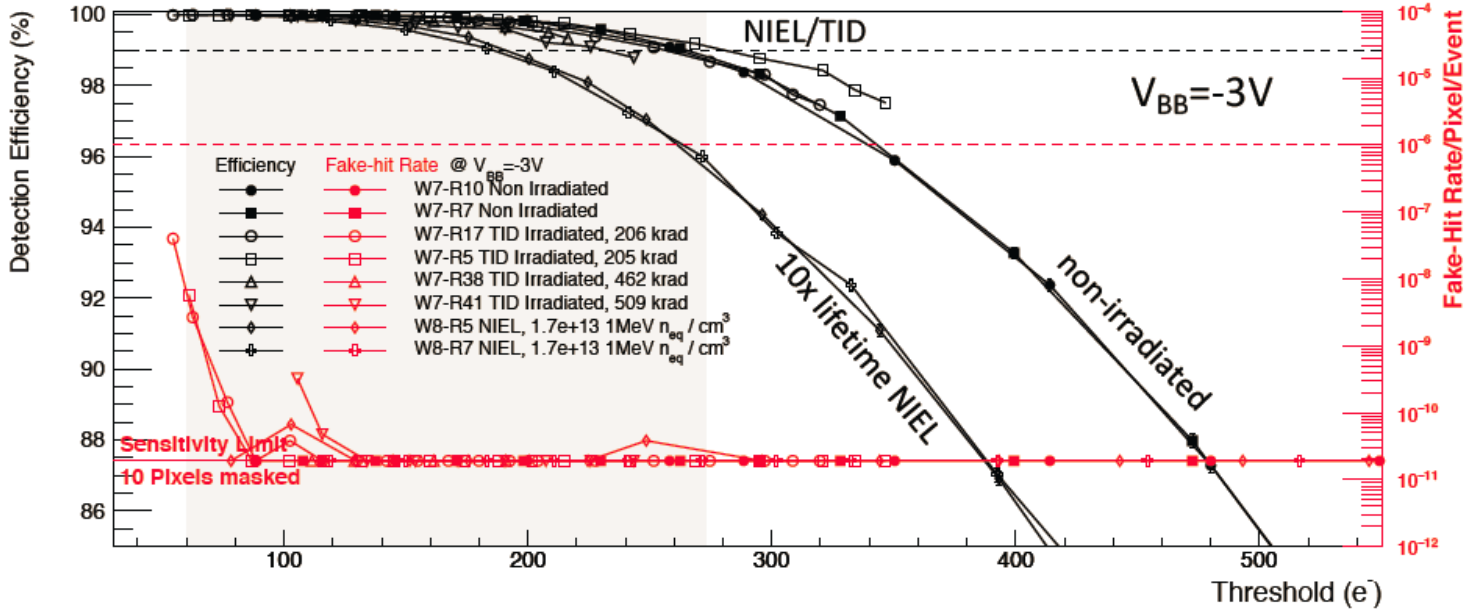
- **Front-end:**
  (9 transistors, full-custom)
  - continuously active
  - shaping time: < 10 μs
  - power consumption: 40 nW
- **Multiple-event memory:** 3 stages (62 transistors, full-custom)
- **Configuration:** pulsing & masking registers (31 transistors, full-custom)
- **Testing:** analogue and digital test pulse circuitry (17 transistors, full-custom)
- **Readout:** priority encoder, asynchronous, hit-driven



O(200) transistors / pixel

ALPIDE performance

Detection Efficiency and Fake-Hit Rate

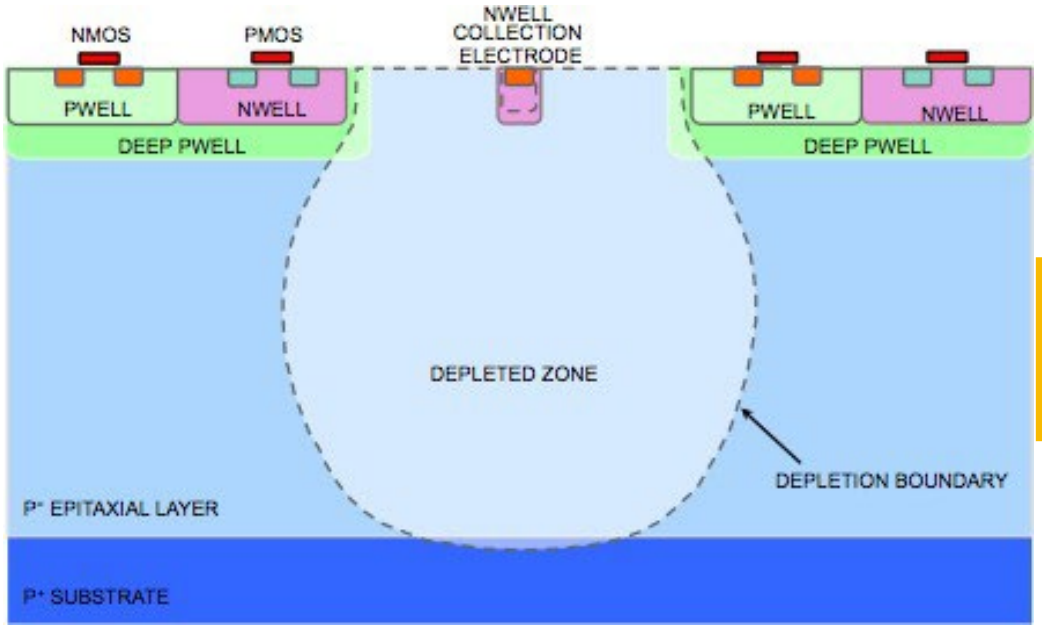


- Big operational margin with only 10 masked pixels (0.002%)
- Chip-to-chip fluctuations negligible
- Non-irradiated and NIEL/TID chips show similar performance
- Sufficient operational margin after 10x lifetime NIEL dose

From ITS Upgrade Talk @ QuarkMatter17, February '17

dell’epitassiale

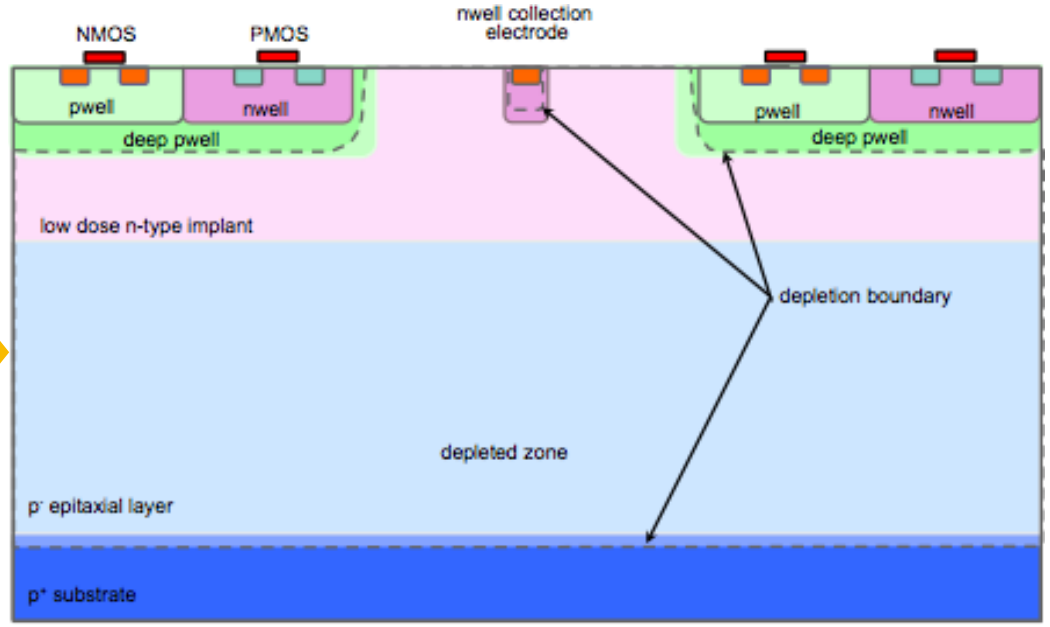
Foundry standard process



Partially depleted epitaxial layer
Charge collection time < 30 ns
Operational up to 10^{14} 1 MeV n_{eq}/cm^2

Developed and prototyped within ALPIDE R&D

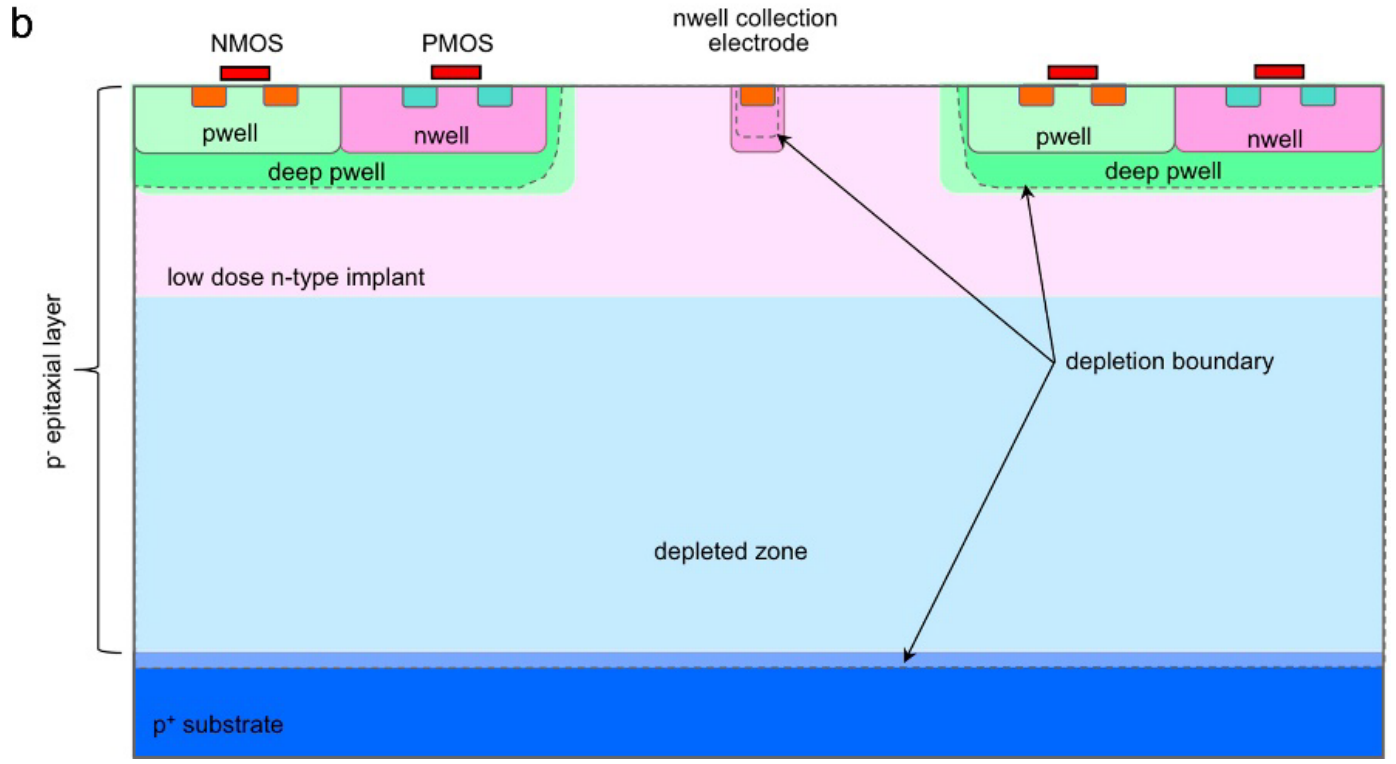
Modified process CERN/Tower



Fully depleted epitaxial layer
Charge collection time < 1 ns
Operational up to 10^{15} 1 MeV n_{eq}/cm^2

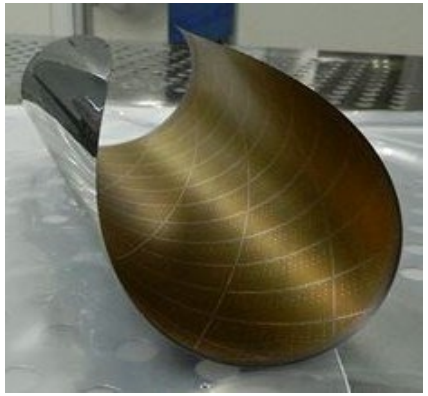
process modification for better timing and radiation hardness

Evoluzione verso lo svuotamento dell'epitassiale

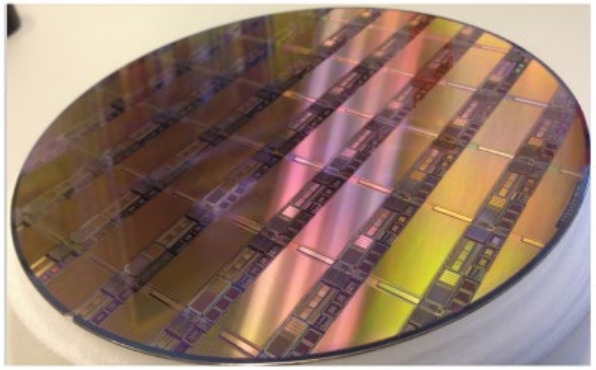


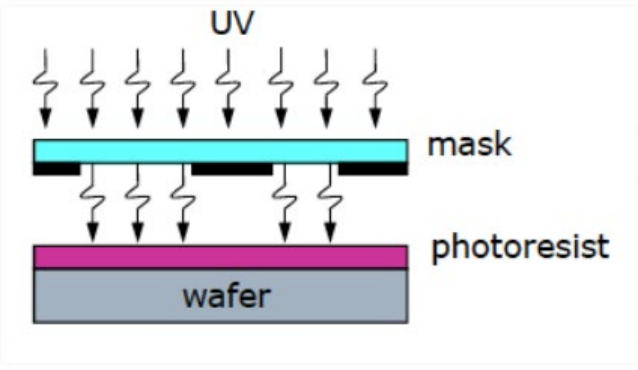
Assottigliamento e cucitura

- Assottigliamento (thinning)
  - Wafer partono da spessori piu' spessi (700-250um) per arrivare allo spessore desiderato (300-150um)
  - Substrato sul lato inattivo viene grattato via per sfregamento con dischi con superficie a grana via via piu' sottile, da 20-80um a 1-8um
  - Il lato attivo e' protetto da adesivo che viene poi lavato via
  - Resistenza alle rotture, deformazione, incurvamento da tenere sotto controllo



- Cucitura (stitching)
  - Esposizione allineata della stessa maschera ripetuta sul reticolo (~25mm*25mm) per coprire grandi superfici

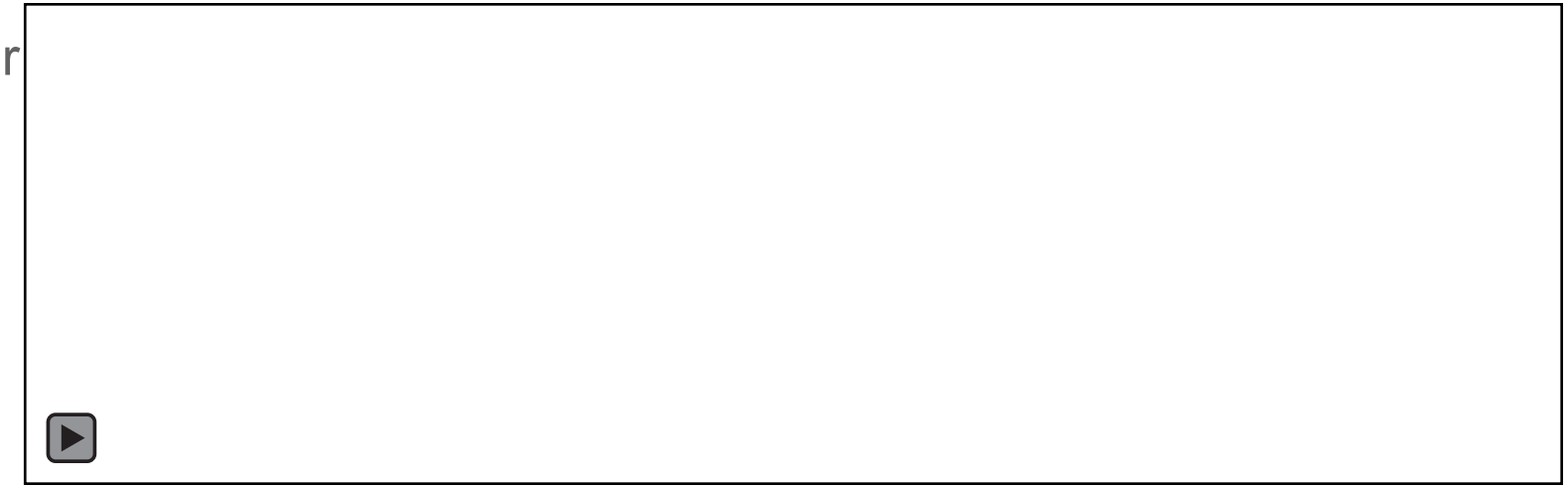




Stitching – Cucitura di strutture ripetute

Processo

- Suddividere la maschera
- Esporre ripetutamente il wafer alla sezione desiderata per raggiungere le dimensioni desiderate



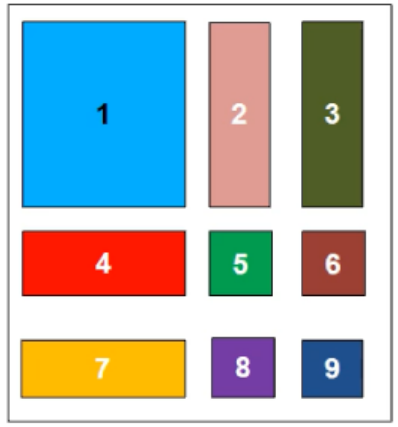
Implicazioni

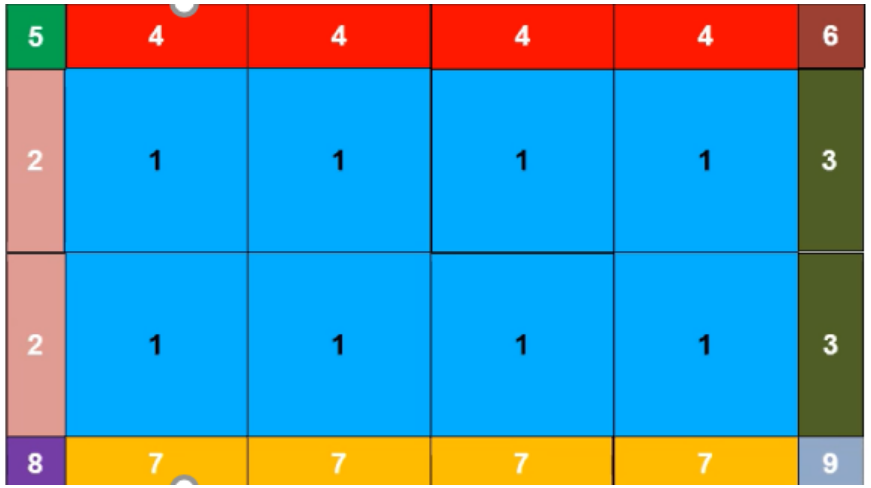
- Limiti aggiuntivi
- Poca flessibilita’
- Come indirizzare il giusto elemento ripetuto
- Resa di produzione per grandi aree

Stitching – Cucitura di strutture ripetute

Processo

- Suddividere la maschera
- Esporre ripetutamente il wafer alla sezione desiderata per raggiungere le dimensioni desiderate

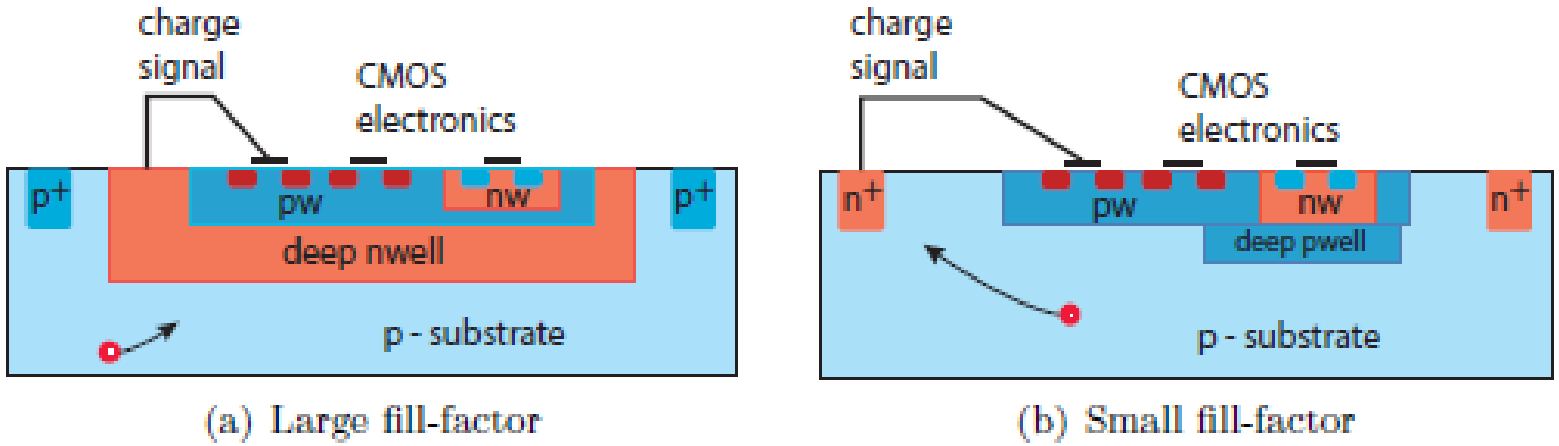




Implicazioni

- Limiti aggiuntivi
- Poca flessibilita’
- Come indirizzare il giusto elemento ripetuto
- Resa di produzione per grandi aree

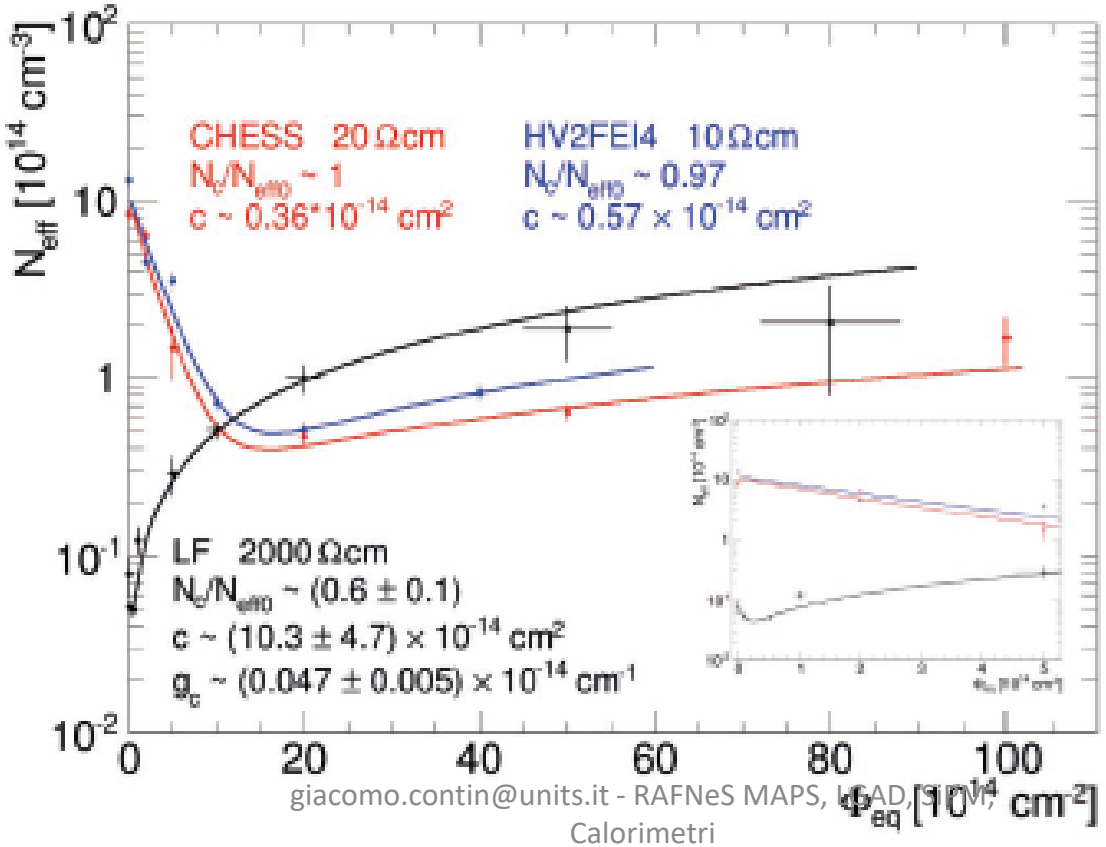
Fill factor



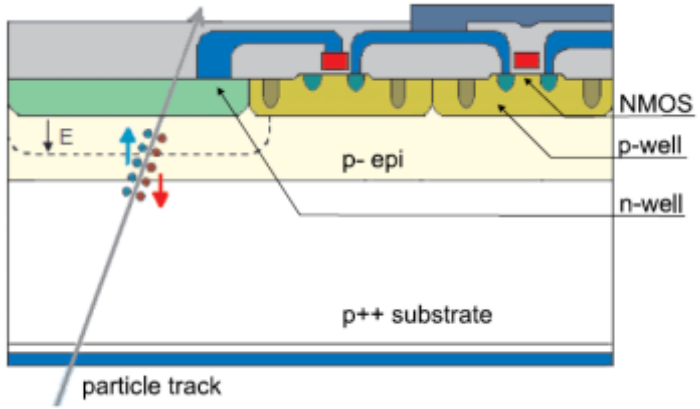
(a) Large fill-factor

(b) Small fill-factor

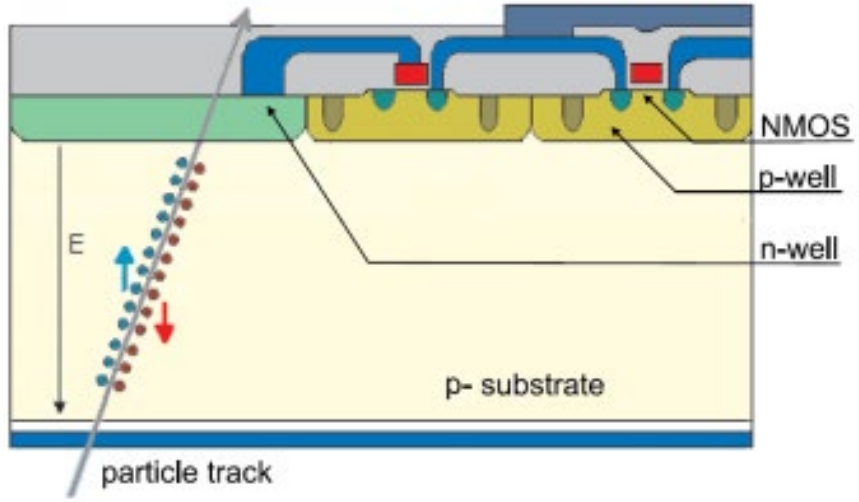
Resistivita' substrato



Monolithic Pixels

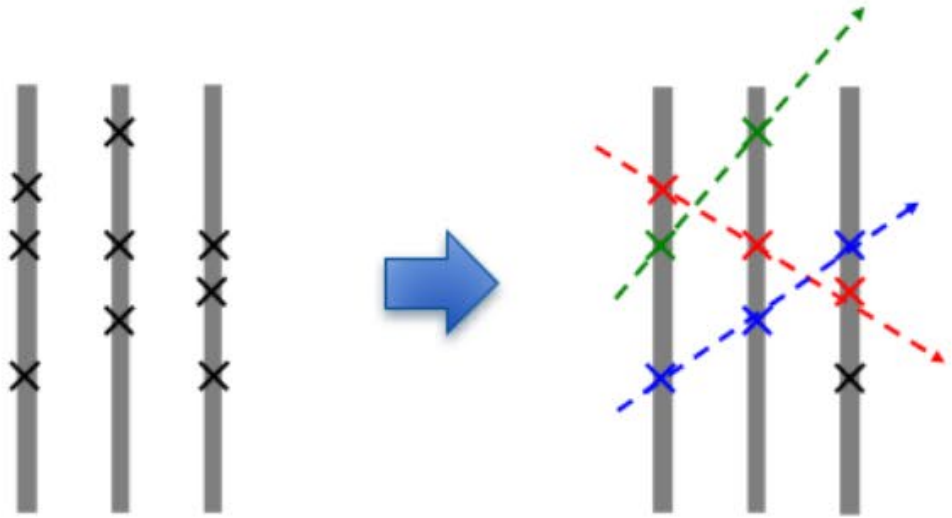


Depleted Monolithic Pixels

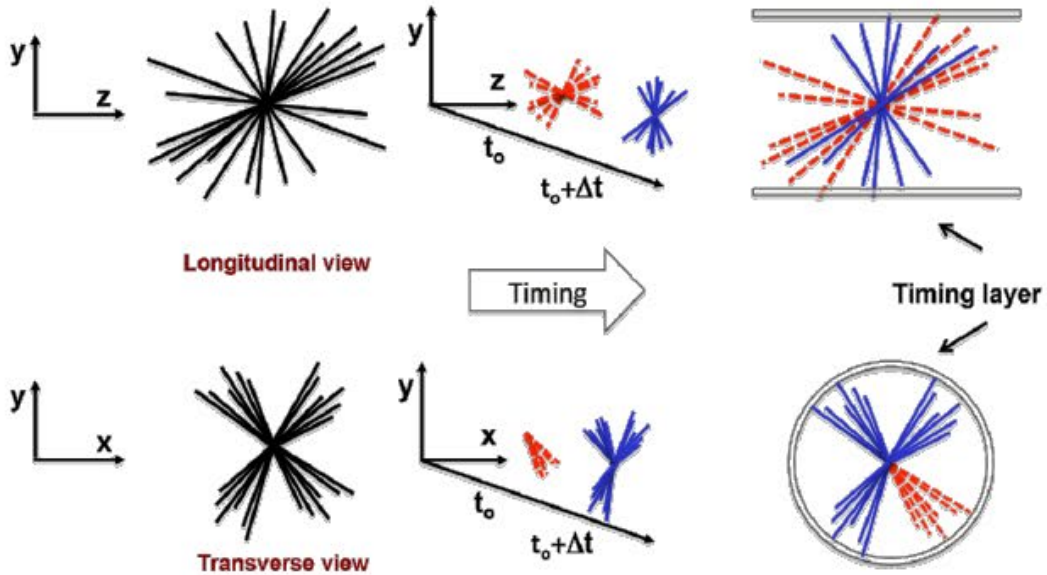


Acquisition of timing information

- Time tagging at each point
  - LHCb Upgrade II (Run 5 ~2030)



- Timing in the event reconstruction
  - HL-LHC: ATLAS and CMS



Rivelatori al silicio per misure di tempo

Si basano sulla moltiplicazione a valanga delle cariche in movimento nel semiconduttore

- Low Gain Avalanche Detectors (LGAD):
  - Rivelatori a valanga a basso guadagno tramite un sottile strato p+ ad alta concentrazione vicino all'anodo di raccolta
  - Gain: ~10
- Avalanche Photon Detectors (APD) & Single photon avalanche photodiode (SPAD)
  - Fotodiodo usato in regime valanga, come un interruttore seguito da una resistenza di quenching che spegne la valanga
  - Gain: ~1000
- Silicon Photo-Multiplier (SiPM)
  - Matrici di SPAD in parallelo, non usato per imagine perche somma i segnali dalle diverse celle
  - Gain: ~10000

Caratteristiche degli LGAD

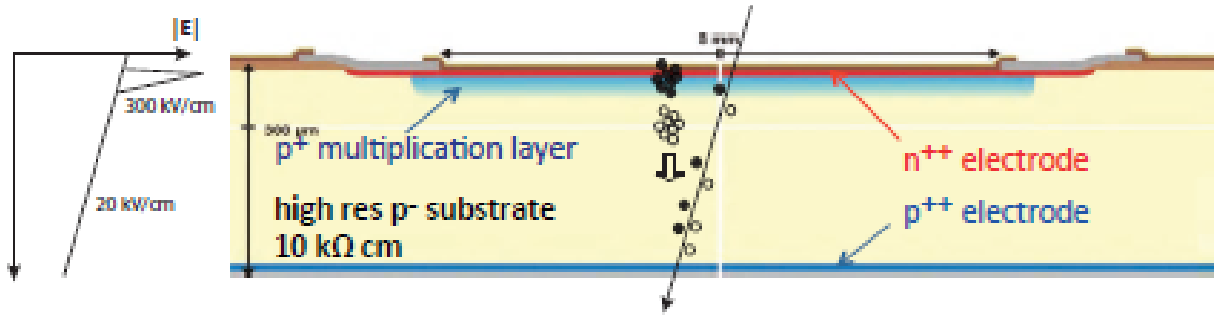
- Guadagno basso:
  - Permette un rumore piu' basso, crea campi meno intensi e quindi la possibilita' di segmentare di piu' la superficie, limita la dissipazione di potenza anche dopo irraggiamento
  - Se usato per particelle cariche, il segnale abbastanza alto permette di avere un buon S/N anche con un guadagno ~10-20

- Spessore sottile:
  - La durata del segnale generato dipende unicamente dal tempo massimo di deriva di un elettrone da una parte all'altra del silicio. L'ampiezza dipende dal fattore di guadagno. Quindi con guadagno fisso, la pendenza del fronte di salita aumenta per spessori piu' sottili.
  - D'altro canto spessori sottili introducono capacita' di carico maggiore, che poi necessitano di alti gain per misurare con precisione il segnale nell'elettronica. Entrambi i fattori creano un rumore piu' alto

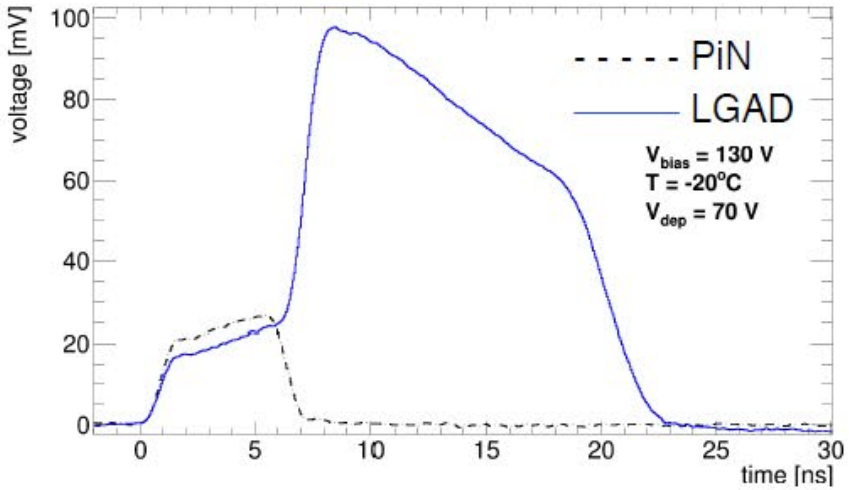
- Ottimali: Gain: ~20 – Spessore: ~50 um

Gain mechanism in LGADs

- Planar silicon sensors (n+/p/p-)
  - n+ implant, p substrate
  - p-type multiplication layer

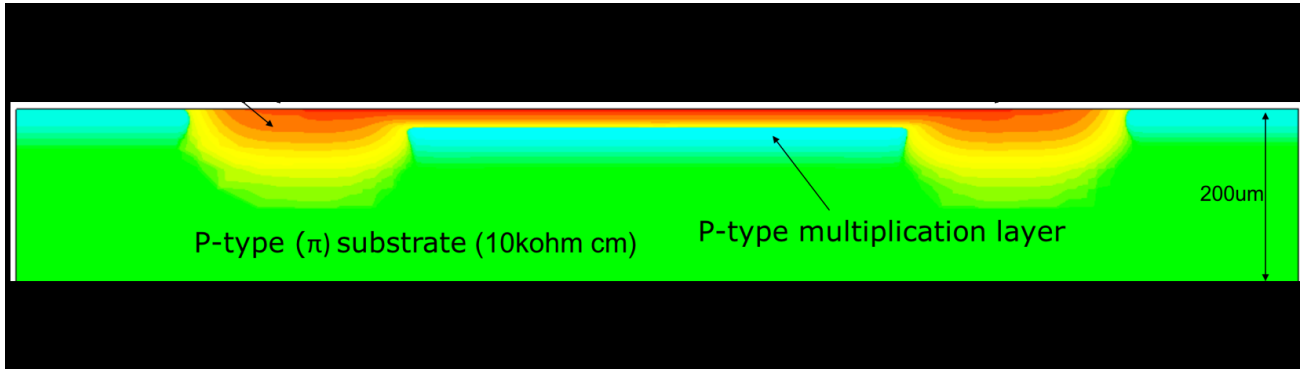


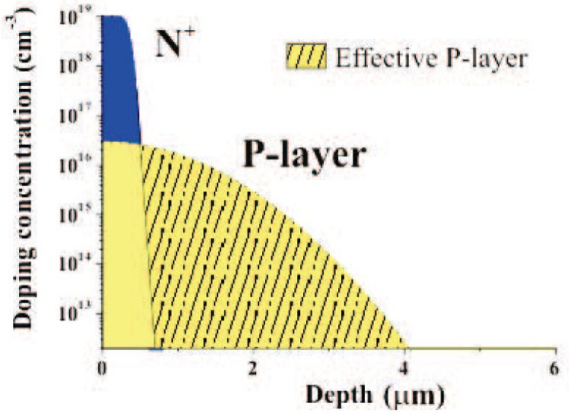
- **High electric field region in the multiplication layer**
  - Charges undergo impact ionisation
  - Gain depends on:
    - multiplication layer doping
    - bias voltage
    - temperature

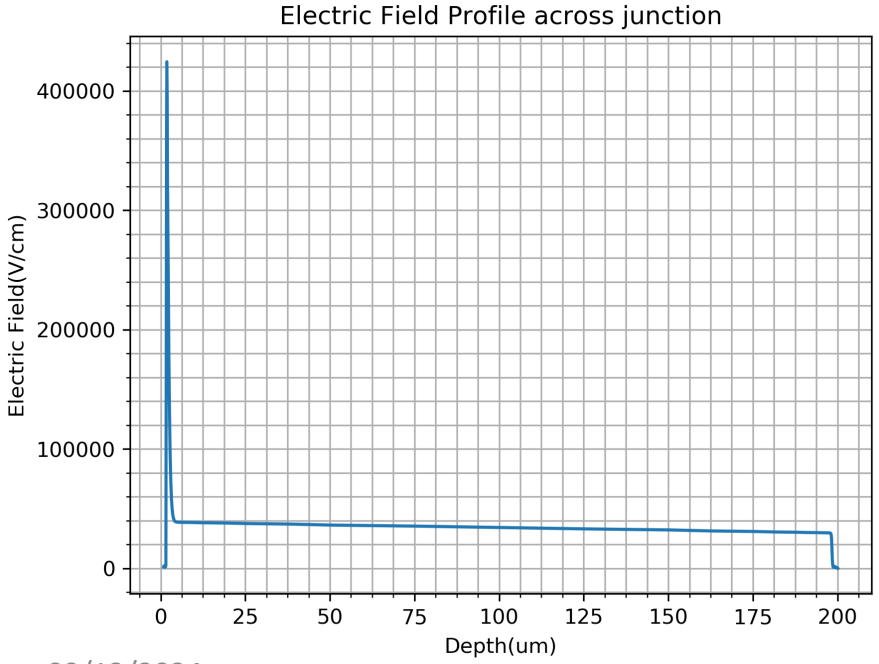


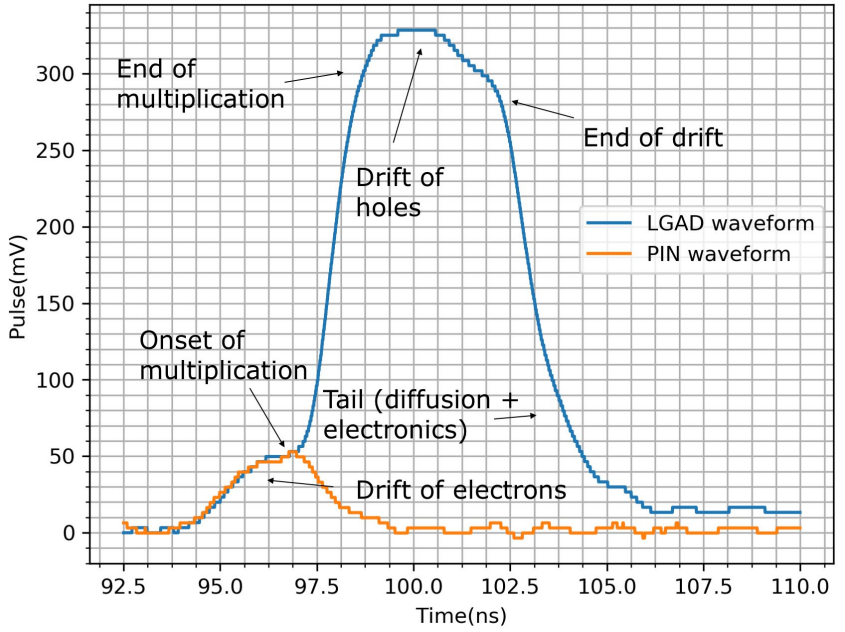
S. Otero Ugobono *et al.*, IEEE TNS (2018) vol. 6, no. 8, pp. 1667-1675

LGAD: simulazioni

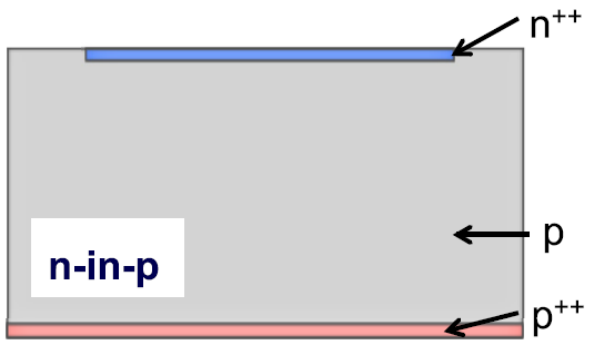




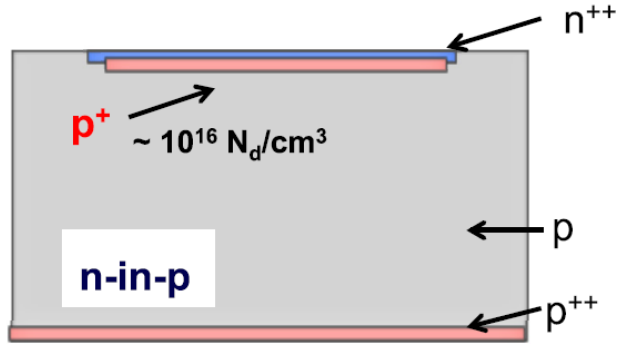




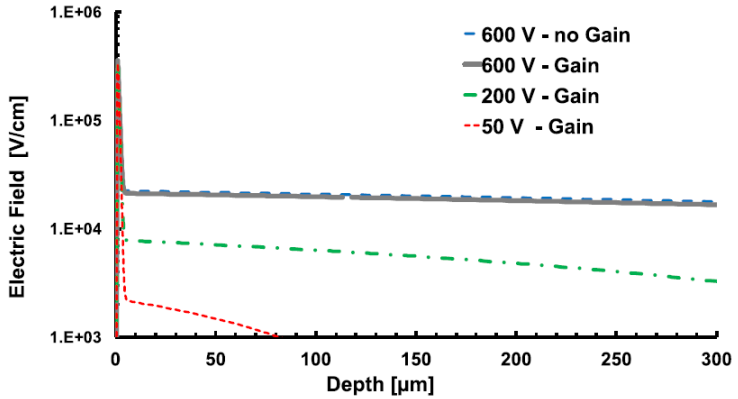
Campo elettrico in confronto a giunzione standard

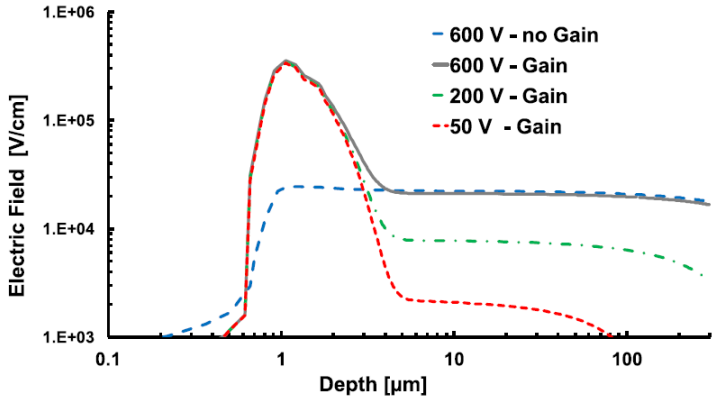


Traditional silicon detector



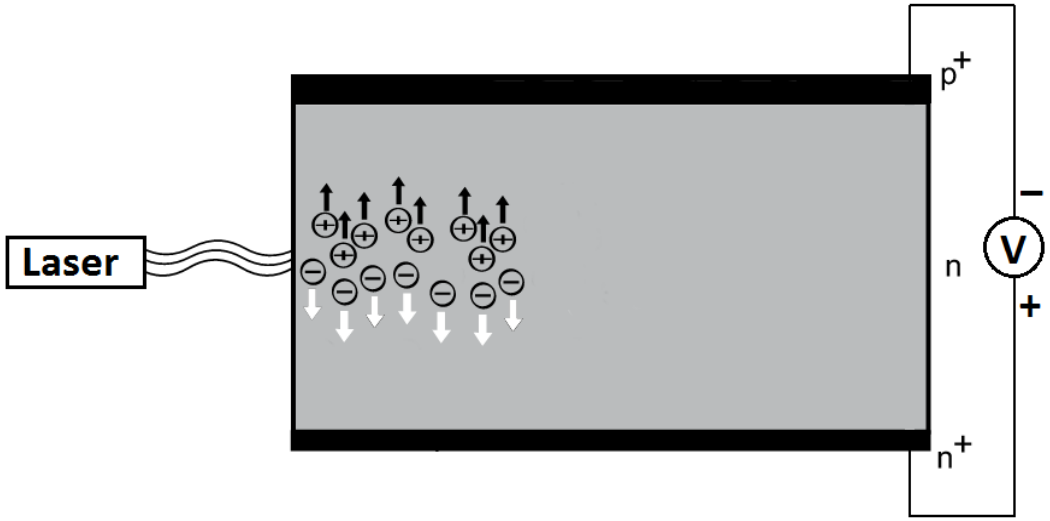
Low gain avalanche detectors

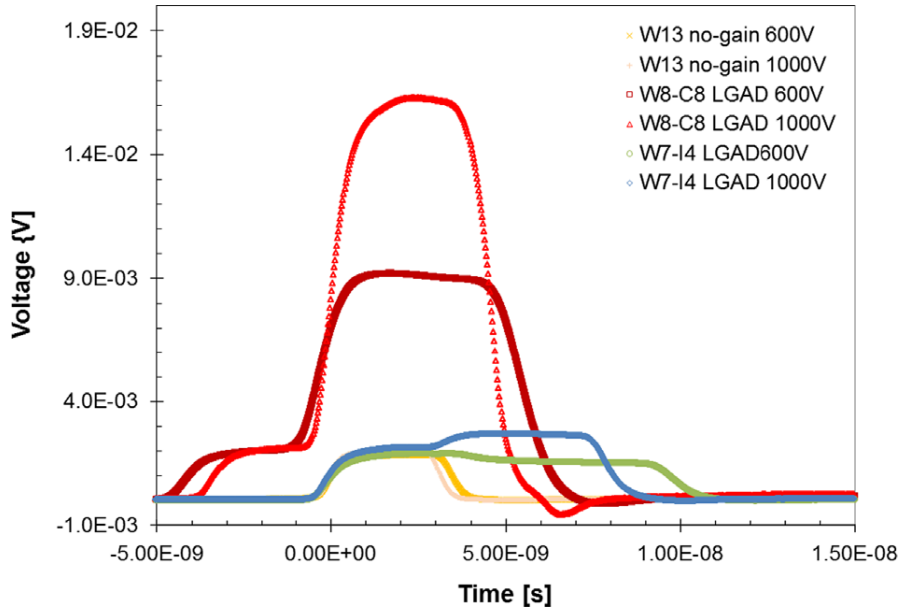




Caratterizzazione LGAD: misure TCT

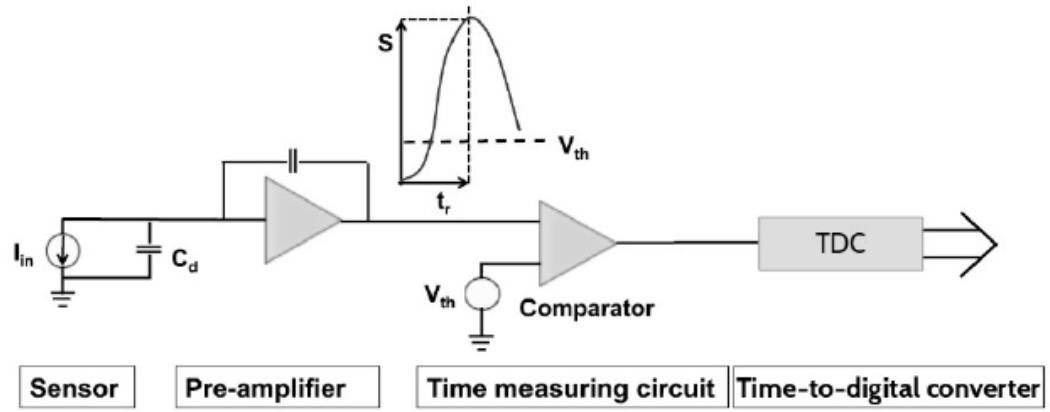
- Principio di funzionamento (Edge-)Transient Current Technique
- Misura TCT su LGAD con diversi Guadagni e a diverse Vbias





Localizzazione della generazione di carica per descrivere il profilo di drogaggio e gli effetti sulla valanga

Time resolution



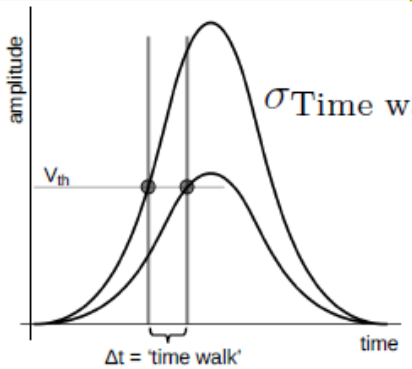
$$\sigma_t^2 = \sigma_{\text{Time walk}}^2 + \sigma_{\text{Landau noise}}^2 + \sigma_{\text{Jitter}}^2 + \sigma_{\text{Distortion}}^2 + \sigma_{\text{TDC}}^2$$

Time resolution is affected by:

- each step in the read-out process
- any effect that changes the shape of the signal

Time resolution

$$\sigma_t^2 = \sigma^2_{\text{Time walk}} + \sigma^2_{\text{Landau noise}} + \sigma^2_{\text{Jitter}} + \sigma^2_{\text{Distortion}} + \sigma^2_{\text{TDC}}$$



$$\sigma_{\text{Time walk}} \propto \left[\frac{N\sigma_n}{\mathrm{dV/dt}}\right]_{RMS}$$

- Variation in time of arrival due to different signal amplitudes
- Can be compensated by electronics

- Caused by inhomogeneous:
  - drift velocity
  - weighting field
- Solutions:
  - saturated drift velocity
  - optimised geometry

TDC: time-to-digital converter

$$\sigma_{\text{TDC}} = \Delta T/\sqrt{12}$$

comparator time bin width

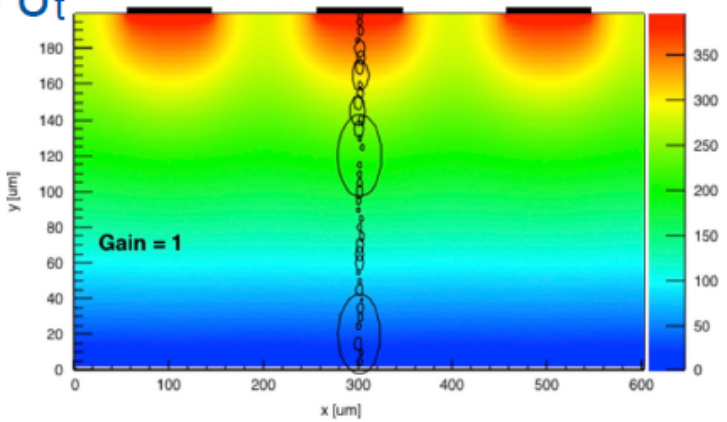
- Sub-picosecond ⇒ negligible

- V_{th}: threshold voltage to determine the time of arrival
- $N\sigma_n$: the threshold is usually expressed in multiples of the system noise

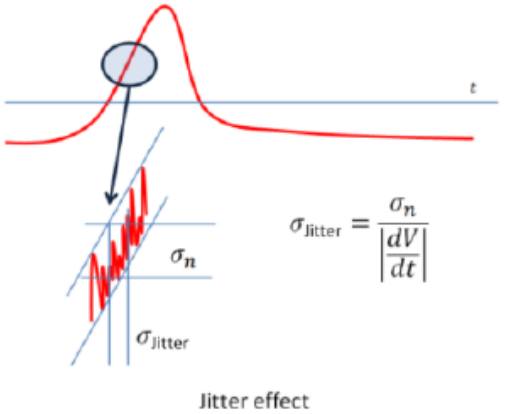
Time resolution

$$\sigma_t^2 = \sigma^2_{\text{Time walk}} + \sigma^2_{\text{Landau noise}} + \sigma^2_{\text{Jitter}} + \sigma^2_{\text{Distortion}} + \sigma^2_{\text{TDC}}$$

- Signal shape variations for MIPs
  - Non-uniform energy deposition per unit length
- Sets a physical limit to σ_t
- Can be minimised by:
  - setting a low V_{th}
  - using thin devices



- Variations in time of arrival due to signal noise



Jitter effect

- Can be minimised with:
  - low noise sensors
  - low noise electronics
  - fast slew rates

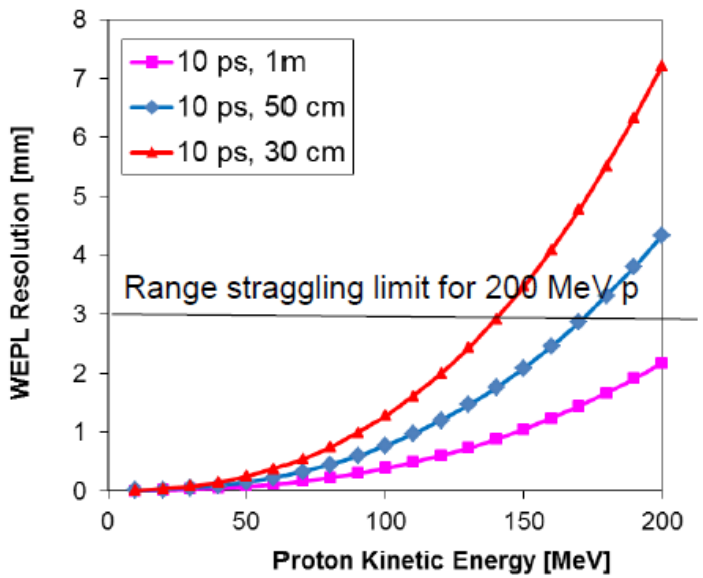
- V_{th}: threshold voltage to determine the time of arrival

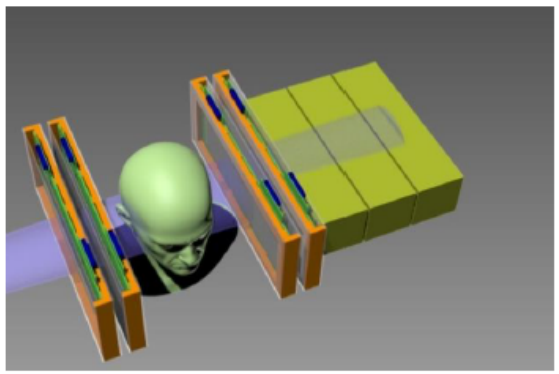
4-D Ultra-Fast Si Detectors in pCT

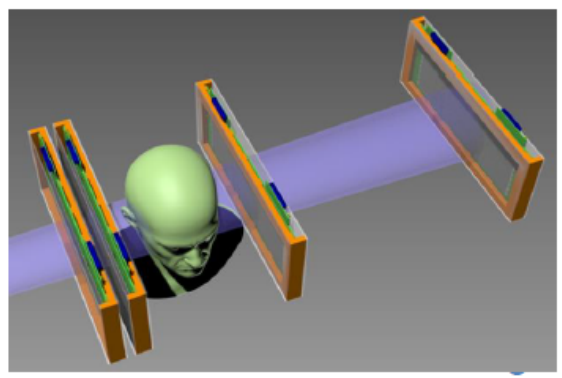
In support of Hadron Therapy, the relative stopping power (RSP) is being reconstructed in 3D.
The UCSC-LLU pCT scanner uses Si strip sensors to locate the proton and heavy scintillator stages to measure its energy loss (WEPL).

Protons of 200 MeV have a range of ~ 30 cm in plastic scintillator. The resulting straggling limits the WEPL resolution.

Replace calorimeter/range counter by UFSD:
Combine tracking with WEPL measurement where the ToF of the proton measures the residual energy., with comparable or better resolution than the scintillator.





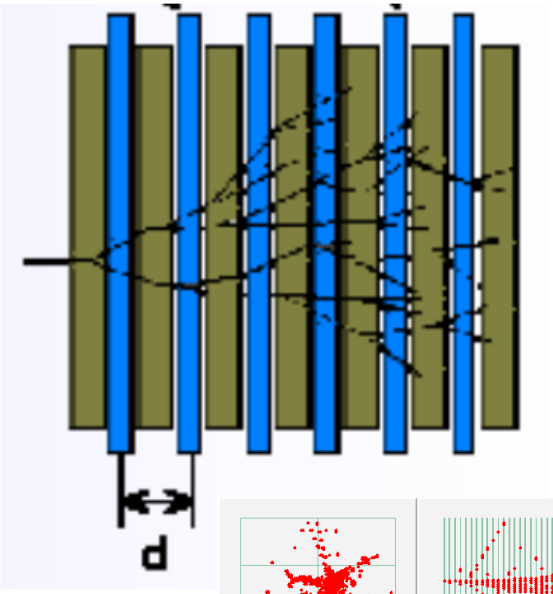


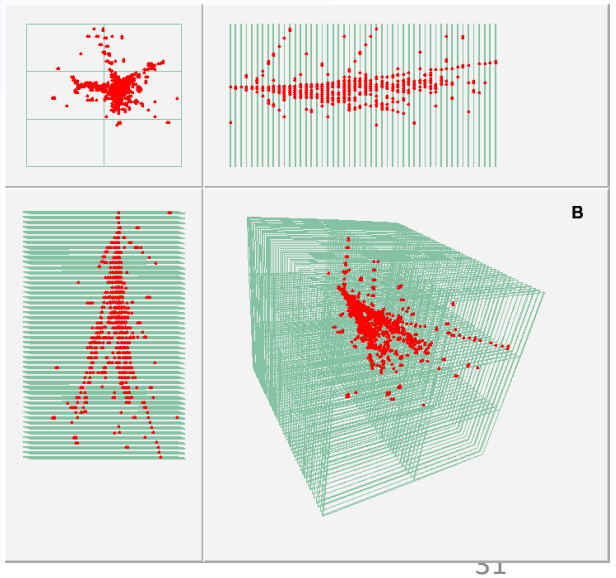
Light-weight, all silicon construction ideal for installation Into the gantry

- Applicazione rivelatori al silicio in calorimetria:
  - Calorimetri a campionamento

Sampling calorimeters

- Use different media
  - High density absorber
  - Interleaved with active readout devices
  - Most commonly used: sandwich structures ➔
  - But also: embedded fibres, ….
- Sampling fraction
  - $f_{sampl} = E_{visible} / E_{total\ deposited}$
- Advantages:
  - Cost, transverse and longitudinal segmentation
- Disadvantages:
  - Only part of shower seen, less precise



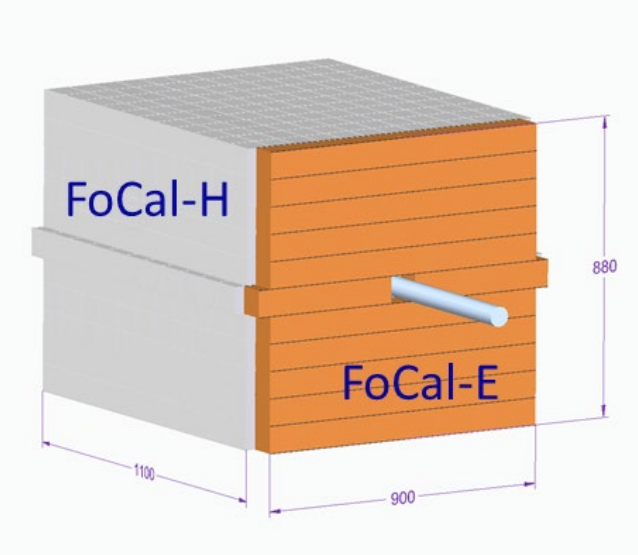


FoCal-H and FoCal-E

FoCal-H: Conventional sampling hadronic calorimeter (Cu + scintillating fibres)

- Providing γ isolation through direct detection of high energy hadrons

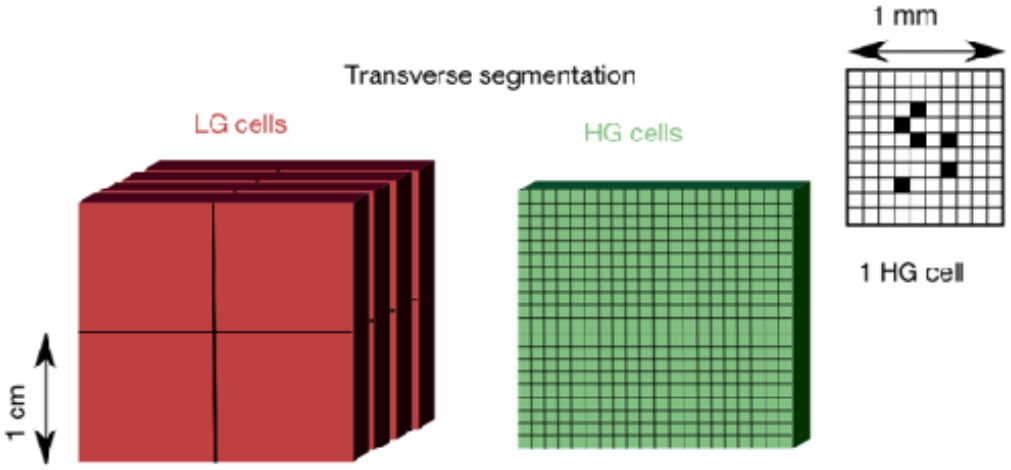
FoCal-E: high-granularity Si-W electromagnetic calorimeter for γ and π_0

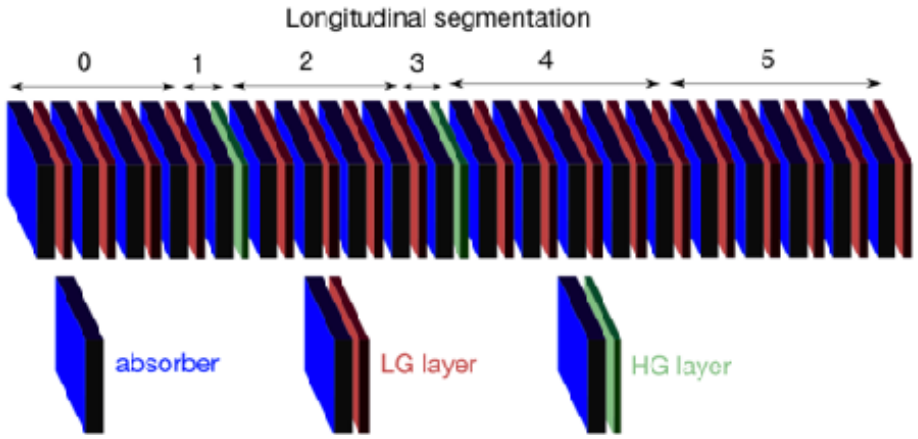


- **Main challenge** for Focal-E**:** γ/π_0 separation at high energy
  - two photon separation from π^0 decay: ~2 mm
  - needs small Molière radius and high granularity readout

  ➔ Si-W calorimeter with effective granularity of ~1 mm^2

FoCal-E detector technologies



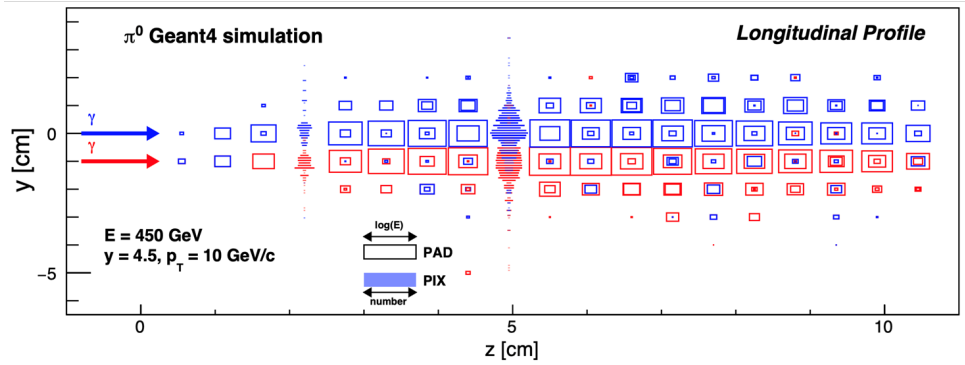


Studied in simulations: 20 layers

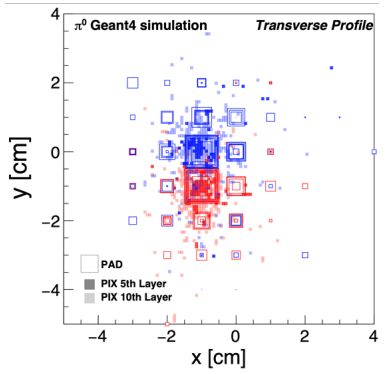
W (3.5 mm ~ $1X_0$) + silicon

- 18 Pad layers
  - Low granularity (LG), provide shower profile and total energy
- 2 Pixel layers (ALPIDE)
  - High granularity (HG), provide position resolution to resolve overlapping showers

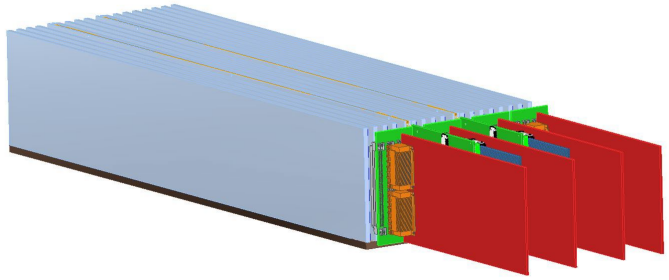
Longitudinal profile (2γ showers)



Trans. profile

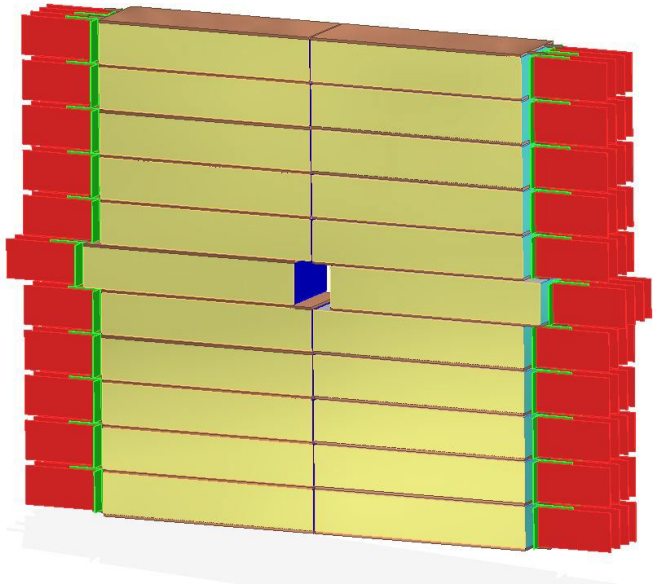


FoCal-E layout and prototypes

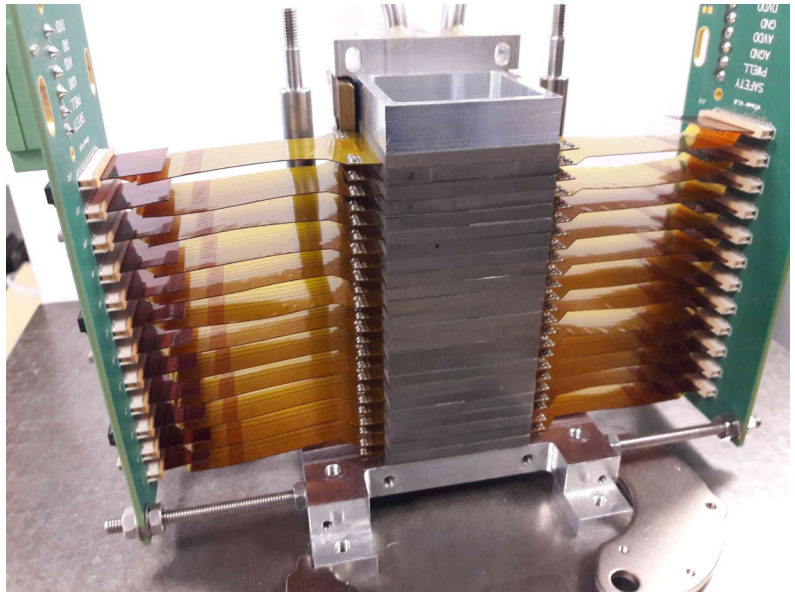


Module: 18 pad layers + 2 pixel layers

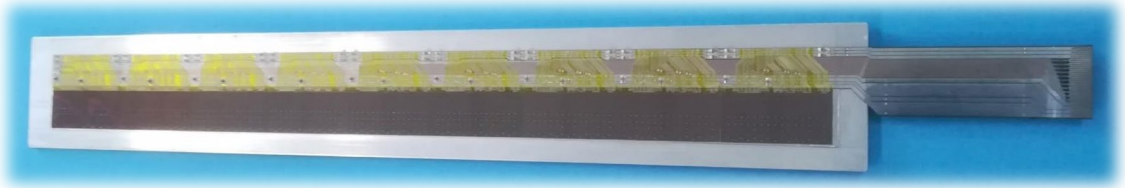
- Readout, power, cooling connected on one side



FoCal-E:
22 modules



EPICAL
all-pixel small E-cal



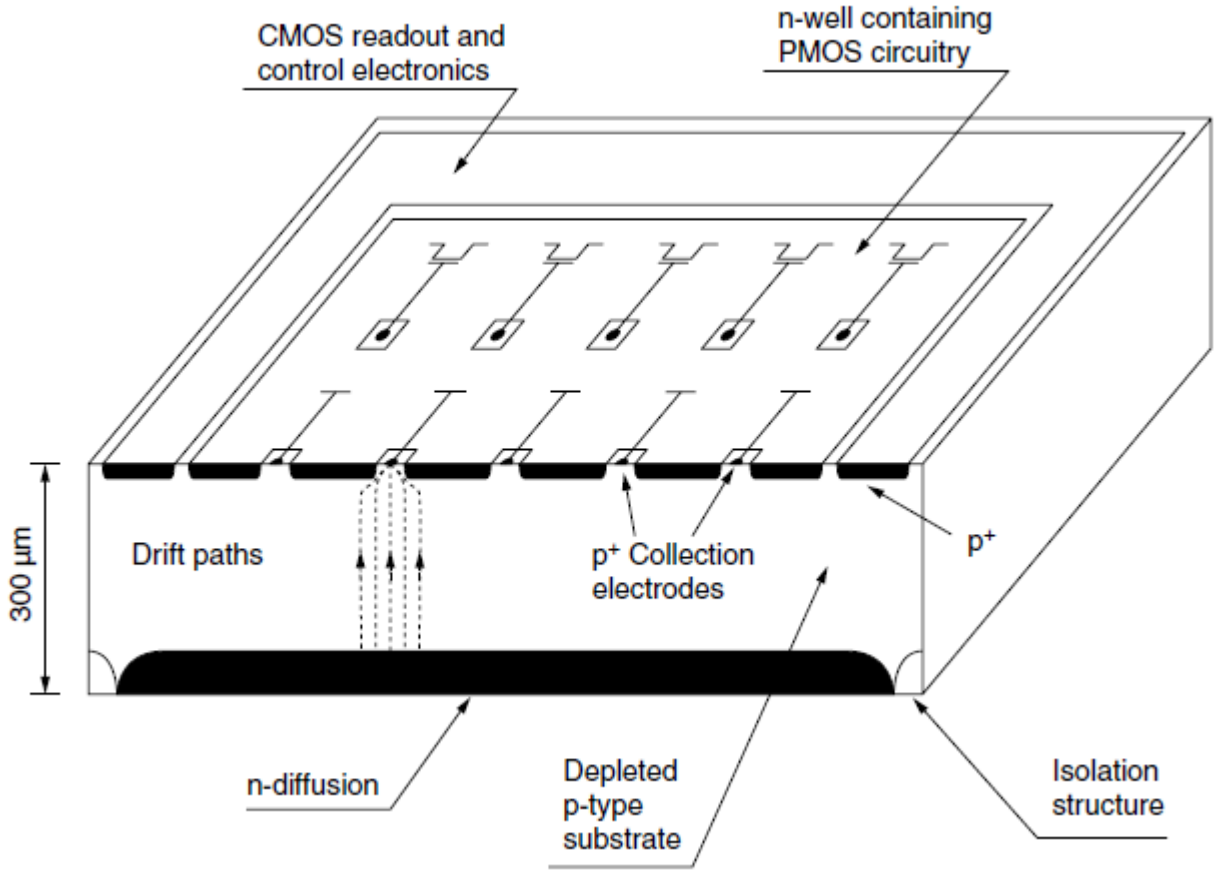
Pixel string prototype: 9x SpTAB bonded ALPIDE
Final pixel layer will have 3x 15-ALPIDEs strings

Approfondimenti/backup

Primi monolitici

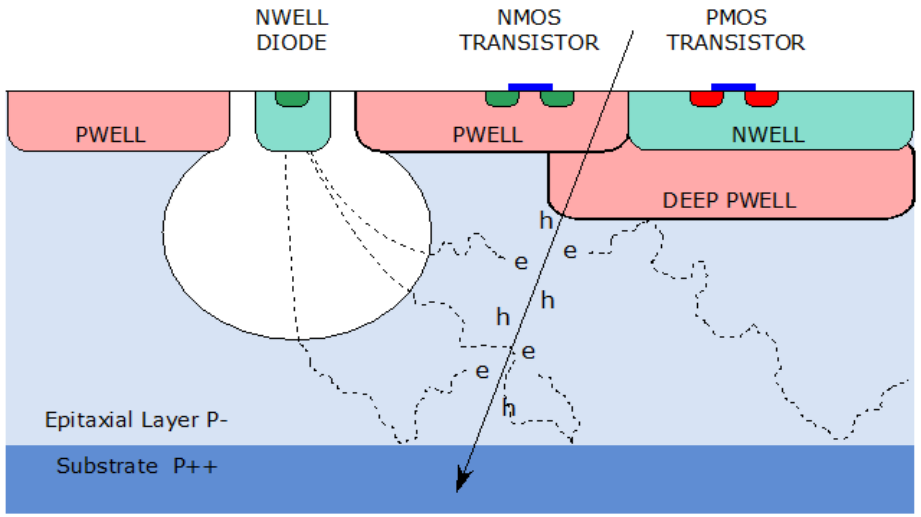
- Silicio molto resistivo e puro
- Svuotamento completo
- Solo un n-well superficiale
  - Forma transistor pmos
  - Fa da schermo tra logica e substrato
- Logica basilare nella matrice
- Logica completa nella periferia
- Basso *fill factor*
- Giunzione si forma dal lato opposto
- Zona di raccolta e' a basso campo in svuotamento completo

- *Caratteristiche:*
- 10 col. X 30 righe
- A = 34 um x 125 um
- S/N ~ 55
- σ_x ~ 2.2 um



ITS Pixel Chip – technology choice

CMOS Pixel Sensor using TowerJazz 0.18µm CMOS Imaging Process

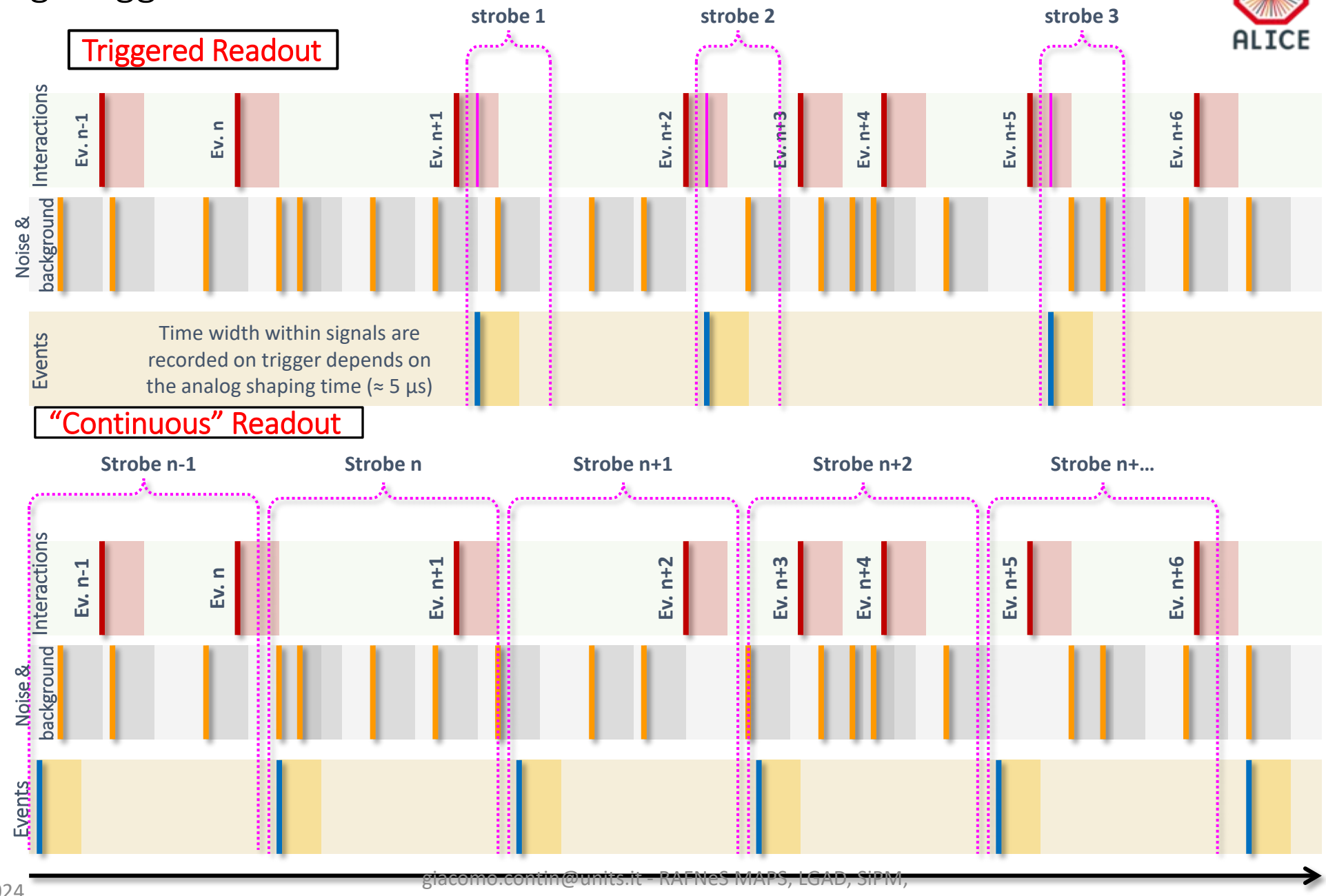


ALPIDE sensor *(developed within ALICE)*

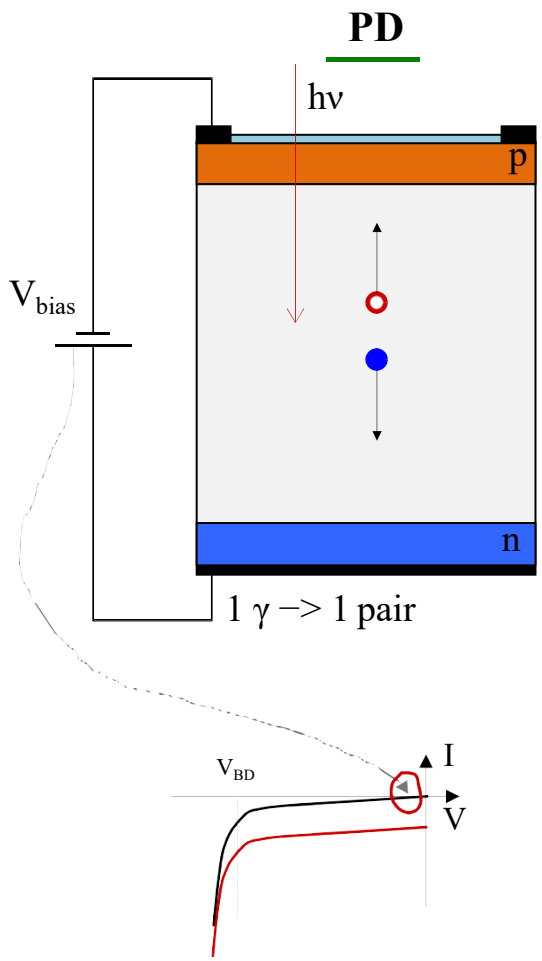
- ~28 µm pitch
- Integration time: < 20 µs
- Trigger rate: 100 kHz
- Read out up to 1.2 Gbit/s
- Power: 40 mW/cm^2
- Priority encoder - sparsified readout
- Rad. Tolerant: 700krad -10^{14} 1MeV n$_{eq}$/cm^2

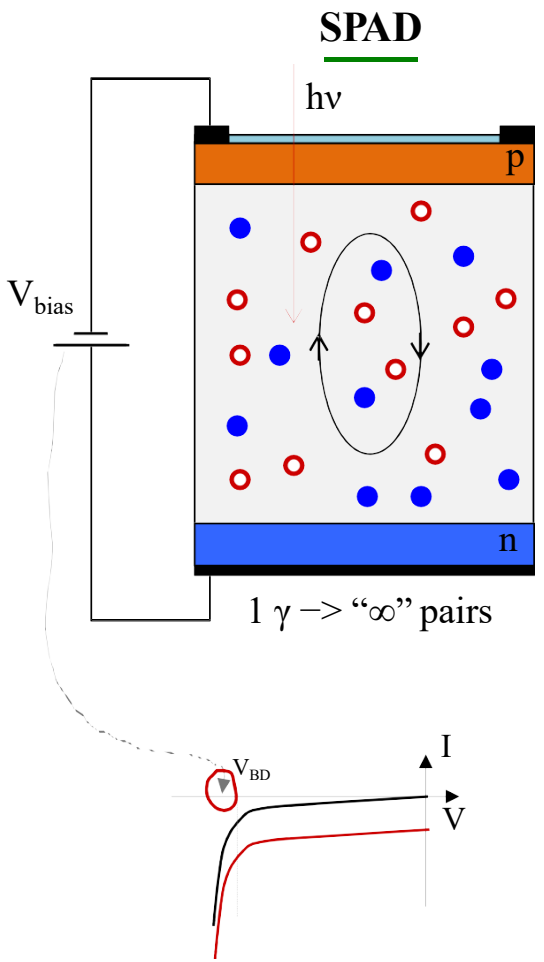
- High-resistivity (> 1kΩ cm) p-type epitaxial layer (20µm - 40µm thick) on p-type substrate
- Small n-well diode (2-3 µm diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate can be used to increase depletion zone around NWELL collection diode
- Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area

ALPIDE Timing: Triggered & “Continuous” Readout

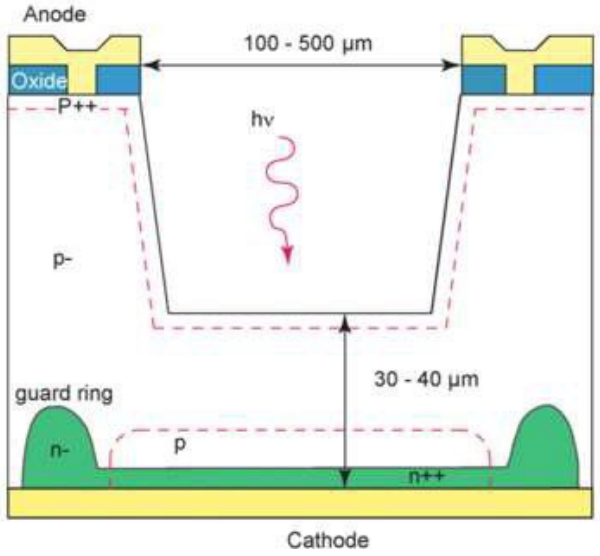


PD and SPAD

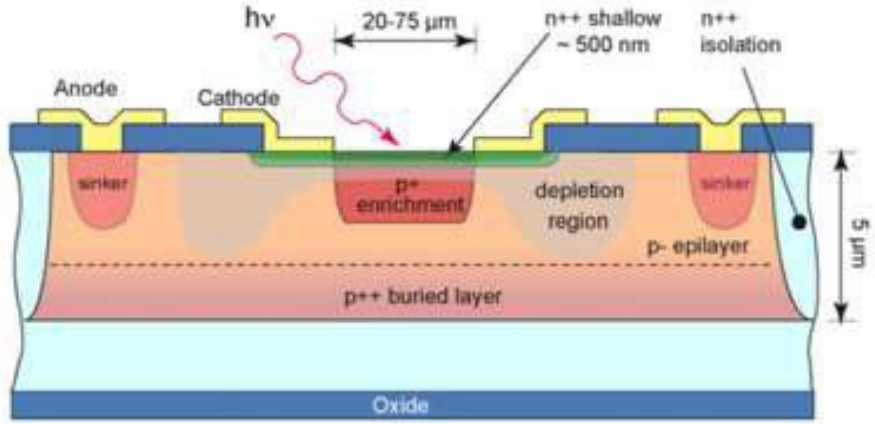




Structure of a SPAD



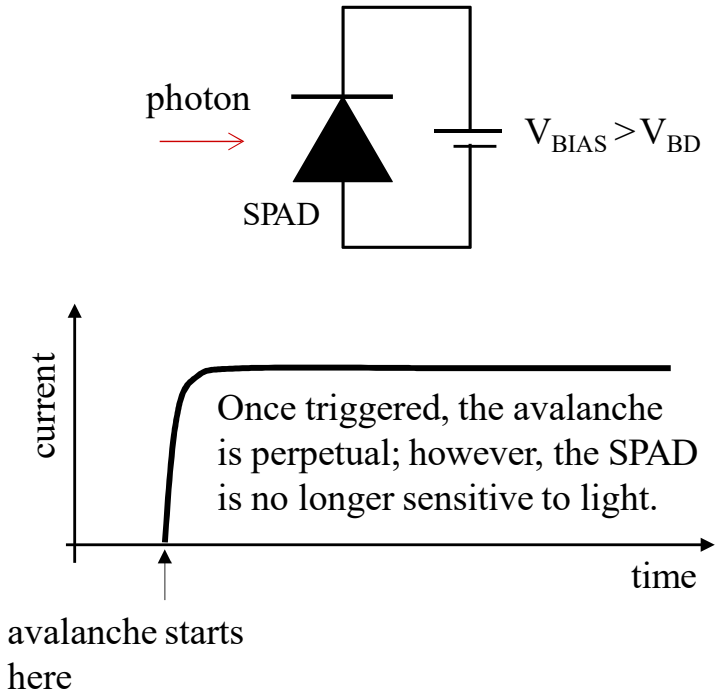
Structure of a *thick* SPAD



Structure of a *thin* SPAD. This structure is used in SPAD arrays.

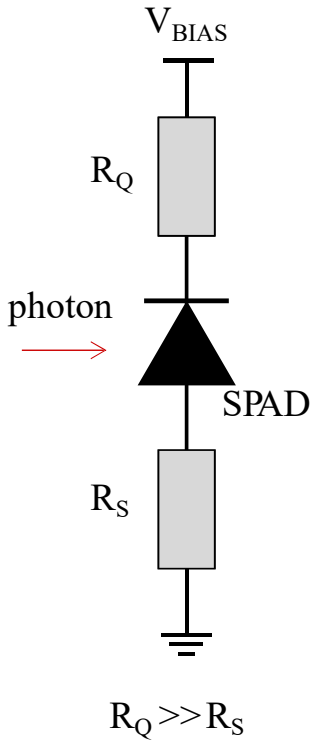
Figures from Zappa et al. 2007

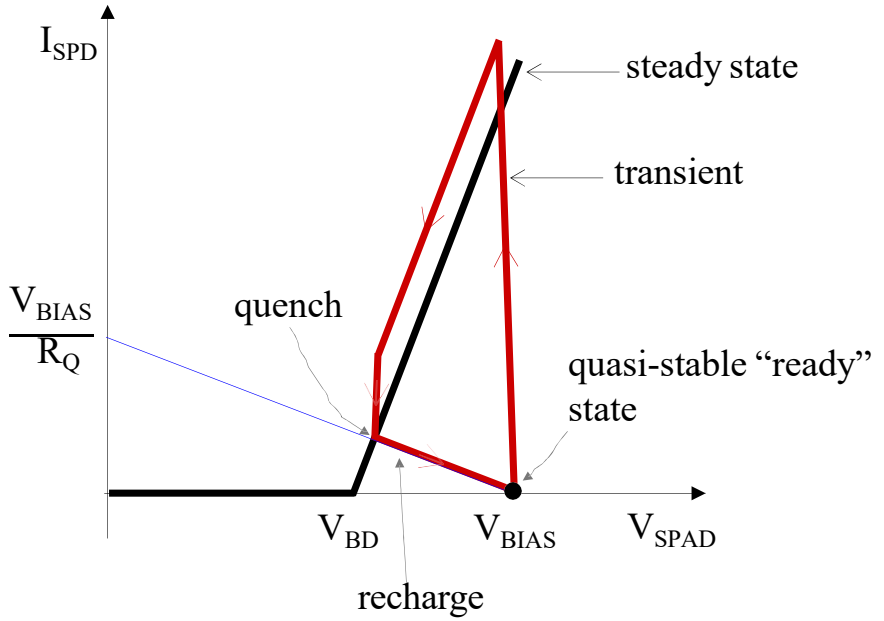
Operation of a SPAD



Without quenching, SPAD operates as a light switch.

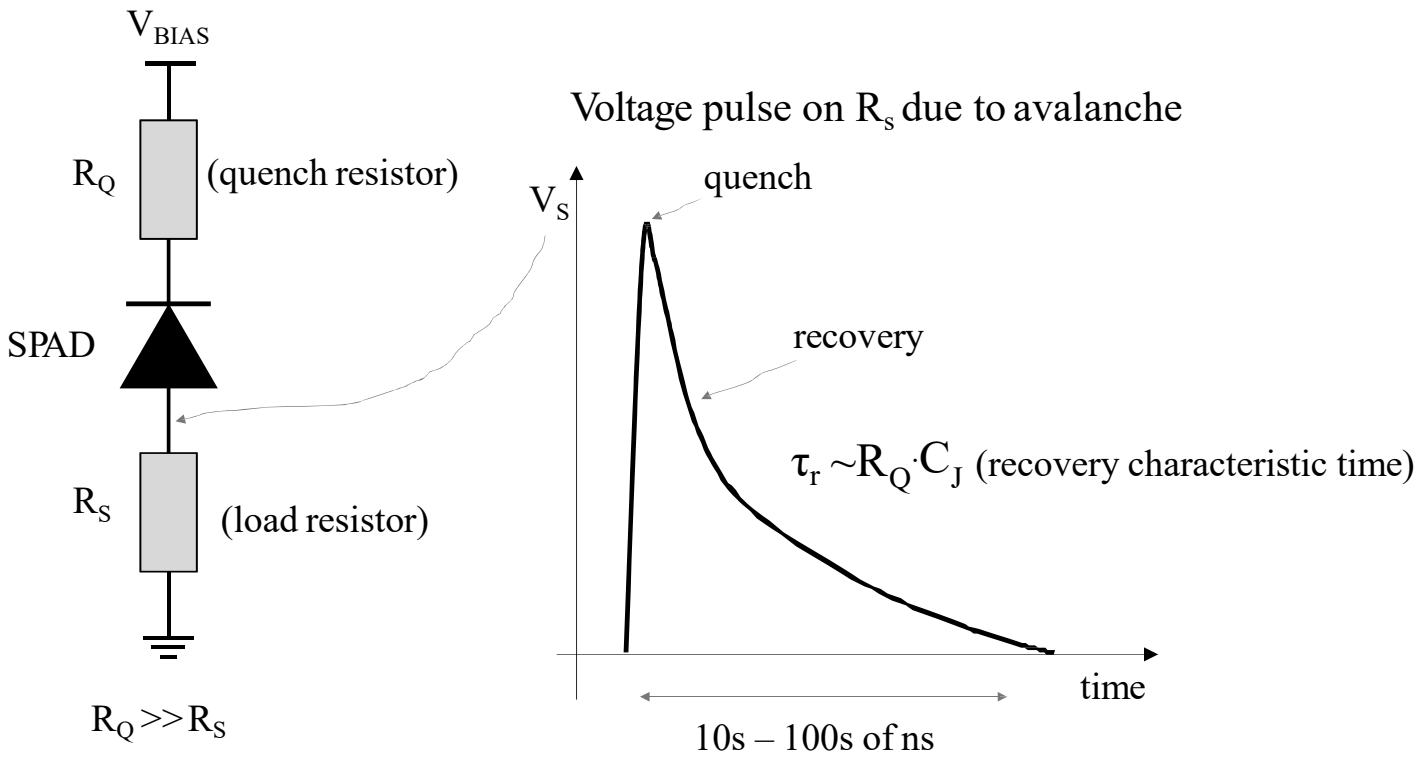
Operation of a SPAD (passive quenching)



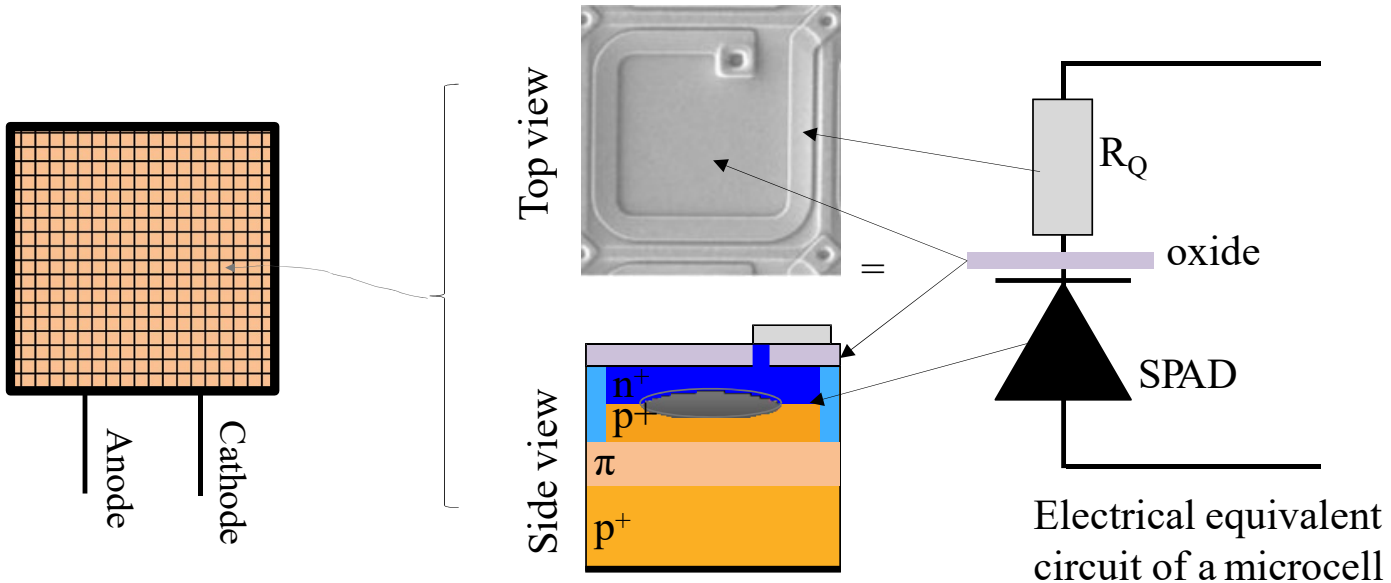


R_Q must be large enough to ensure quenching.

Operation of SPAD (passive quenching)

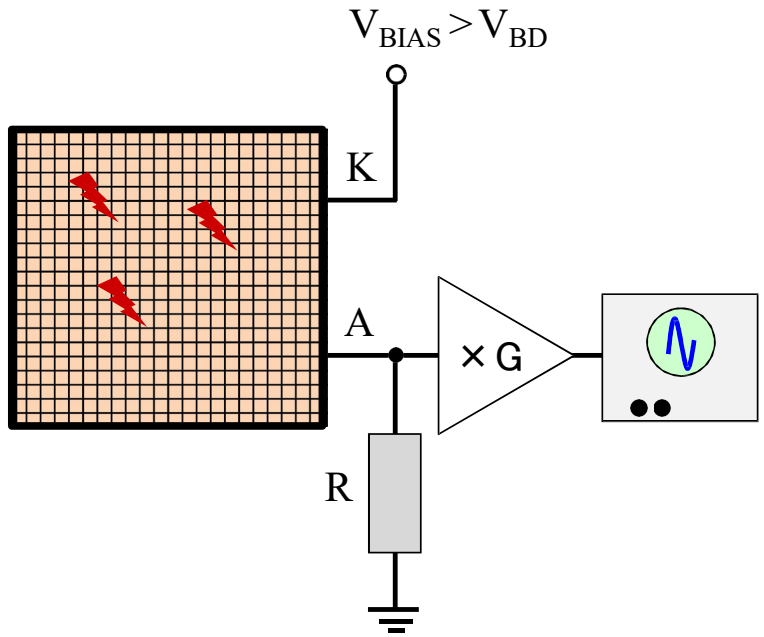


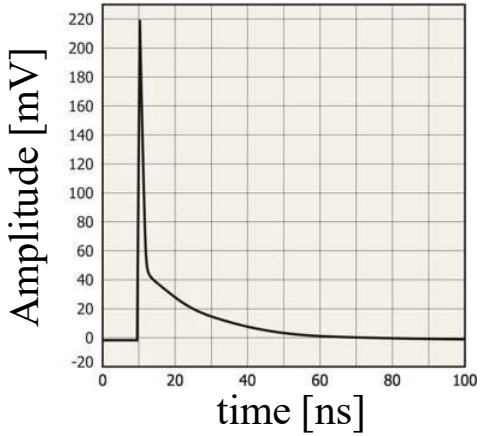
Si-PM Silicon photomultiplier: structure



Each microcell is a SPAD in series with a quench resistor. All microcells are connected in parallel. SiPM is **not** an imaging device because all microcells share a common current summing node.

Silicon photomultiplier: operation



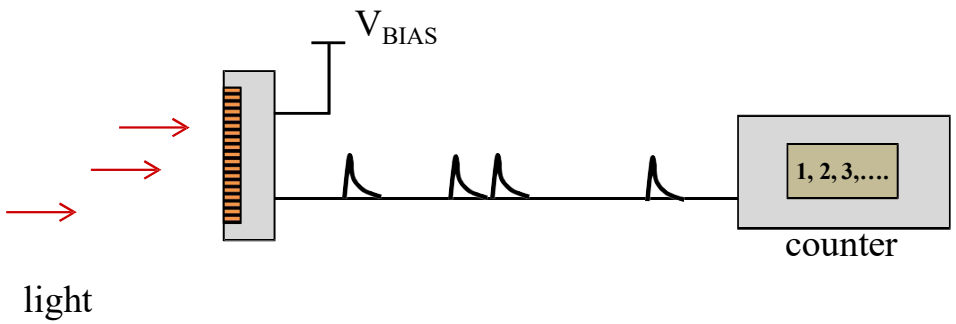


Example of single-photoelectron waveform (1 p.e.)

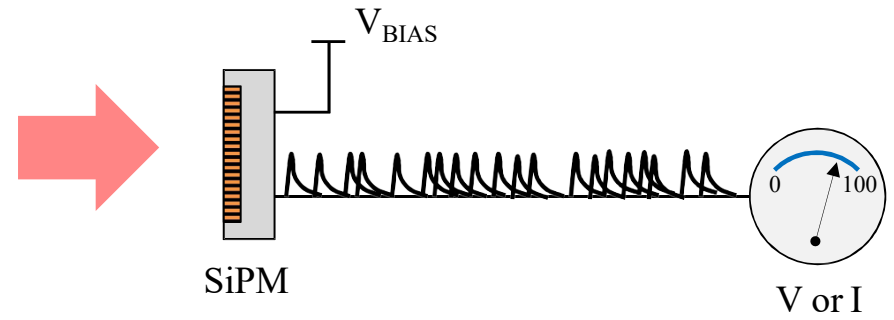
Gain = area under the curve in electrons

Overvoltage, $\Delta V = V_{BIAS} - V_{BD}$

Silicon photomultiplier: modes of operation



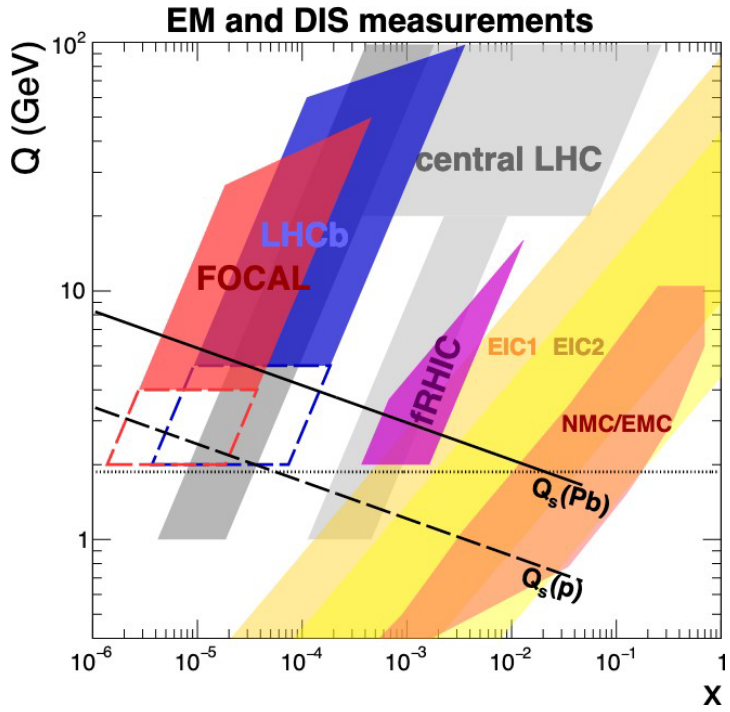
If the pulses are distinguishable, SiPM can be operated in a **photon counting** mode.



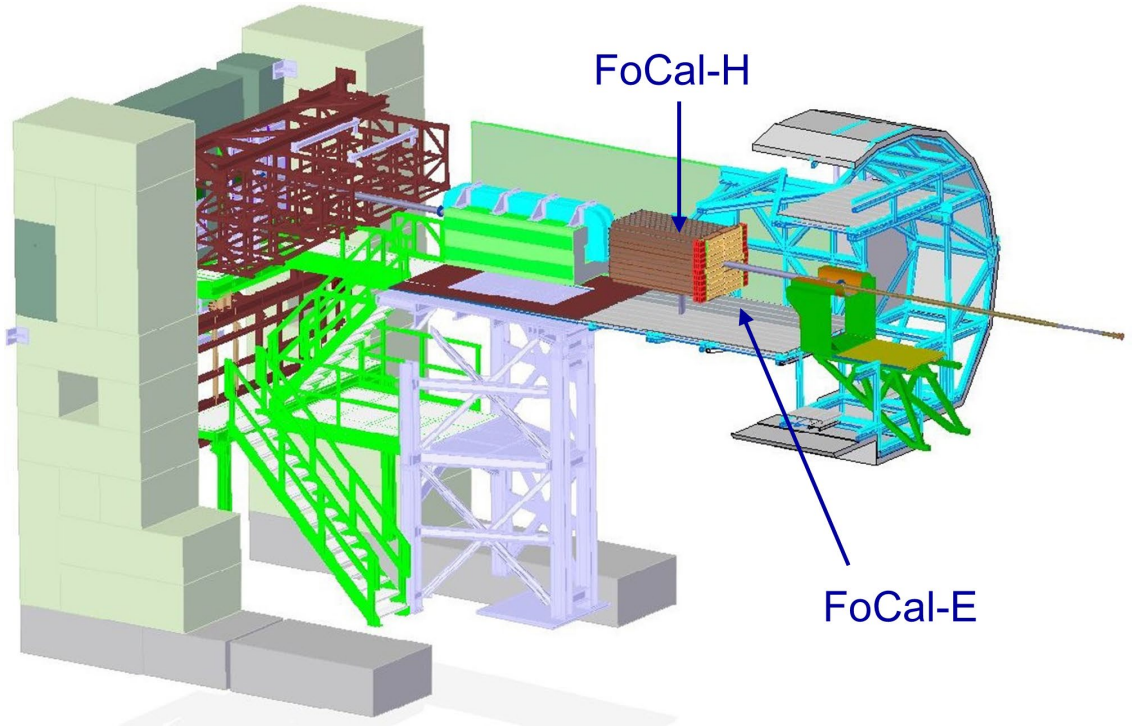
If the pulses overlap, the SiPM can be operated in an **analog mode**. The measured output is voltage or current.

Forward Calorimeter

- Physics Goal: unravel nucleus structure at small-x
  - Unique capabilities to measure **direct photons** in pp and p-Pb
  - Study the **gluon distributions** at **small-x** scale and **low Q**



FoCal LoI - CERN-LHCC-2020-009



$3.4 < \eta < 5.8$
(baseline design @ 7 m from IP)